74LV245AT

Octal bus transceiver; 3-state

Rev. 1 — 3 June 2016 Product data sheet

1. General description

The 74LV245AT is an 8-bit transceiver with 3-state outputs. The device features an output enable ($\overline{OE}$) and send/receive (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

The 74LV245AT is designed to operate over a V_{CC} range from 4.5 V to 5.5 V. The inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I_{OFF}.
The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t_{pd} of 3.1 ns at 5 V
- Typical $V_{OL(p)}$ < 0.8 V at V_{CC} = 5 V, T_{amb} = 25 °C
- Typical $V_{OH(v)}$ > 2.3 V at V_{CC} = 5 V, T_{amb} = 25 °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 2 kV
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV245ATPW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LV245ATBQ	−40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

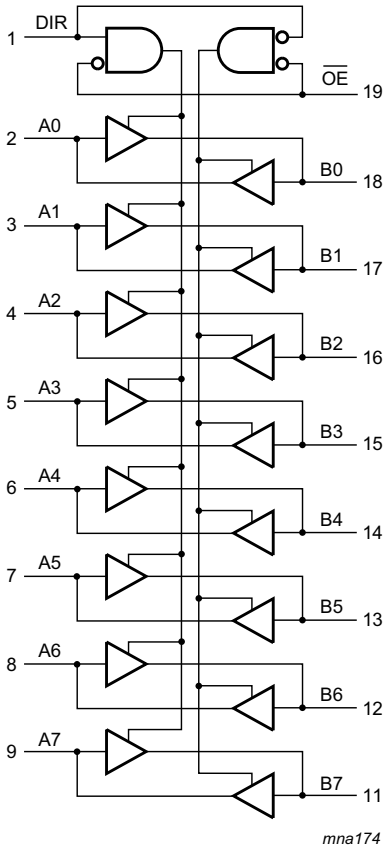


Fig 1. Logic symbol

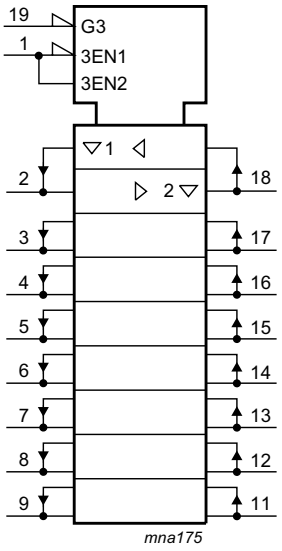


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

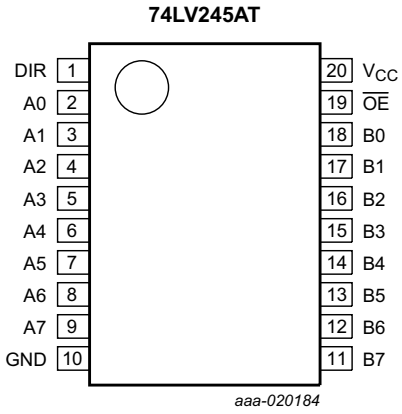
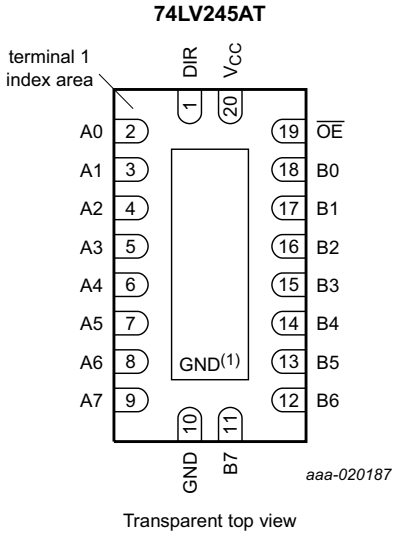


Fig 3. Pin configuration TSSOP20



Transparent top view

(1) This pad is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 4. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0 to B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
$\overline{OE}$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7.0	V
V_I	input voltage	[1]	−0.5	+7.0	V
V_O	output voltage	active mode [2][3]	−0.5	V_{CC} + 0.5	V
		power-down or 3-state mode [2]	−0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V	−20	-	mA
I_{OK}	output clamping current	V_O < 0 V	−50	-	mA
I_O	output current	V_O = 0 V to V_{CC}	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		−70	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C [4]	-	500	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7.0 V maximum.

[4] For TSSOP20 package: above 100 °C, the value of P_{tot} derates linearly with 10 mW/K.
For DHVQFN20 package: above 110 °C, the value of P_{tot} derates linearly with 12.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		power-down or 3-state mode	0	5.5	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 5.0 V ± 0.5 V	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2	-	-	2	-	2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −16 mA	3.94	-	-	3.8	-	3.8	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 16 mA	-	-	0.44	-	0.55	-	0.55	V
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = GND to 5.5 V; V_{CC} = 0 V	-	-	0.5	-	5	-	5	μA
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2	-	20	-	20	μA
ΔI_{CC}	additional supply current	per input pin; V_I = 3.4 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Figure 7.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	An to Bn or Bn to An; see Figure 5 [2]								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.1	7.7	1	8.5	1	9.7	ns
		C_L = 50 pF	-	4.4	8.7	1	9.5	1	10.7	ns
t_{en}	enable time	$\overline{OE}$ to An or $\overline{OE}$ to Bn; see Figure 6								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.5	13.8	1	15	1	16.3	ns
		C_L = 50 pF	-	5.8	14.8	1	16	1	17.3	ns
t_{dis}	disable time	$\overline{OE}$ to An or $\overline{OE}$ to Bn; see Figure 6 [2]								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.8	7.5	1	8	1	8.6	ns
		C_L = 50 pF	-	6.0	15.4	1	16.5	1	17	ns
$t_{sk(o)}$	output skew time	V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	-	1	-	1	-	1	ns
C_I	input capacitance	V_I = V_{CC} or GND; V_{CC} = 5 V	-	2	6	-	6	-	6	pF
$C_{I/O}$	input/output capacitance	V_O = V_{CC} or GND; V_{CC} = 5 V	-	5.5	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 10 MHz; V_I = GND to V_{CC} [3]	-	10.3	-	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5 V.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

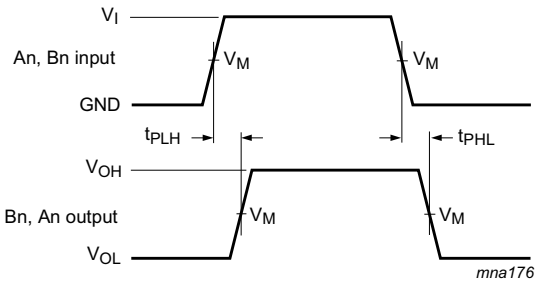
[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts.

Table 8. Noise characteristics

GND = 0 V. For test circuit, see Figure 7.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
V_{CC} = 5 V; C_L = 50 pF						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.6	1.5	V
$V_{OL(v)}$	LOW-level output voltage (valley)		−1.5	−0.6	-	V
$V_{OH(v)}$	HIGH-level output voltage (valley)		-	4.0	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage	dynamic	2	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	dynamic	-	-	0.8	V

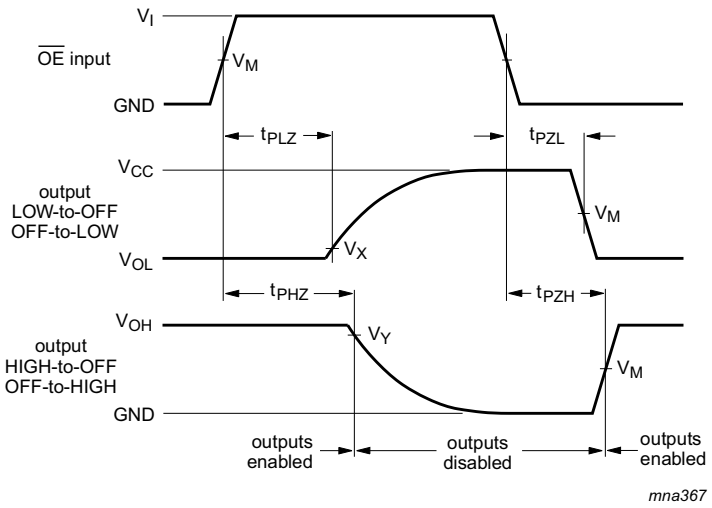
11. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (An, Bn) to output (Bn, An)



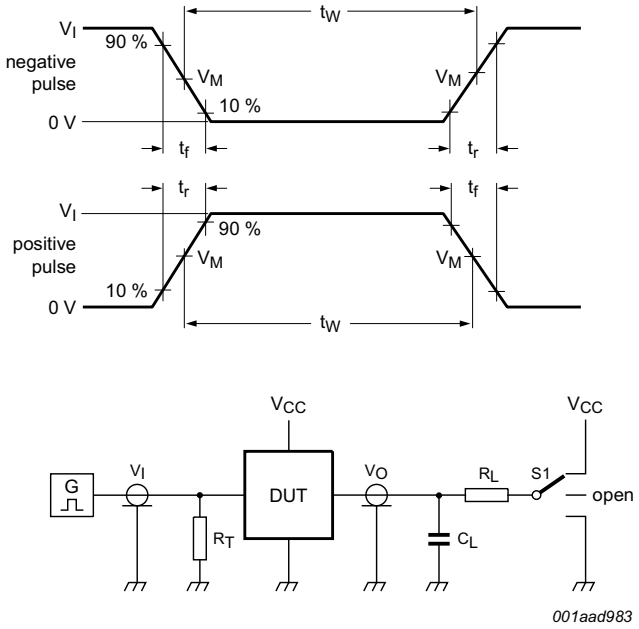
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Enable and disable times

Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

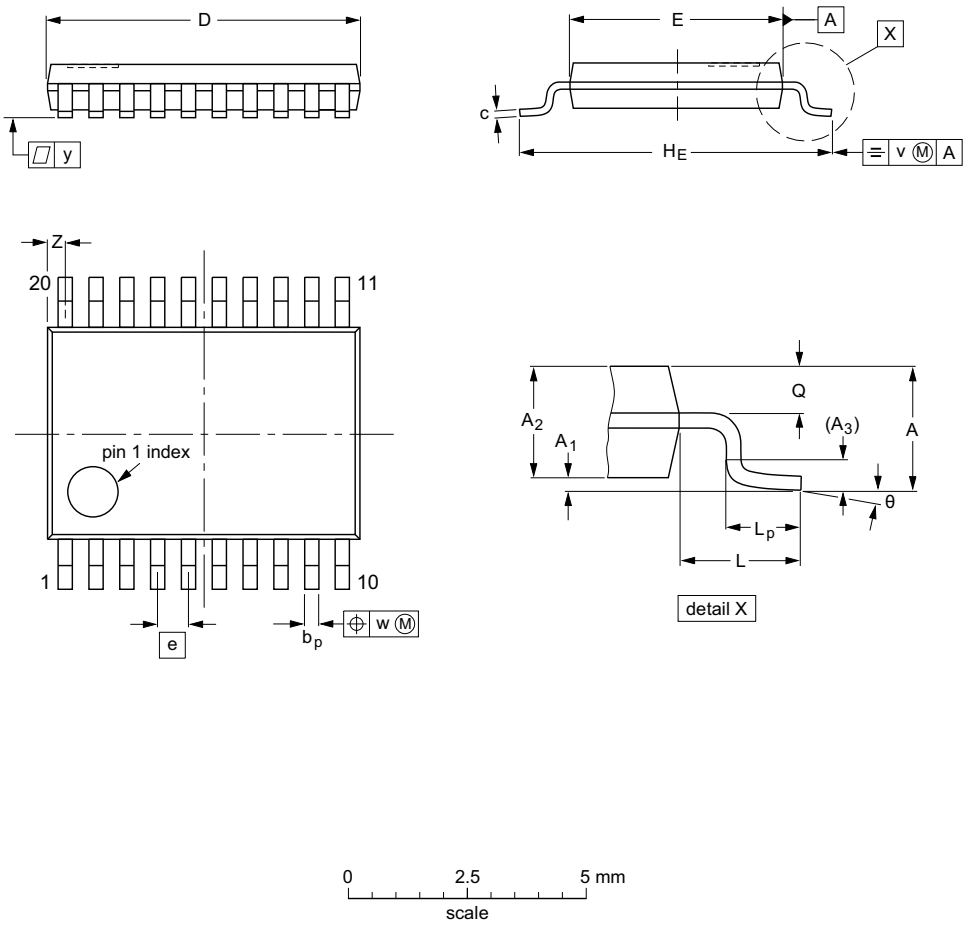
Fig 7. Test circuit for measuring switching times

Table 10. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
GND to 3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

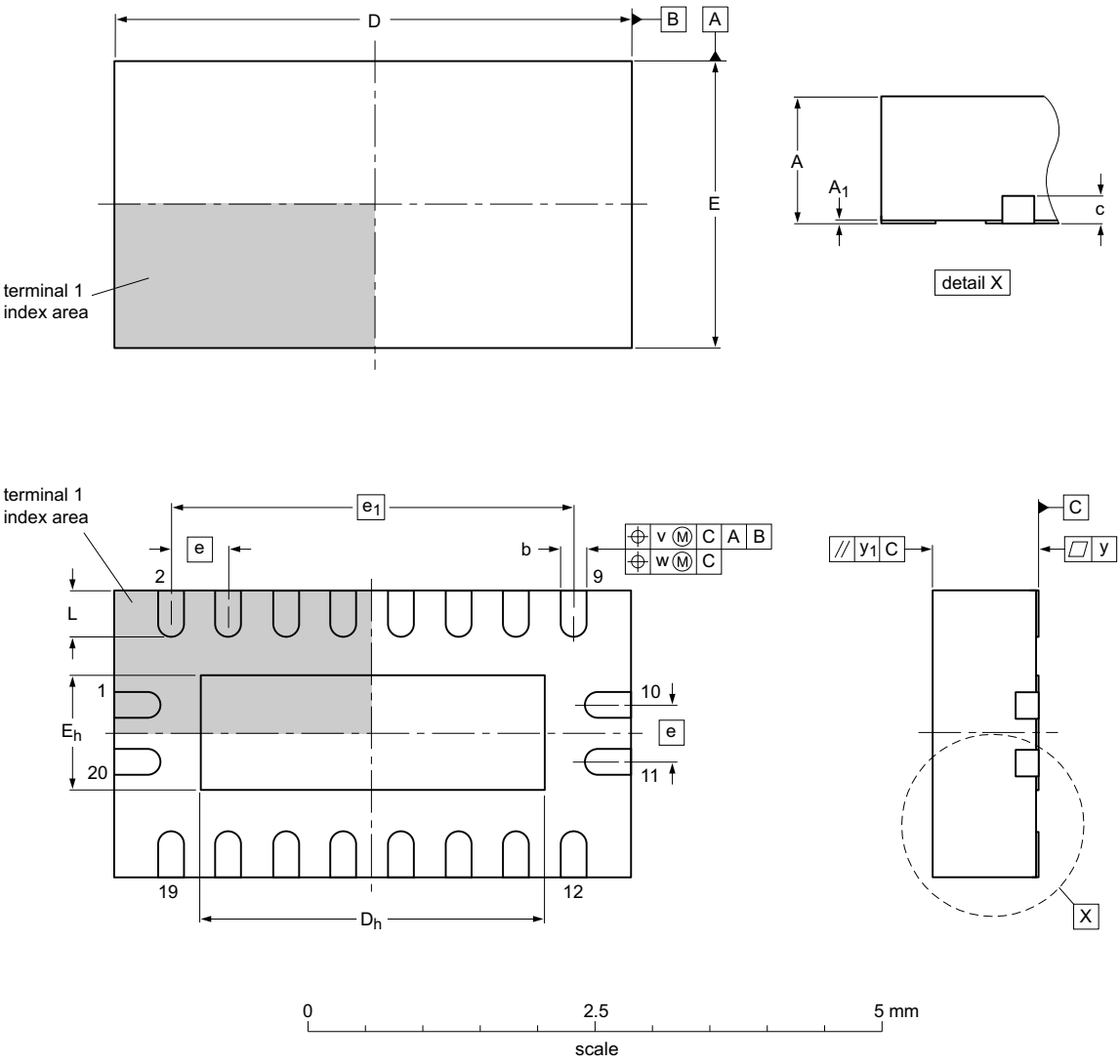
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig 9. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV245AT v.1	20160603	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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17. Contents

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