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Kind regards,

Team Nexperia

PHD78NQ03LT

N-channel TrenchMOS logic level FET

Rev. 06 — 11 June 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources

1.3 Applications

- Computer motherboards
- DC-to-DC convertors

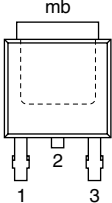
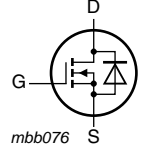
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 ; see Figure 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	107	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 12\text{ V}; T_j = 25\text{ °C};$ see Figure 11 ; see Figure 12	-	4	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 9 ; see Figure 10	-	7.65	9	m Ω

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;">SOT428 (SC-63; DPAK)</p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain [1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

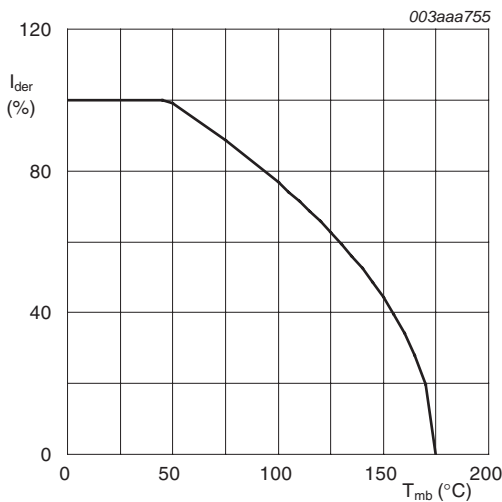
Type number	Package		Version
	Name	Description	
PHD78NQ03LT	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

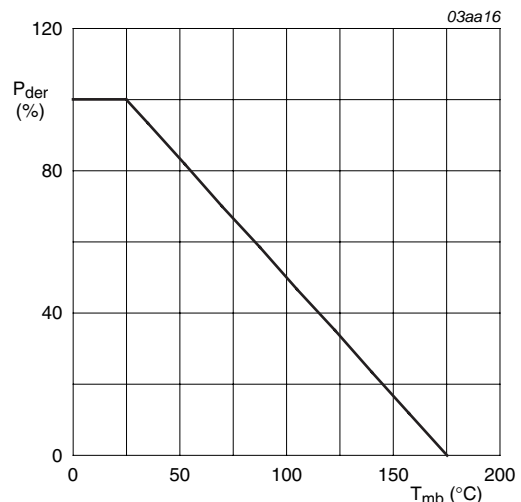
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	25	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ; T _{mb} ≥ 25 °C; T _{mb} ≤ 175 °C	-	25	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 100 °C	-	46.9	A
		V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	57.5	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1 ; see Figure 3	-	75	A
		V _{GS} = 5 V; T _{mb} = 25 °C	-	66.4	A
I _{DM}	peak drain current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C; see Figure 3	-	240	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	107	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	75	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	240	A
Avalanches ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _j (init) = 25 °C; I _D = 32 A; V _{sup} ≤ 25 V; unclamped; R _{GS} = 50 Ω; t _p = 0.17 ms	-	100	mJ



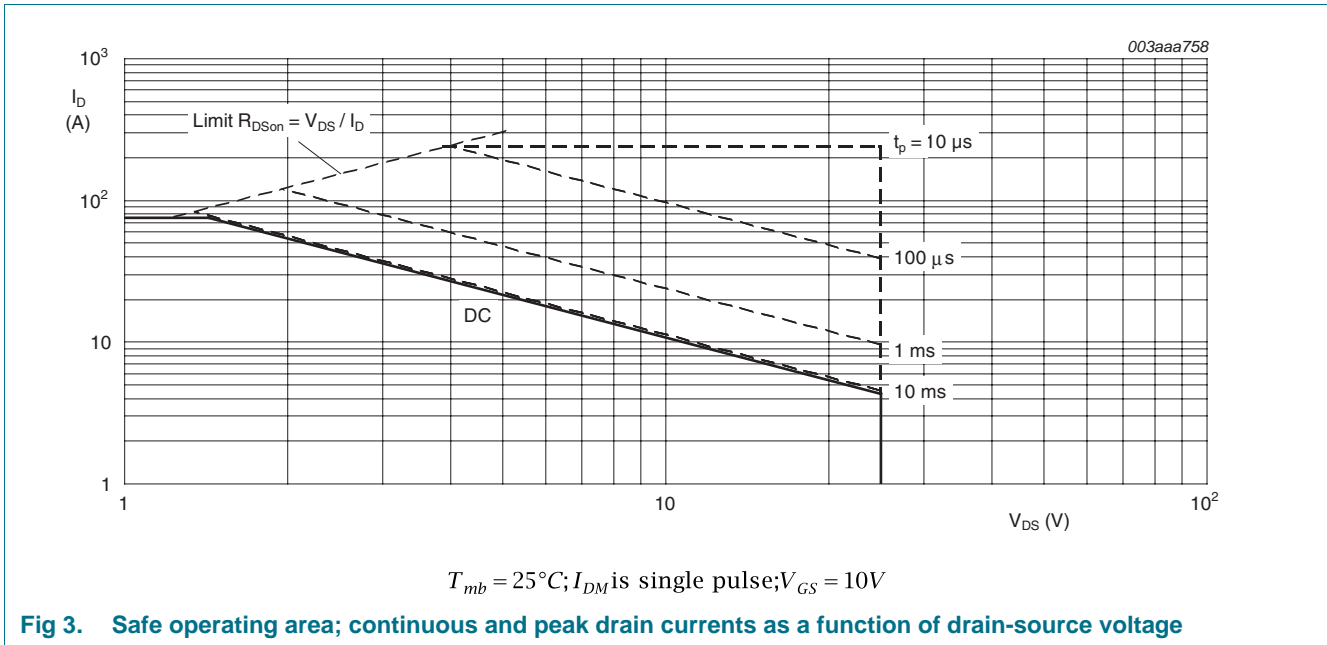
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

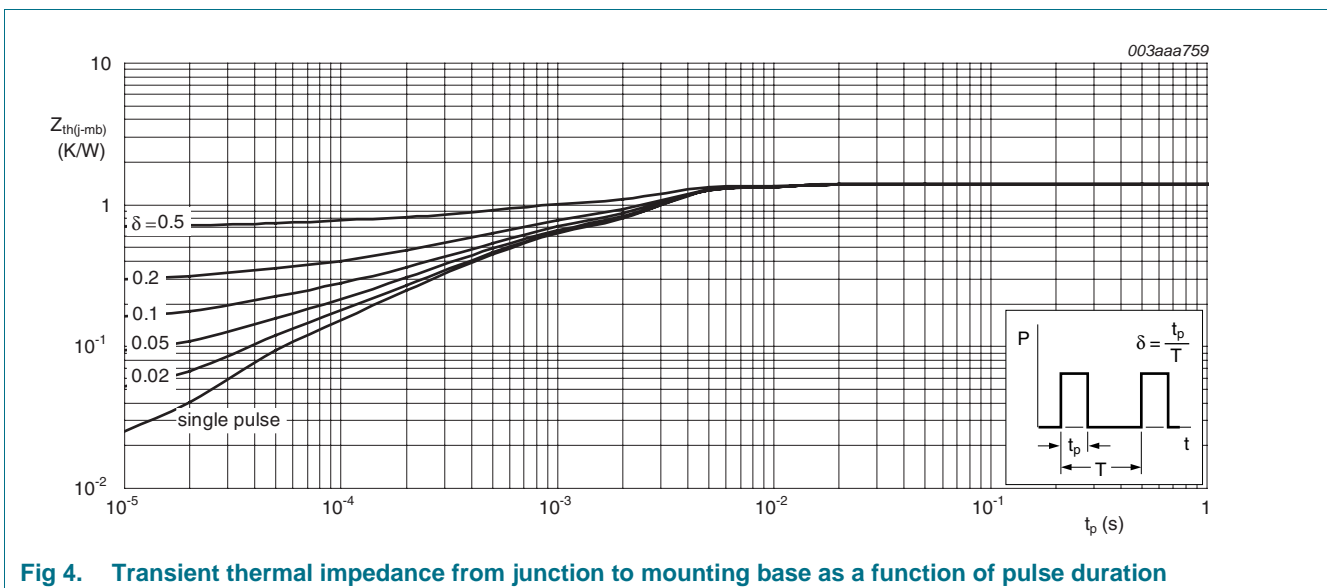


5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.4	K/W	
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint;	[1]	-	75	-	K/W
		SOT404 minimum footprint;	[1]	-	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 7 ; see Figure 8	-	-	2.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 7 ; see Figure 8	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 7 ; see Figure 8	1	1.5	2	V
I_{DSS}	drain leakage current	$V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 25 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 15 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	7.65	9	m Ω
		$V_{GS} = 5 V; I_D = 25 A; T_j = 175 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	18.9	24.3	m Ω
		$V_{GS} = 5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	-	10.5	13.5	m Ω
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	8.6	-	nC
		$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$; see Figure 11 ; see Figure 12	-	11	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$; see Figure 12 ; see Figure 12	-	3.6	-	nC
Q_{GS1}	pre-threshold gate-source charge		-	1.8	-	nC
Q_{GS2}	post-threshold gate-source charge		-	1.8	-	nC
Q_{GD}	gate-drain charge		-	4	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 12 V; T_j = 25 \text{ }^\circ C$; see Figure 11 ; see Figure 12	-	3	-	V
C_{iss}	input capacitance	$V_{DS} = 12 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; see Figure 13	-	970	-	pF
		$V_{DS} = 0 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	1460	-	pF
C_{oss}	output capacitance	$V_{DS} = 12 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; see Figure 13	-	415	-	pF
C_{rss}	reverse transfer capacitance		-	170	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\ \Omega; V_{GS} = 5\text{ V};$	-	13	-	ns
t_r	rise time	$R_{G(ext)} = 5.6\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	46	-	ns
$t_{d(off)}$	turn-off delay time		-	20	-	ns
t_f	fall time		-	15	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 14	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	35	-	ns
Q_r	recovered charge	$V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	20	-	nC

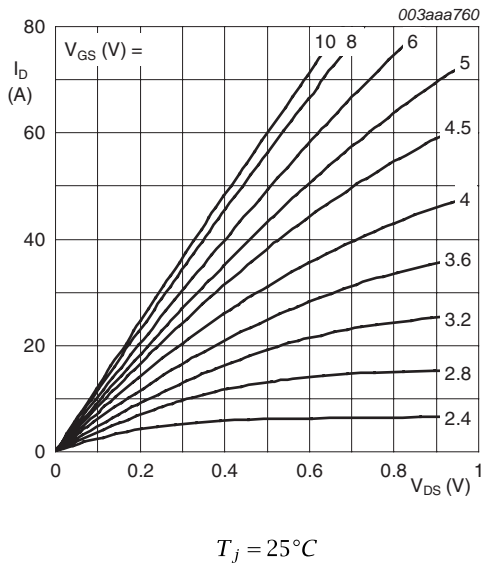


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

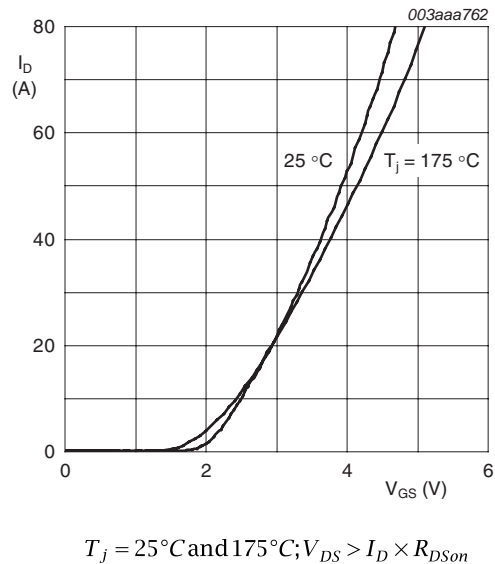
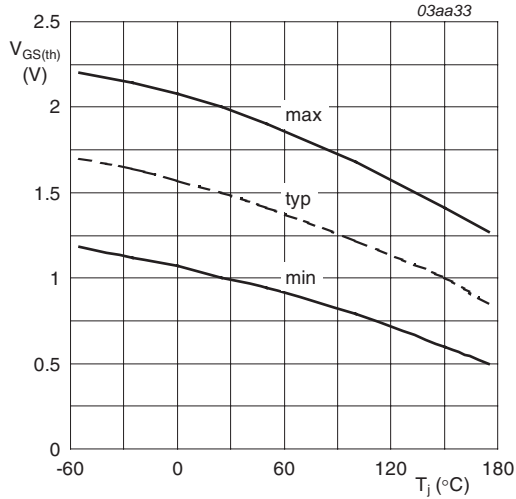
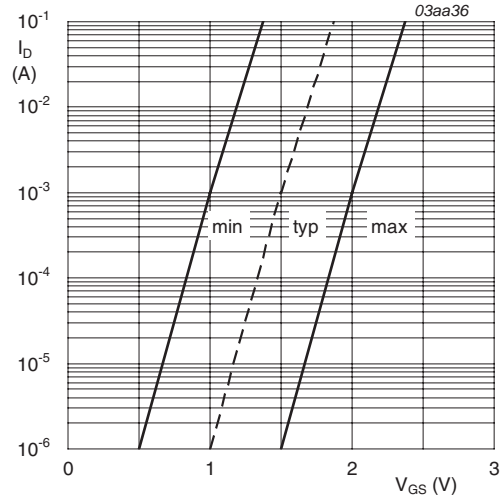


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



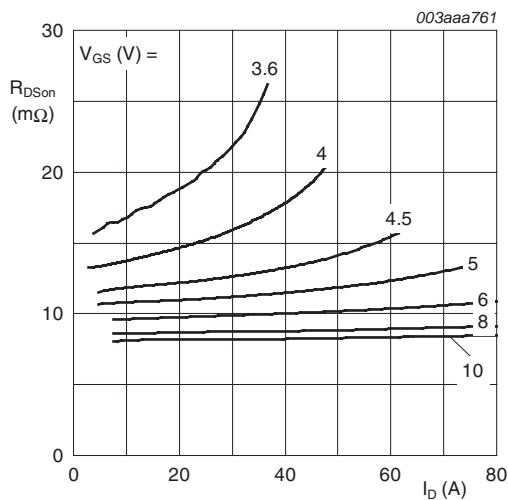
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 7. Gate-source threshold voltage as a function of junction temperature



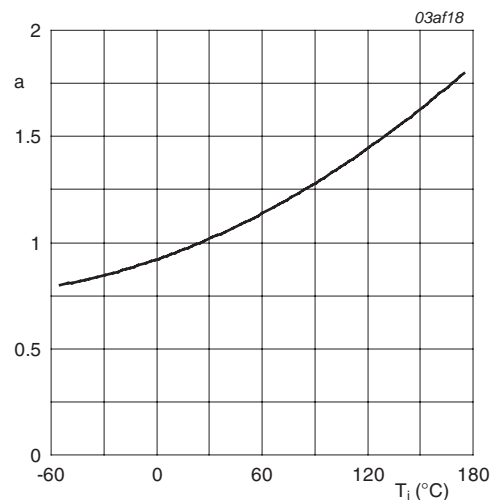
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



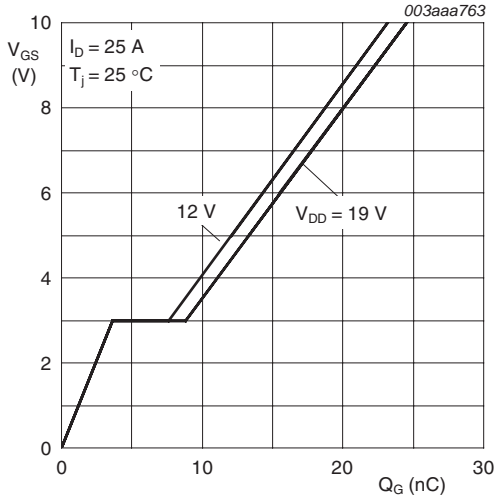
$$T_j = 25\text{ }^\circ\text{C}$$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



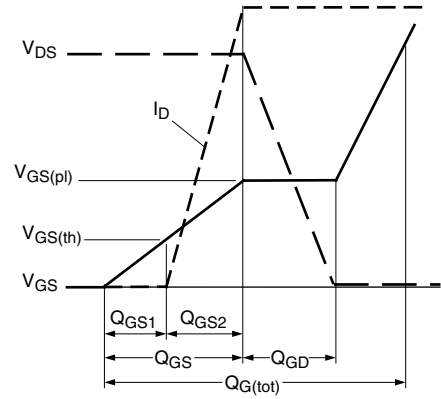
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



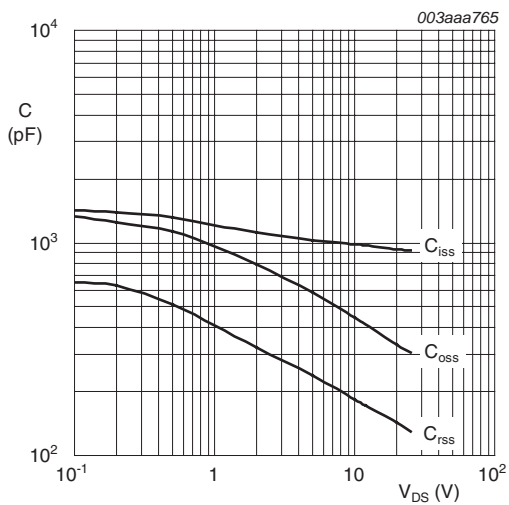
$I_D = 25A; V_{DS} = 12V \text{ and } 19V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



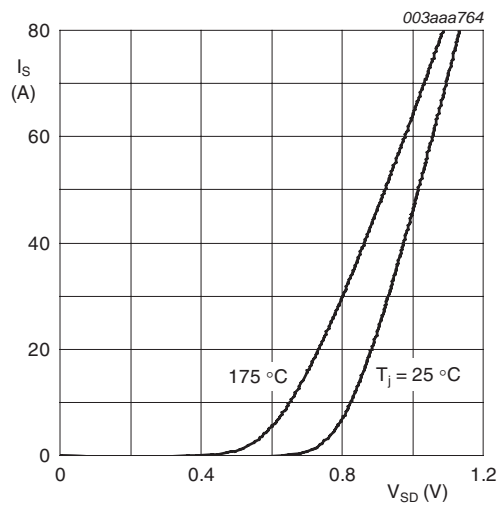
003aaa508

Fig 12. Gate charge waveform definitions



$V_{GS} = 0V; f = 1MHz$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ C \text{ and } 175^\circ C; V_{GS} = 0V$

Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

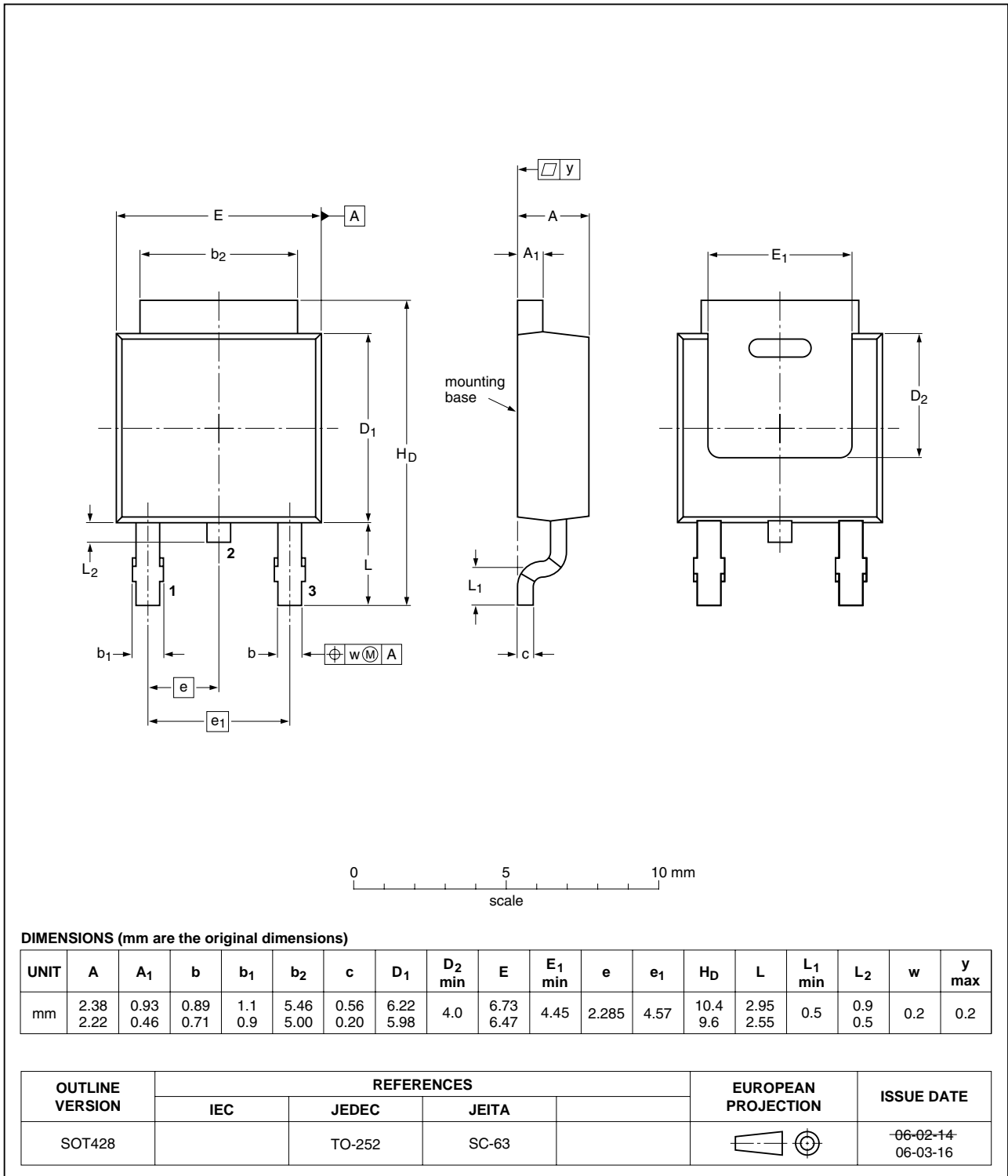


Fig 15. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD78NQ03LT_6	20090611	Product data sheet	-	PHU_PHD78NQ03LT_5
Modifications:				<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate.
PHU_PHD78NQ03LT_5 (9397 750 15084)	20050727	Product data sheet	-	PHP_PHU78NQ03LT_4
PHP_PHU78NQ03LT_4 (9397 750 13431)	20040726	Product data sheet	-	PHP_PHB_PHD78NQ03LT-03
PHP_PHB_PHD78NQ03LT-03 (9397 750 09667)	20020626	Product data	-	PHP_PHB_PHD78NQ03LT-02
PHP_PHB_PHD78NQ03LT-02 (9397 750 09418)	20020322	Product data	-	PHP_PHB_PHD78NQ03LT-01
PHP_PHB_PHD78NQ03LT-01 (9397 750 08916)	20011114	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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