INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT652

Octal bus transceiver/register; 3-state

Product specification
File under Integrated Circuits, IC06

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Philips
Semiconductors

PHILIPS

Octal bus transceiver/register; 3-state 74HC/HCT652

FEATURES

- Multiplexed real-time and stored data
- Independent register for A and B buses
- Independent enables for A and B buses
- 3-state
- Output capability: Bus driver
- Low power consumption by CMOS technology
- I_{CC} category: MSI.

APPLICATIONS

- Bus interfaces.

DESCRIPTION

The 74HC/HCT652 are high-speed SI-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with Jedec standard no. 7A.

The 74HC/HCT652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and central circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the “A” or “B” or both buses, will be stored in the internal registers, at the appropriate clock pins (CP_{AB} or CP_{BA}) regardless of the select pins (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control pins. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the output enable pins this operating mode permits. The output enable pins OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input. Thus when all other data sources to the two sets of bus lines are at high-impedance, each set of the bus lines will remain at its last state. This type differs from the HC/HCT646 in one extra bus-management function. This is the possibility to transfer stored “A data to the “B” bus and transfer stored ”B” data to the ”A” bus at the same time. The examples at the application information demonstrate all bus management functions. Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns; V_{CC} = 4.5 V; C_L = 50 pF.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PLH}/t_{PZL}	propagation delay A_n/B_n to B_n/A_n	C_L = 15 pF; V_{CC} = 5 V	13	13	ns
	propagation delay CP_{AB}/CP_{BA} to B_n/A_n		18	20	ns
	propagation delay S_{AB}/S_{BA} to B_n/A_n		20	23	ns
t_{PHZ}/t_{PZL}	3-state output enable time $OE_{AB}/\overline{OE}_{BA}$ to B_n/A_n		14	15	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $OE_{AB}/\overline{OE}_{BA}$ to B_n/A_n		12	13	ns
f_{max}	maximum clock frequency		92	92	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per channel	notes 1 and 2	26	28	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

Octal bus transceiver/register; 3-state 74HC/HCT652

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT652N	24	DIL	plastic	SOT101L
74HC/HCT652D	24	SO	plastic	SOT137A

PINNING

SYMBOL	PIN	DESCRIPTION
CP_{AB}	1	A to B clock input
S_{AB}	2	select A to B source input
OE_{AB}	3	output enable A to B input
$A_0..A_7$	4..11	A data inputs/outputs
GND	12	ground (0 V)
$B_7..B_0$	13..20	B data inputs/outputs
$\overline{OE}_{BA}$	21	output enable B to A input
S_{BA}	22	select B to A source input
CP_{BA}	23	B to A clock input
V_{CC}	24	positive supply voltage

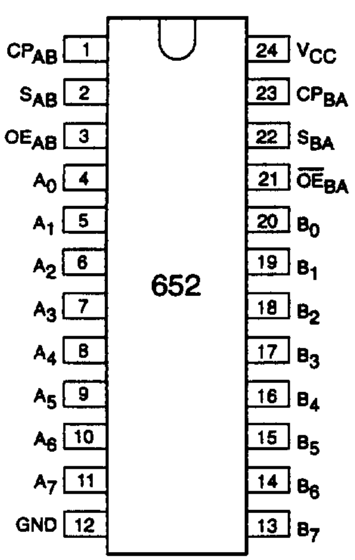


Fig.1 Pin configuration.

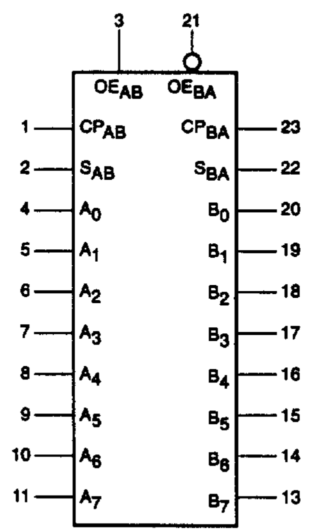


Fig.2 Logic symbol.

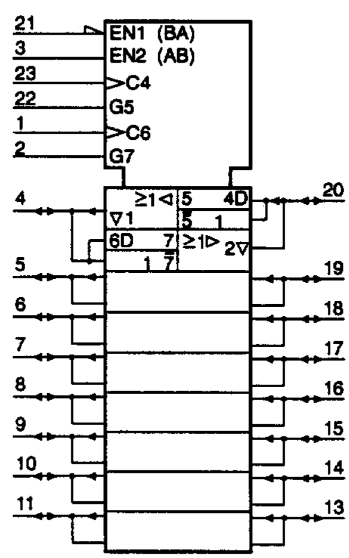


Fig.3 IEC logic symbol.

FUNCTION TABLE

INPUTS [1]						DATA I/O [2]		OPERATION OR FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_1 THRU A_8	B_1 THRU B_8	HC/HCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B
L	L	↑	↑	X	L	Ouput	Input	Store B in both registers
L	L	X	X	X	L	Ouput	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH transition
2. The data output functions may be enabled or disabled by various signals at OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

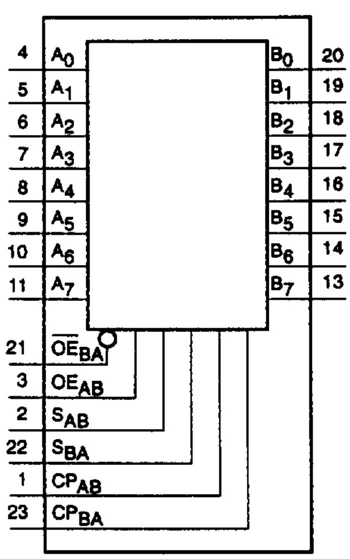


Fig.4 Functional diagram.

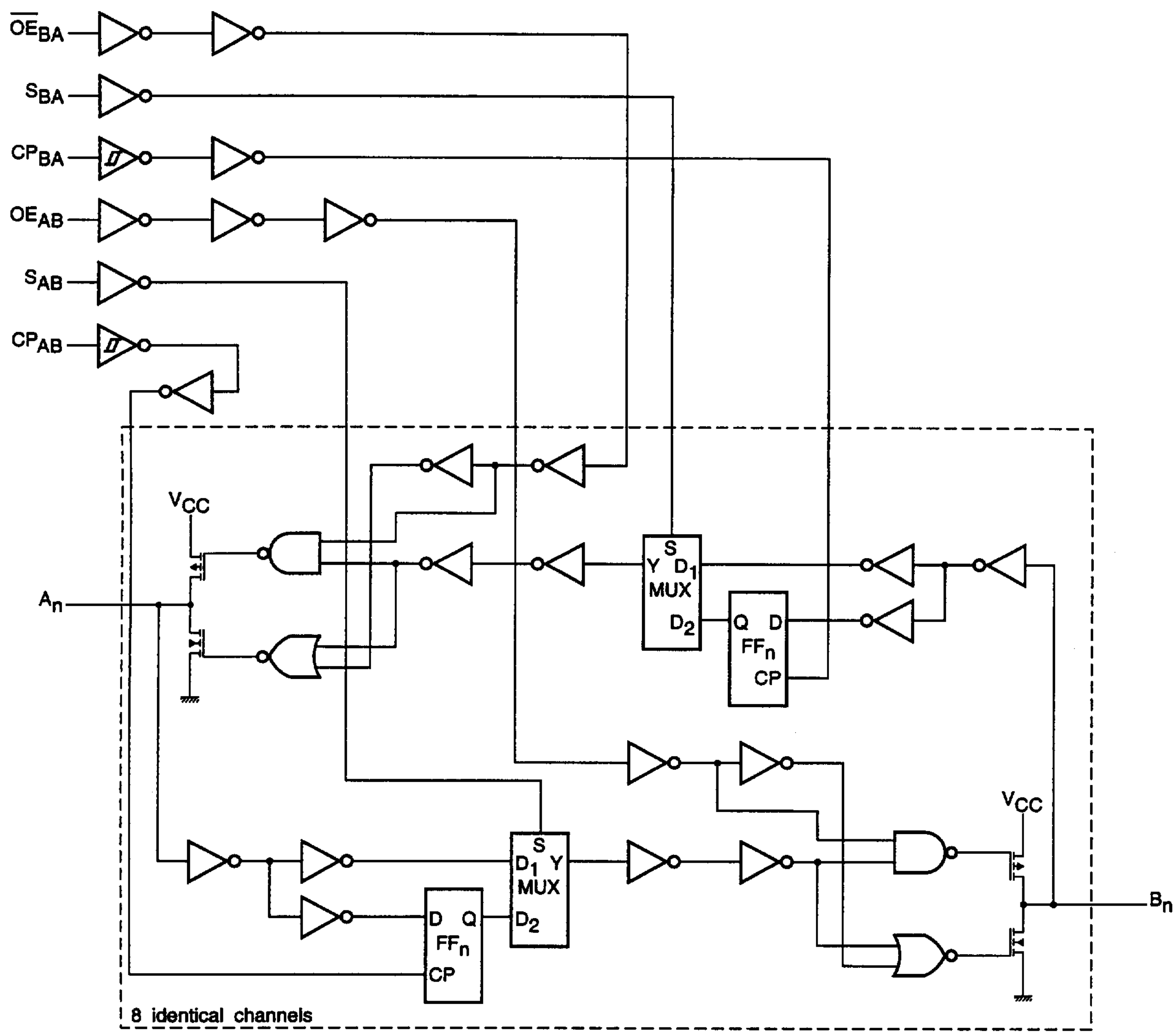


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Output capability: bus driver
I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 MIN.	TYP.	MAX.	−40 to +85 MIN.	MAX.	−40 to +125 MIN.	MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	– – –	44 16 13	135 27 23	– – –	170 34 29	– – –	205 41 35	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	– – –	61 22 18	190 38 32	– – –	240 48 41	– – –	285 57 48	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	– – –	63 23 18	195 39 33	– – –	245 49 42	– – –	295 59 50	ns	2.0 4.5 6.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	– – –	47 17 14	150 30 26	– – –	190 38 33	– – –	225 45 38	ns	2.0 4.5 6.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	– – –	41 15 12	150 30 26	– – –	190 38 33	– – –	225 45 38	ns	2.0 4.5 6.0	Fig.9
t_{THL}/t_{TLH}	output transition time	– – –	14 5 4	60 12 10	– – –	75 15 13	– – –	90 18 15	ns	2.0 4.5 6.0	Figs 6, 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	80 16 14	17 6 5	– – –	100 20 17	– – –	120 24 20	– – –	ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	100 20 17	17 6 5	– – –	125 25 21	– – –	150 30 26	– – –	ns	2.0 4.5 6.0	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	25 5 4	–8 –3 –2	– – –	30 6 5	– – –	35 7 6	– – –	ns	2.0 4.5 6.0	Fig.7
f_{max}	maximum clock pulse frequency	6.0 30 35	16 83 98	– – –	4.8 24 28	– – –	4.0 20 24	– – –	MHz	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Output capability: bus driver
I_{CC} category: MSI.

Note to the HCT types

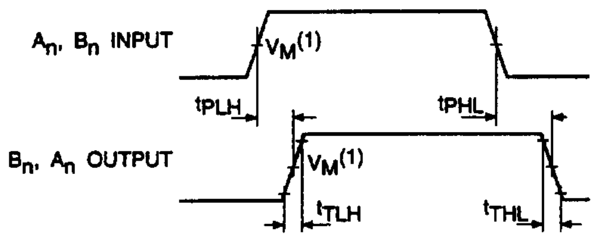
The value of additional quiescent supply current (ΔI_{CC}) for unit a load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below

INPUT	UNIT LOAD COEFFICIENT
S_{AB}, S_{BA}	0.75
A_0 to A_7 and B_0 to B_7	0.75
CP_{AB}, CP_{BA}	1.50
OE_{AB}	1.50
$\overline{OE}_{BA}$	1.50

AC CHARACTERISTICS FOR 74HCT

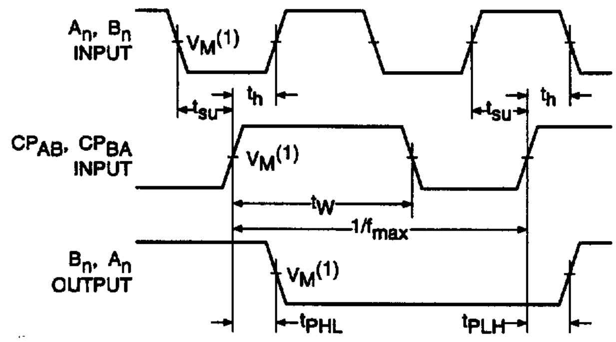
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

INPUT	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	–	16	27	–	34	–	41	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	–	23	39	–	49	–	59	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	–	27	46	–	55	–	66	ns	4.5	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	–	18	33	–	41	–	50	ns	4.5	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB}, $\overline{OE}_{BA}$ to A_n, B_n	–	16	35	–	44	–	53	ns	4.5	Fig.9
t_{THL}/t_{TLH}	output transition time	–	5	12	–	15	–	18	ns	4.5	Fig.6, 8
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	16	6	–	20	–	24	–	ns	4.5	Fig.7
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	10	5	–	13	–	15	–	ns	4.5	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	5	−2	–	6	–	8	–	ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	30	83	–	24	–	20	–	MHz	4.5	Fig.7



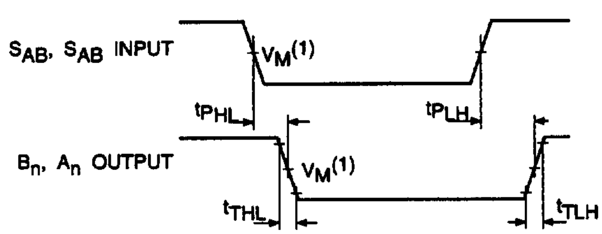
(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delay times and the output transition times.



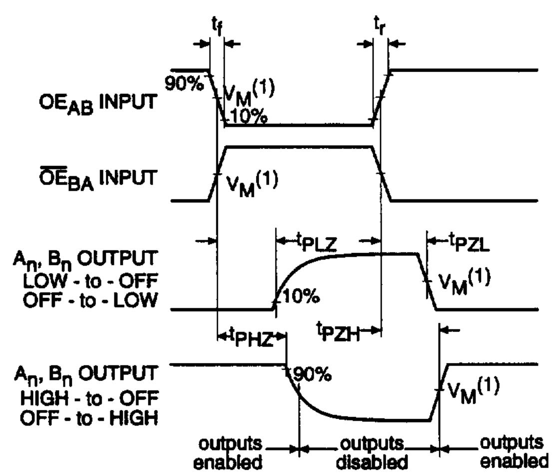
(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.



(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

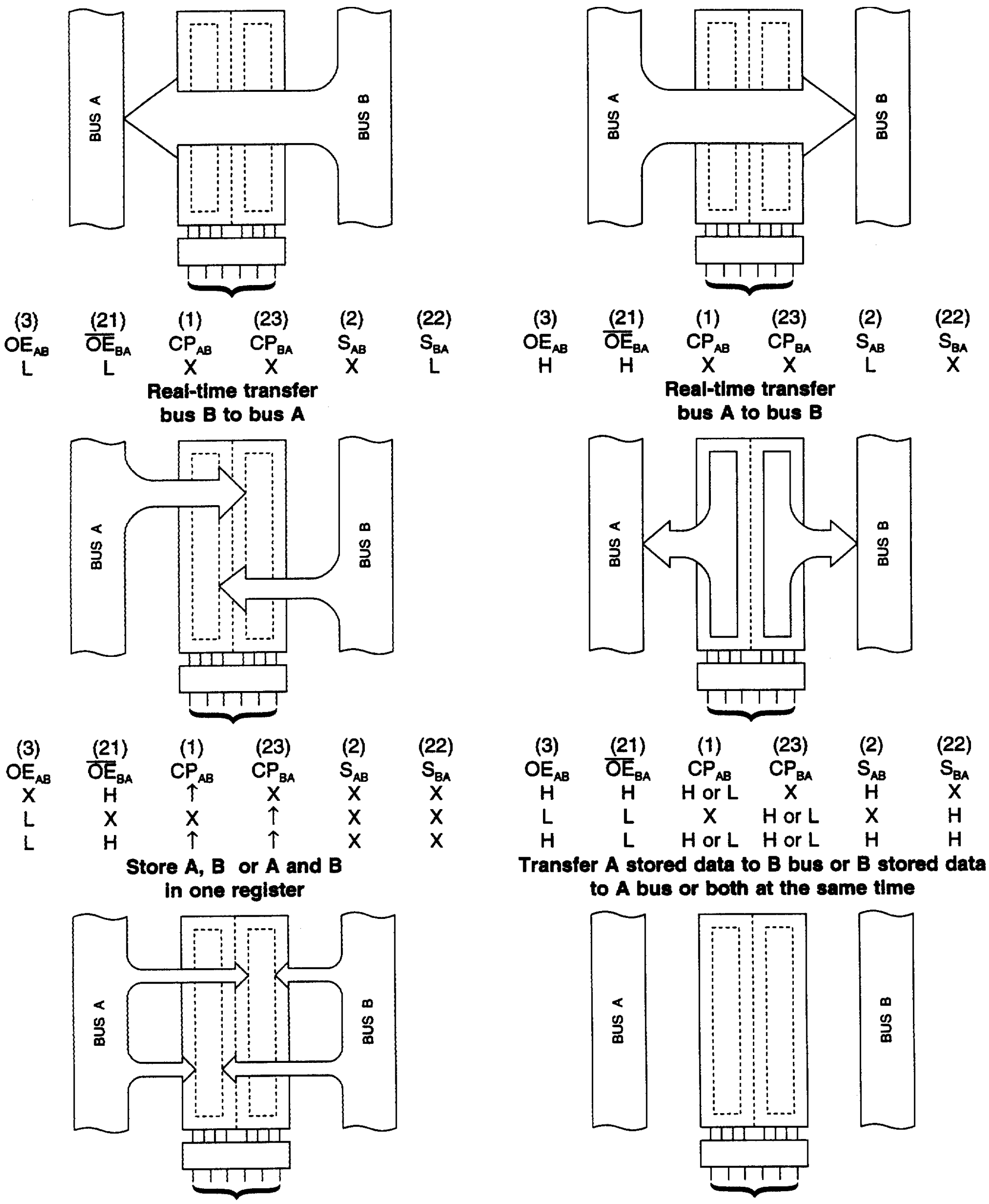
Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and the output transition times.



(1) HC: V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the output enable inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

APPLICATION INFORMATION



(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
L	L	X	X	X	L

Real-time transfer bus B to bus A

(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
H	H	X	X	L	X

Real-time transfer bus A to bus B

(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
X	H	$\uparrow$	X	X	X
L	X	X	$\uparrow$	X	X
L	H	$\uparrow$	$\uparrow$	X	X

Store A, B or A and B in one register

(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Transfer A stored data to B bus or B stored data to A bus or both at the same time

(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
H	H	$\uparrow$	$\uparrow$	L	X
L	L	$\uparrow$	$\uparrow$	X	L

Store bus A in both registers or store bus B in both registers

(3) OE_{AB}	(21) $\overline{OE}_{BA}$	(1) CP_{AB}	(23) CP_{BA}	(2) S_{AB}	(22) S_{BA}
L	H	H or L	H or L	X	X

Isolation

Fig.10 Application information.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.