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Kind regards,

Team Nexperia

PMG45UN

20 V, single N-channel Trench MOSFET

13 November 2012

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a SOT363 (SC-88) small Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J = 25\text{ °C}$	-	-	20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3.3	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3\text{ A}; T_J = 25\text{ °C}$	-	45	55	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

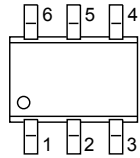
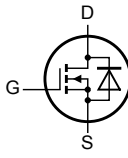


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2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa253</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMG45UN	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking codes

Type number	Marking code
PMG45UN	U5%

[1] % = placeholder for manufacturing site code

5. Limiting values

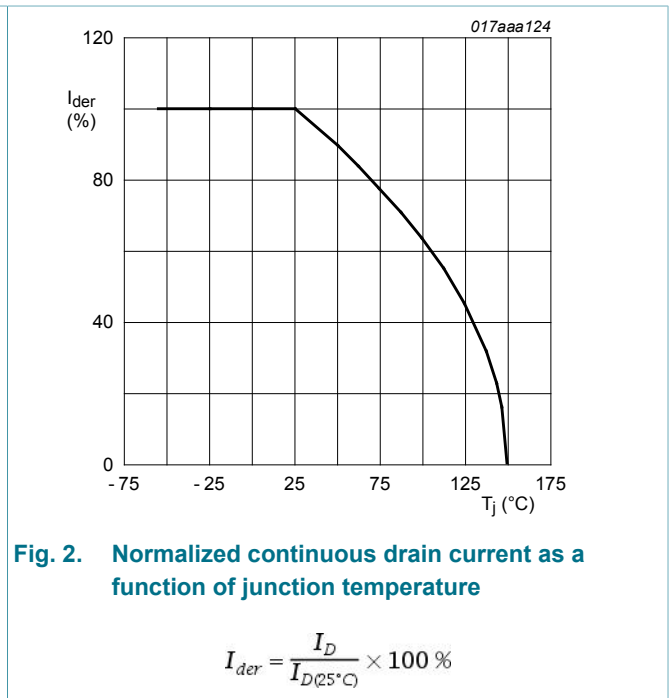
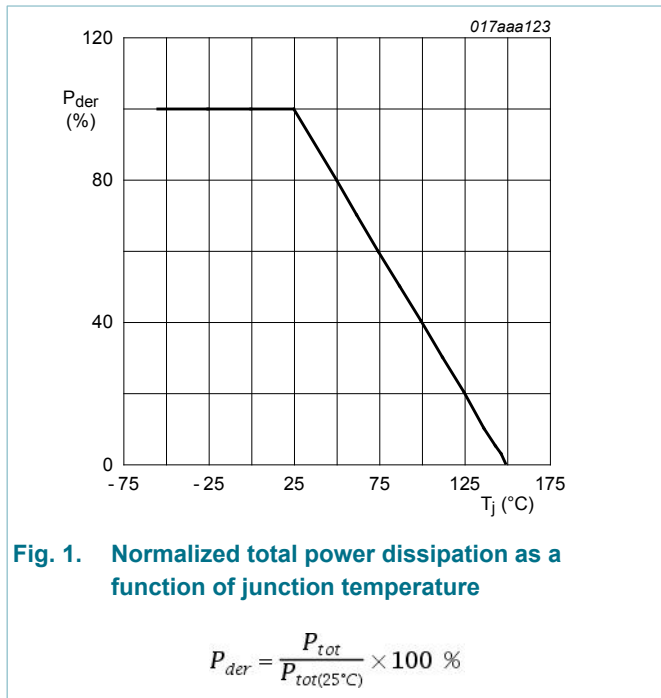
Table 5. Limiting values

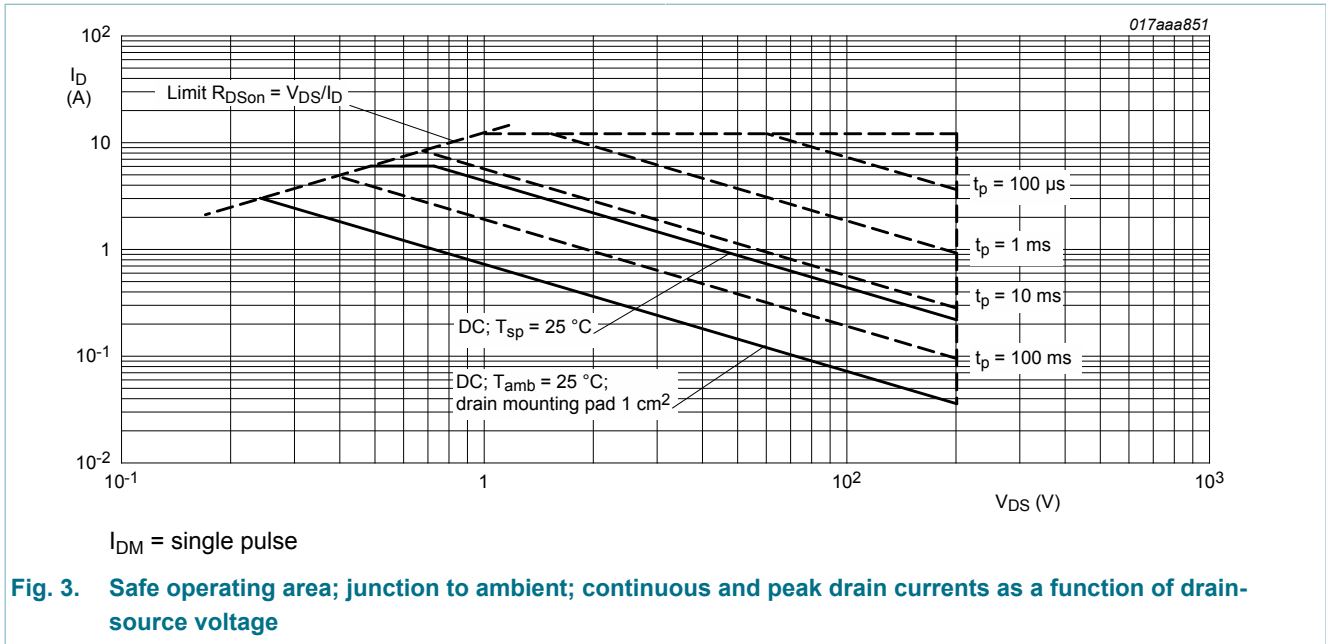
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3.3	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	3	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	1.9	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	12	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	375	mW
			[1]	-	715	mW

Symbol	Parameter	Conditions	Min	Max	Unit
		T _{sp} = 25 °C	-	4350	mW
T _j	junction temperature		-55	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C
Source-drain diode					
I _s	source current	T _{amb} = 25 °C	[1]	0.8	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





6. Thermal characteristics

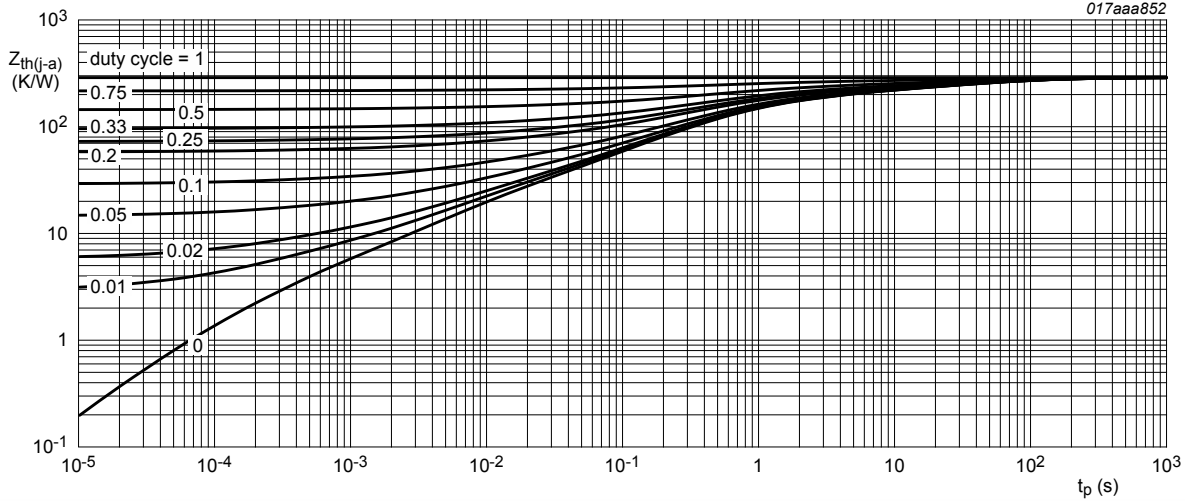
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	289	332	K/W
			[2]	-	152	175	K/W
			[3]	-	117	145	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	25	29	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

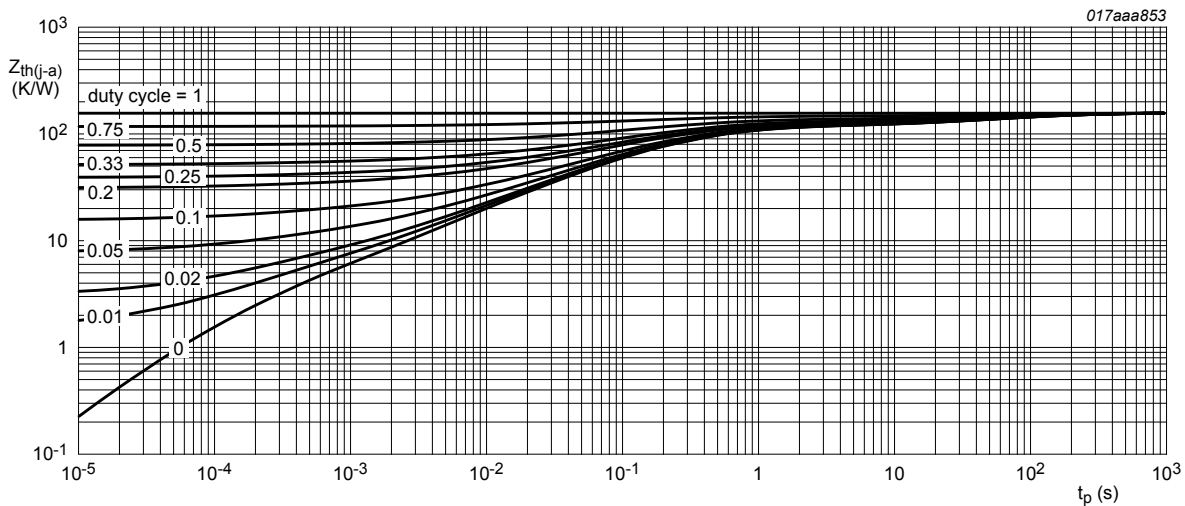
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 , $t \leq 5\text{ s}$.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

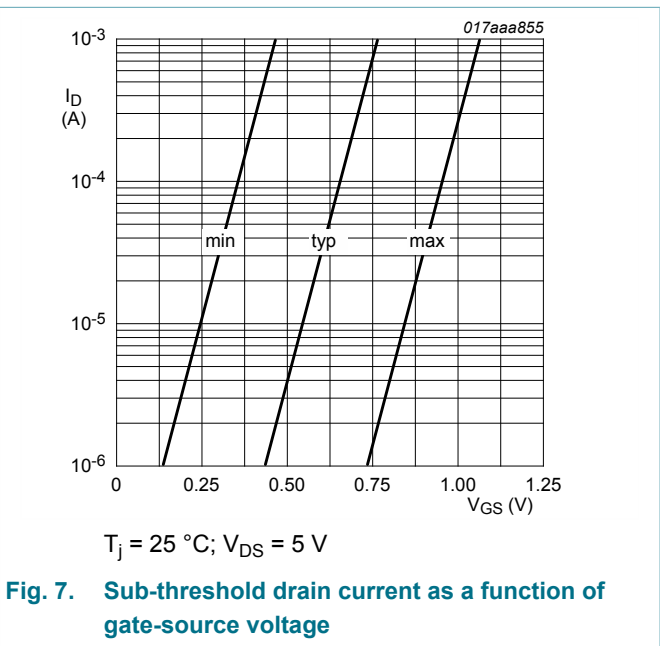
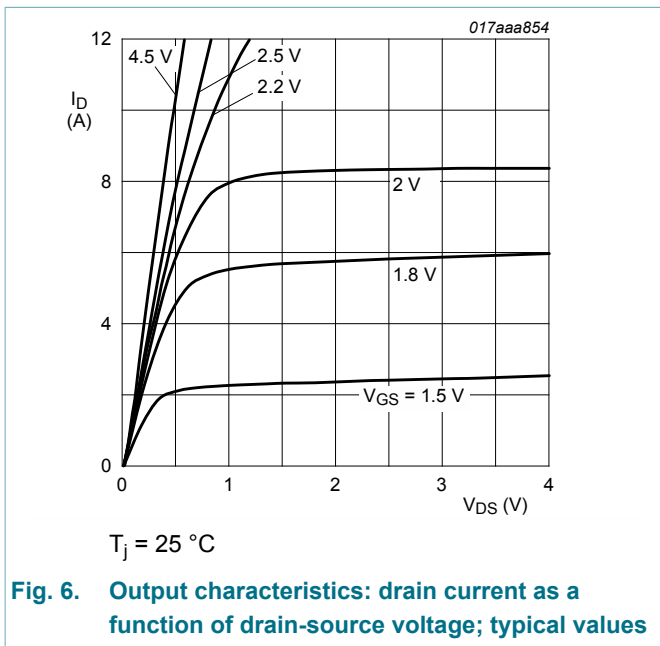
Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	0.4	0.7	1	V
I_{DSS}	drain leakage current	$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = -8\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	-100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	45	55	m Ω
		$V_{GS} = 4.5\text{ V}; I_D = 3\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	66	81	m Ω
		$V_{GS} = 2.5\text{ V}; I_D = 2.5\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	58	76	m Ω
		$V_{GS} = 1.8\text{ V}; I_D = 0.8\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	85	125	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	11.2	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10\text{ V}; I_D = 3\text{ A}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	2.2	3.3	nC
Q_{GS}	gate-source charge		-	0.32	-	nC
Q_{GD}	gate-drain charge		-	0.56	-	nC
C_{iss}	input capacitance	$V_{DS} = 10\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	184	-	pF
C_{oss}	output capacitance		-	51	-	pF
C_{rss}	reverse transfer capacitance		-	29	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\text{ V}; I_D = 3\text{ A}; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 6\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	8	-	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	30	-	ns
t_f	fall time		-	26	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 0.8\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.8	1.2	V



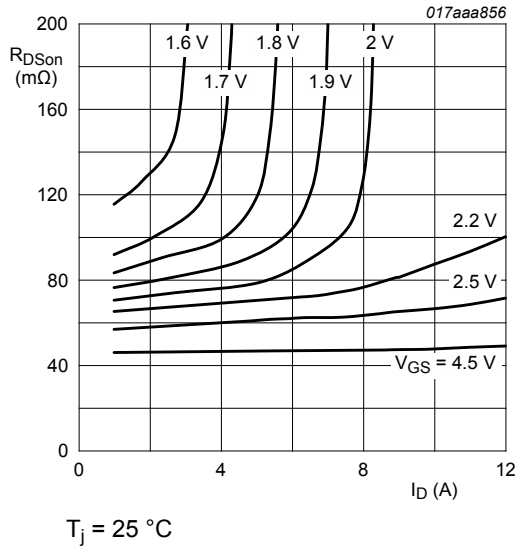


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

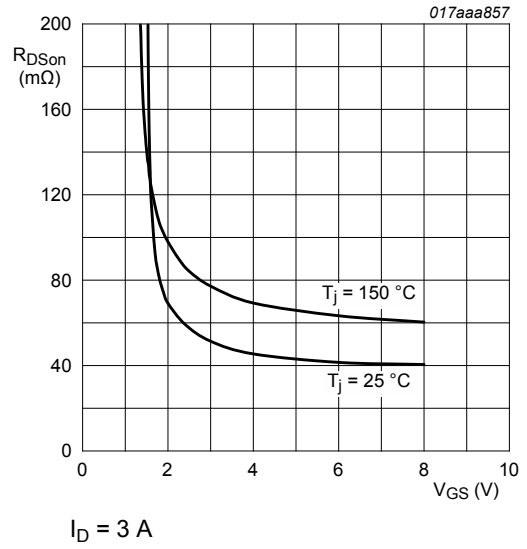


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

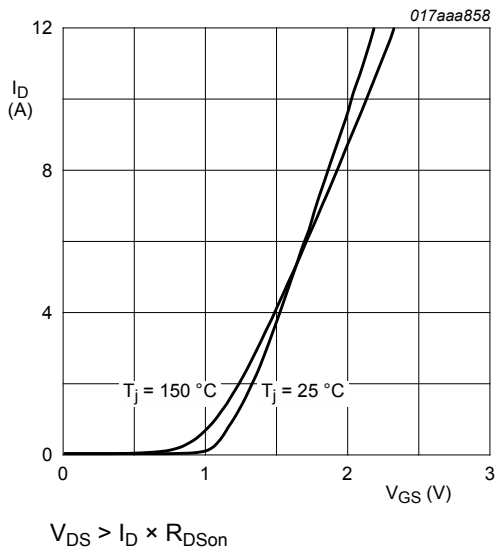


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

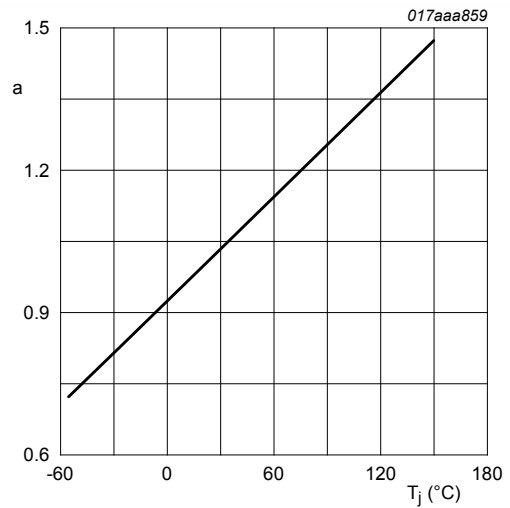


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

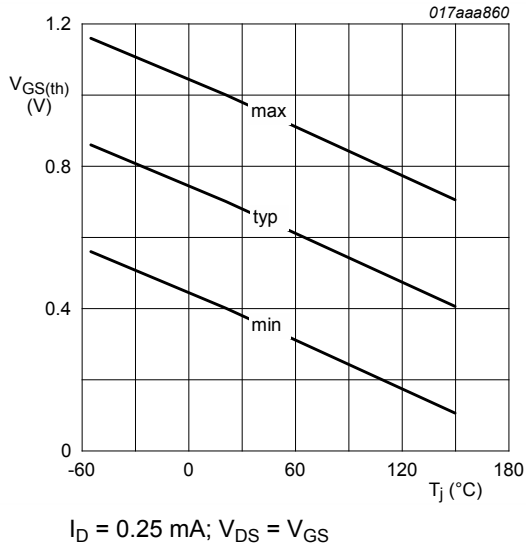


Fig. 12. Gate-source threshold voltage as a function of junction temperature

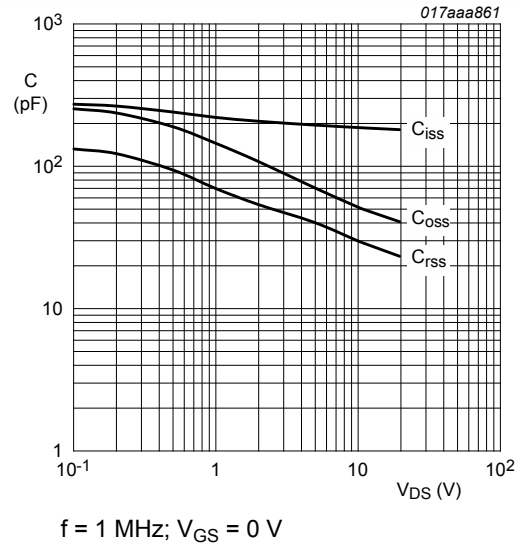


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

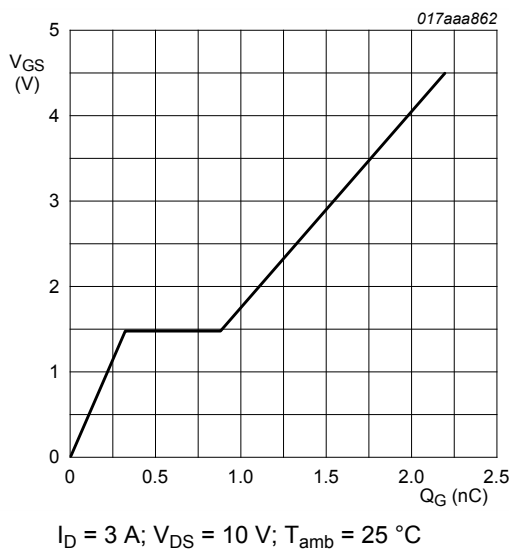


Fig. 14. Gate-source voltage as a function of gate charge; typical values

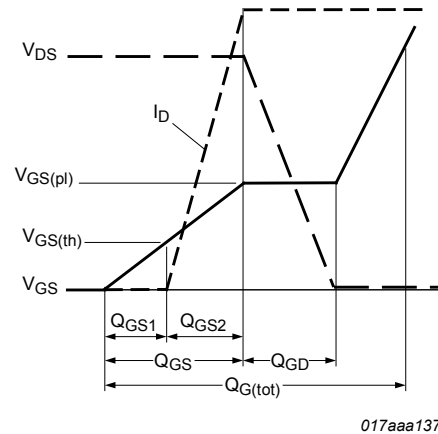
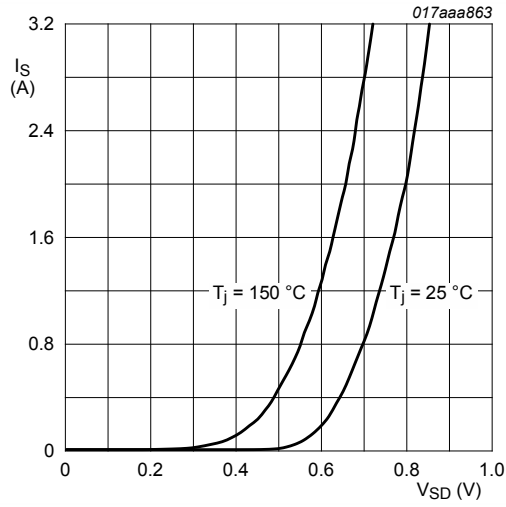


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

8. Test information

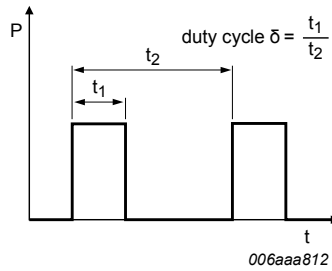


Fig. 17. Duty cycle definition

9. Package outline

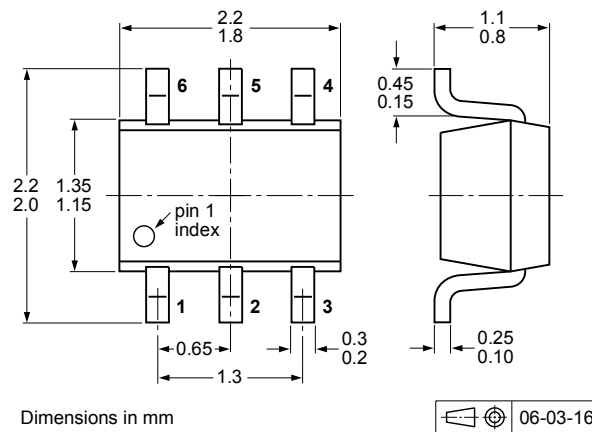


Fig. 18. Package outline TSSOP6 (SOT363)

10. Soldering

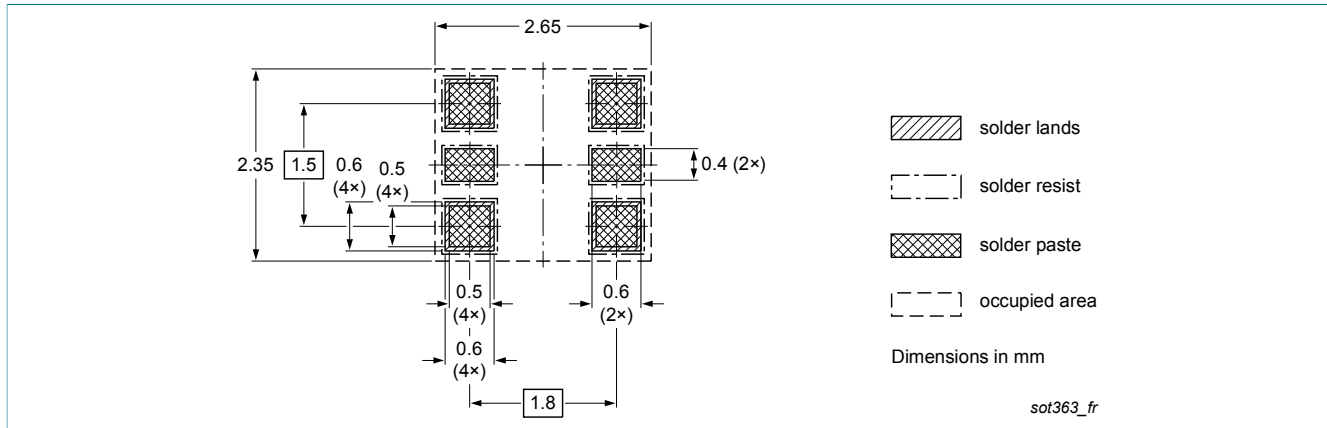


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

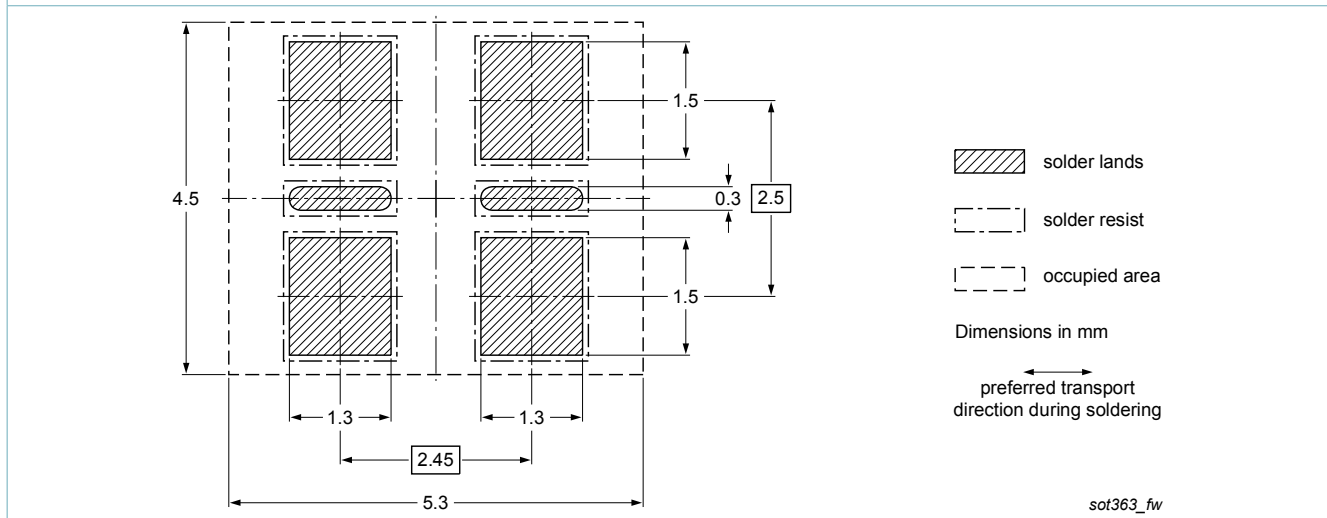


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMG45UN v.1	20121113	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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