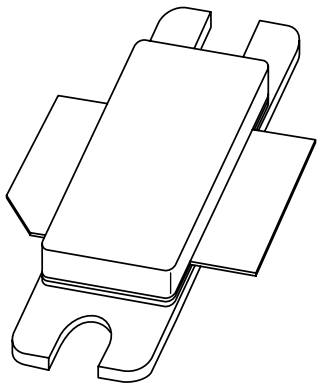


DATA SHEET



BLF1820-70 UHF power LDMOS transistor

Product specification
Supersedes data of 2001 Feb 12

2003 Feb 10

UHF power LDMOS transistor

BLF1820-70

FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 500 mA:
 - Output power = 65 W (PEP)
 - Gain = 12 dB
 - Efficiency = 32%
 - $dim = -26$ dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (1800 to 2000 MHz)
- Internally matched for ease of use.

APPLICATIONS

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the 1800 to 2000 MHz frequency range.

DESCRIPTION

70 W LDMOS power transistor for base station applications at frequencies from 1800 to 2000 MHz.

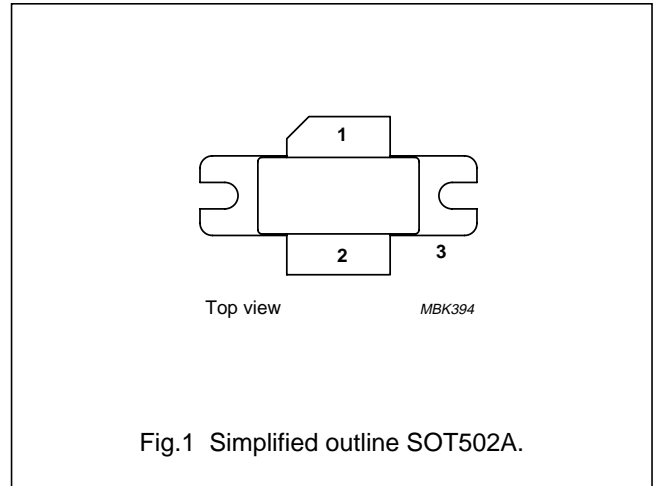
QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	$f_1 = 2000; f_2 = 2000.1$	26	65 (PEP)	>11	>30	≤ -25

PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange



CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	9	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_h = 25\text{ °C}$, note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions.

CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 1.4\text{ mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 140\text{ mA}$	4.4	–	5.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$	–	–	10	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	18	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0$	–	–	25	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 5\text{ A}$	–	4.2	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GSth} + 9\text{ V}$; $I_D = 5\text{ A}$	–	0.15	–	Ω
C_{rss}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$; $f = 1\text{ MHz}$	–	3.4	–	pF

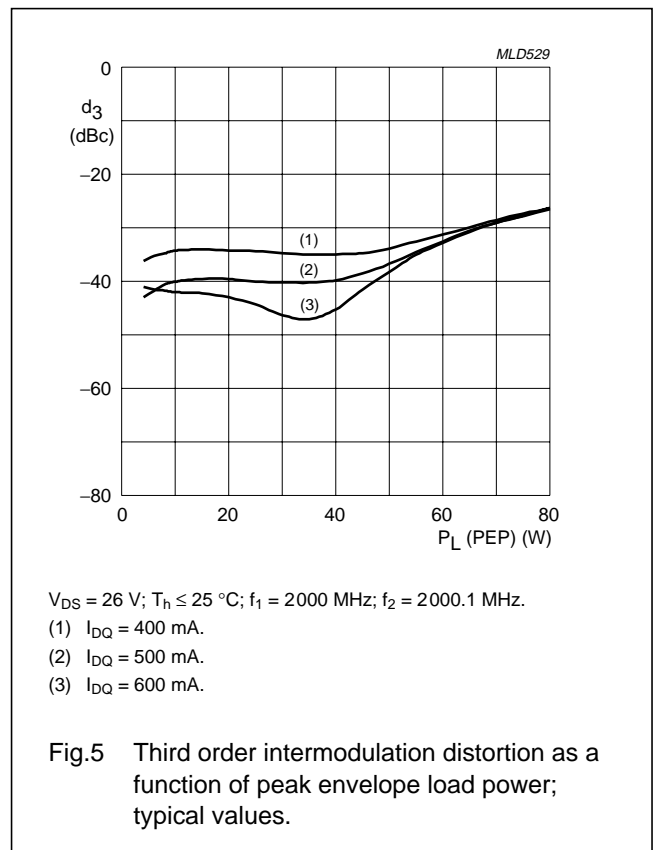
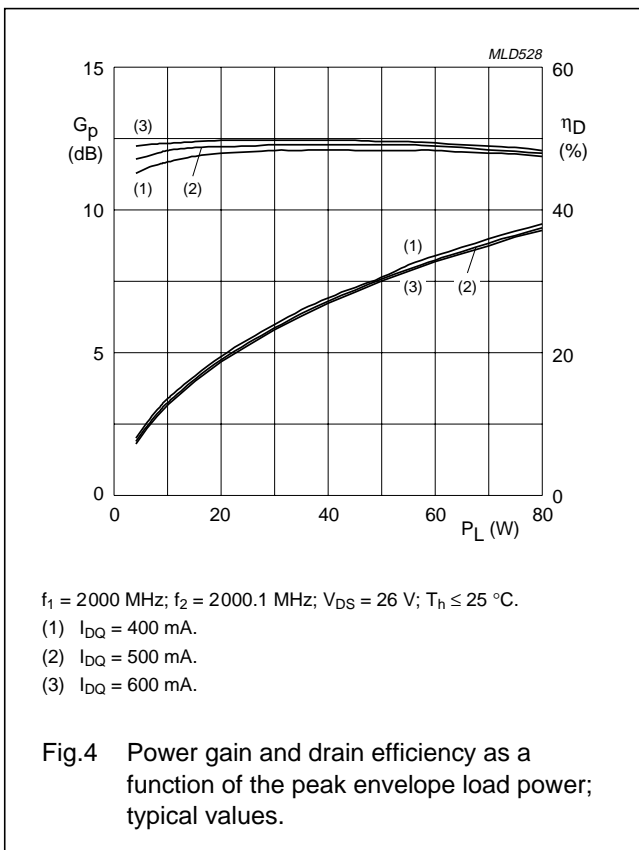
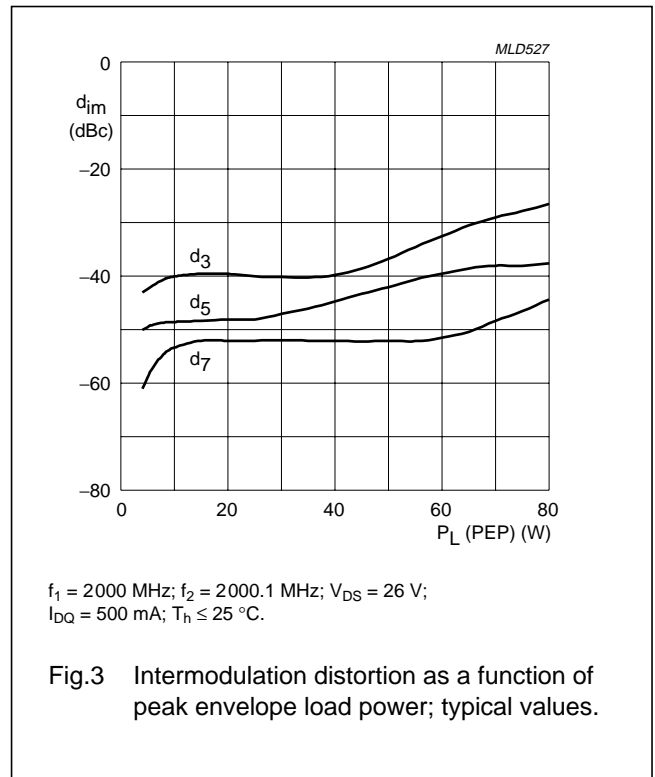
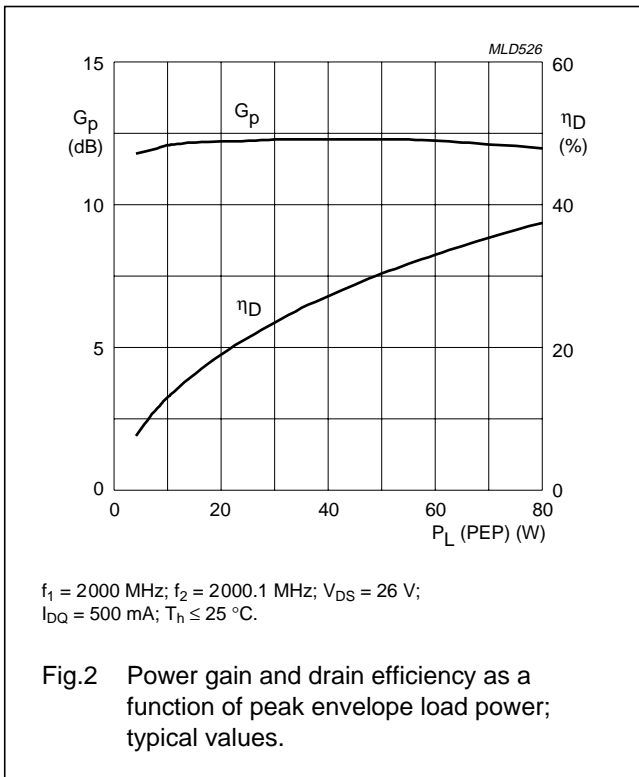
APPLICATION INFORMATIONRF performance in a common source class-AB circuit. $T_h = 25\text{ °C}$; $R_{th\ j-h} = 1.15\text{ K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	$f_1 = 2000$; $f_2 = 2000.1$	26	500	65 (PEP)	>11	>30	≤–25

Ruggedness in class-AB operationThe BLF1820-70 is capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 26\text{ V}$; $I_{DQ} = 500\text{ mA}$; $P_L = 65\text{ W}$; $f = 2000\text{ MHz}$.

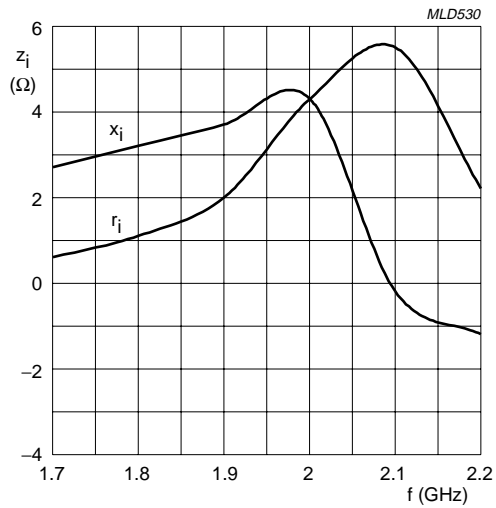
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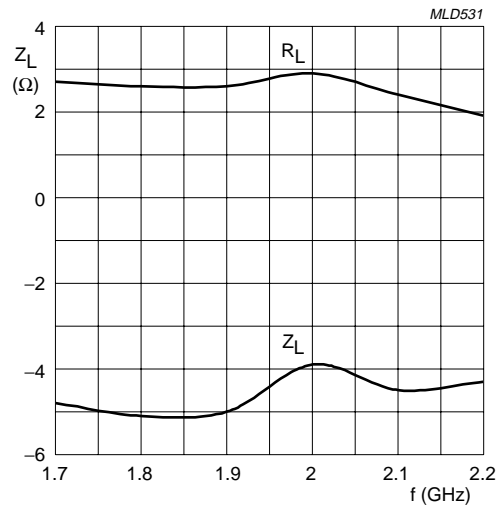
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$V_{DS} = 26\text{ V}$; $I_{DQ} = 500\text{ mA}$; $P_L = 65\text{ W}$; $T_n \leq 25\text{ }^\circ\text{C}$.

Fig.6 Input impedance as a function of frequency (series components); typical values.



$V_{DS} = 26\text{ V}$; $I_{DQ} = 500\text{ mA}$; $P_L = 65\text{ W}$; $T_n \leq 25\text{ }^\circ\text{C}$.

Fig.7 Load impedance as a function of frequency (series components); typical values.

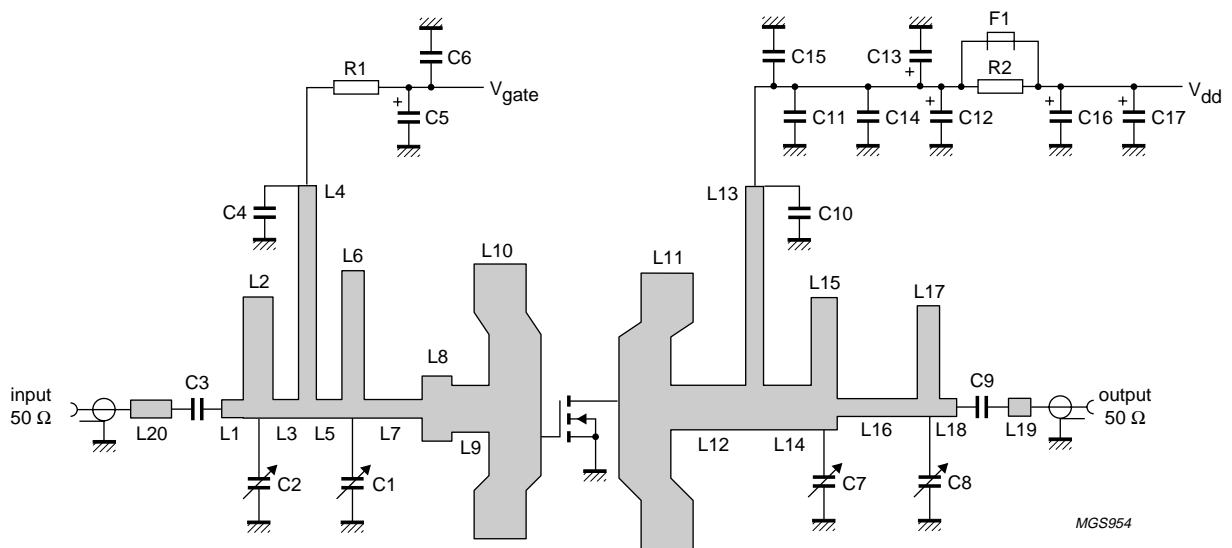


Fig.8 Class-AB test circuit at $f = 2\text{ GHz}$.

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List of components (see Figs. 8 and 9)

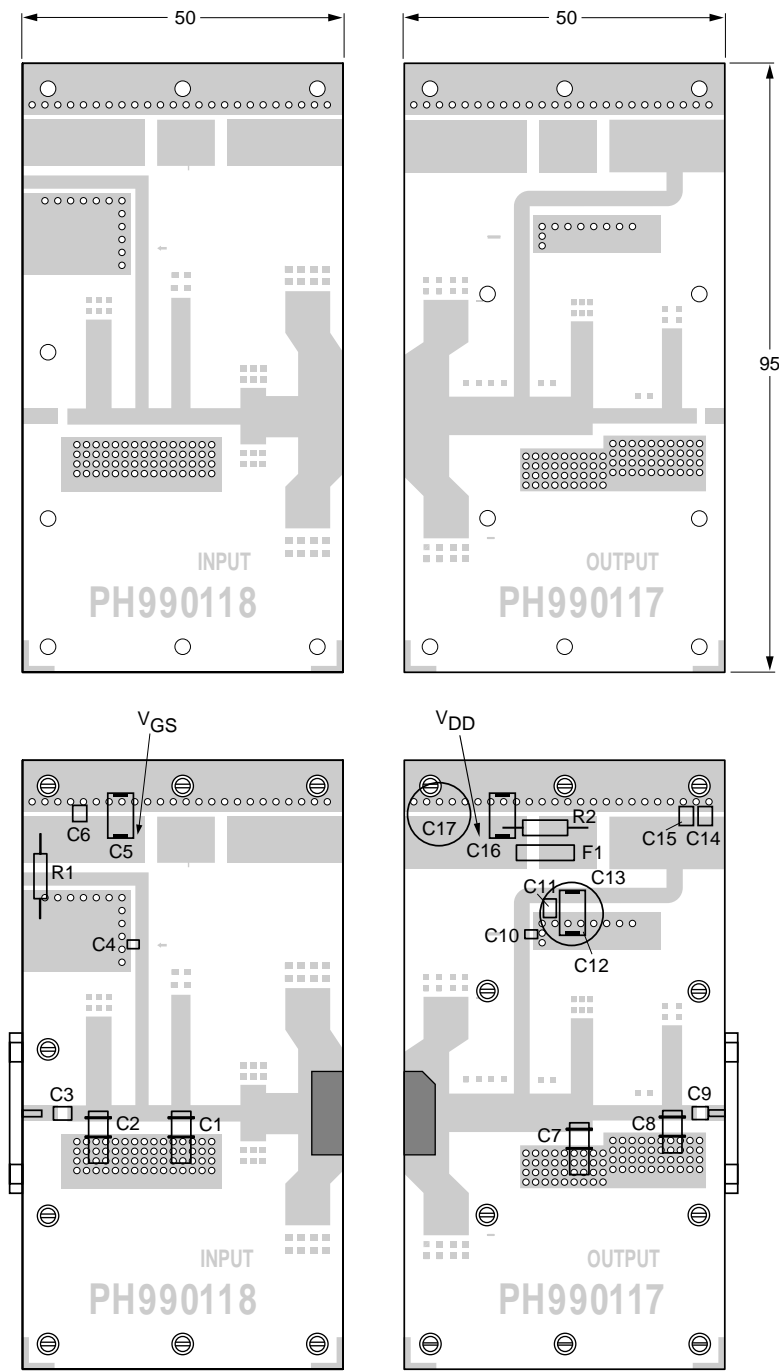
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7 and C8	Tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C3, C9	multilayer ceramic chip capacitor; note 1	12 pF		
C4, C10	multilayer ceramic chip capacitor; note 2	12 pF		
C5, C12 and C16	electrolytic capacitor	4.5 μ F; 50 V		
C6, C11 and C15	multilayer ceramic chip capacitor; note 1	1 nF		
C13 and C17	electrolytic capacitor	100 μ F; 63 V		2222 037 58101
C14	multilayer ceramic chip capacitor	100 nF		2222 581 16641
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	2.9 \times 2.4 mm	
L2		10.8 Ω	4 \times 16.3 mm	
L3		50 Ω	3.7 \times 2.4 mm	
L4		6 Ω	2 \times 30.8 mm	
L5		50 Ω	3.6 \times 2.4 mm	
L6		9 Ω	3 \times 19.9 mm	
L7		50 Ω	7.8 \times 2.4 mm	
L8		18.5 Ω	4 \times 8.8 mm	
L9		24.4 Ω	5 \times 6.3 mm	
L10 and L11		5.1 Ω	7 \times 37 mm	
L12		25.4 Ω	10.1 \times 6 mm	
L13		5.7 Ω	2.4 \times 32.8 mm	
L14		25.4 Ω	6.4 \times 6 mm	
L15		10 Ω	3.5 \times 17.8 mm	
L16		50 Ω	10.8 \times 2.4 mm	
L17		11.8 Ω	3 \times 14.9 mm	
L18		50 Ω	2.3 \times 2.4 mm	
L19		50 Ω	3 \times 2.4 mm	
L20		50 Ω	5.5 \times 2.4 mm	
R1 and R2		metal film resistor	10 Ω , 0.6 W	

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$); thickness 0.79 mm.

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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2 GHz class-AB test circuit.

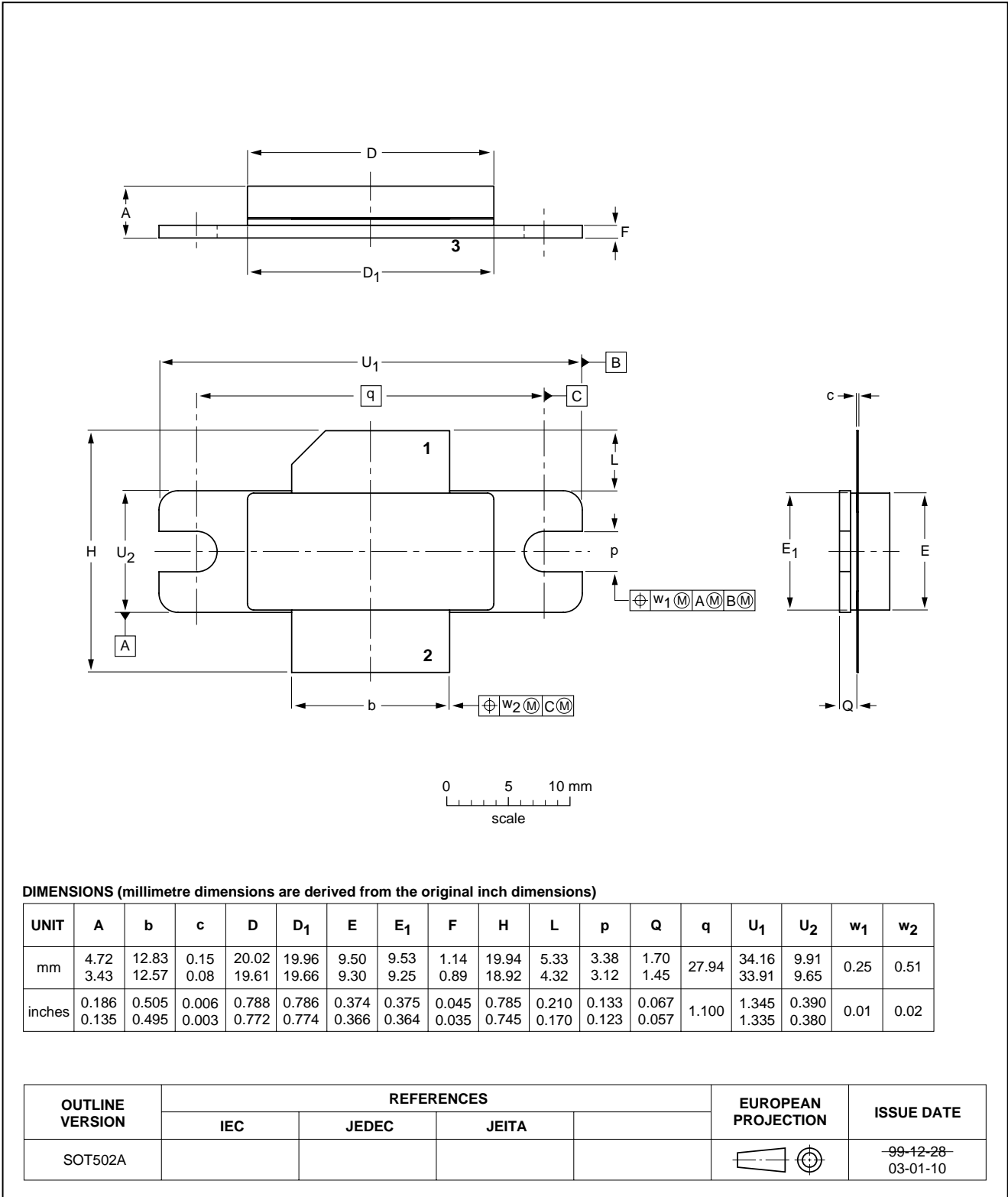
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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NOTES

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NOTES

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