Document Number: AFT18S230-12N
Rev. 0, 7/2015

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 50 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1880 MHz.

1800 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 50 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

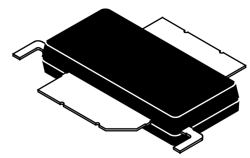
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	17.1	33.3	7.1	–33.6	–14
1840 MHz	17.5	33.3	7.1	–33.6	–16
1880 MHz	17.6	33.8	6.9	–33.7	–11

Features

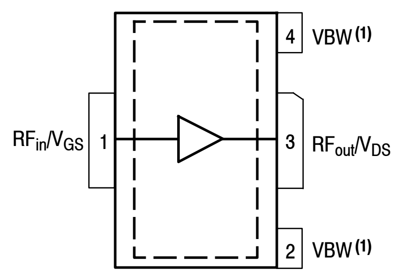
- High thermal conductivity packaging technology for reduced thermal resistance
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems
- Optimized for Doherty applications

AFT18S230-12NR3

1805–1880 MHz, 50 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-780-2L2L PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 2 and pin 4.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 50 W CW, 28 Vdc, I_{DQ} = 1400 mA, 1842.5 MHz	$R_{\theta JC}$	0.27	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 291 μAdc)	$V_{GS(th)}$	1.0	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1400 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.3	2.8	3.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.9 Adc)	$V_{DS(on)}$	0.1	0.24	0.3	Vdc

Functional Tests [4] (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 50 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Power Gain	G_{ps}	16.3	17.6	19.3	dB
Drain Efficiency	η_D	29.0	33.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.0	6.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	–33.7	–30.0	dBc
Input Return Loss	IRL	—	–11	–6	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Part internally matched both on input and output.

(continued)

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Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1400 mA, f = 1840 MHz					
VSWR 10:1 at 32 Vdc, 309 W CW Output Power (3 dB Input Overdrive from 204 W CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	204	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz bandwidth)	Φ	—	–17	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 50 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.009	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
AFT18S230-12NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-2L2L

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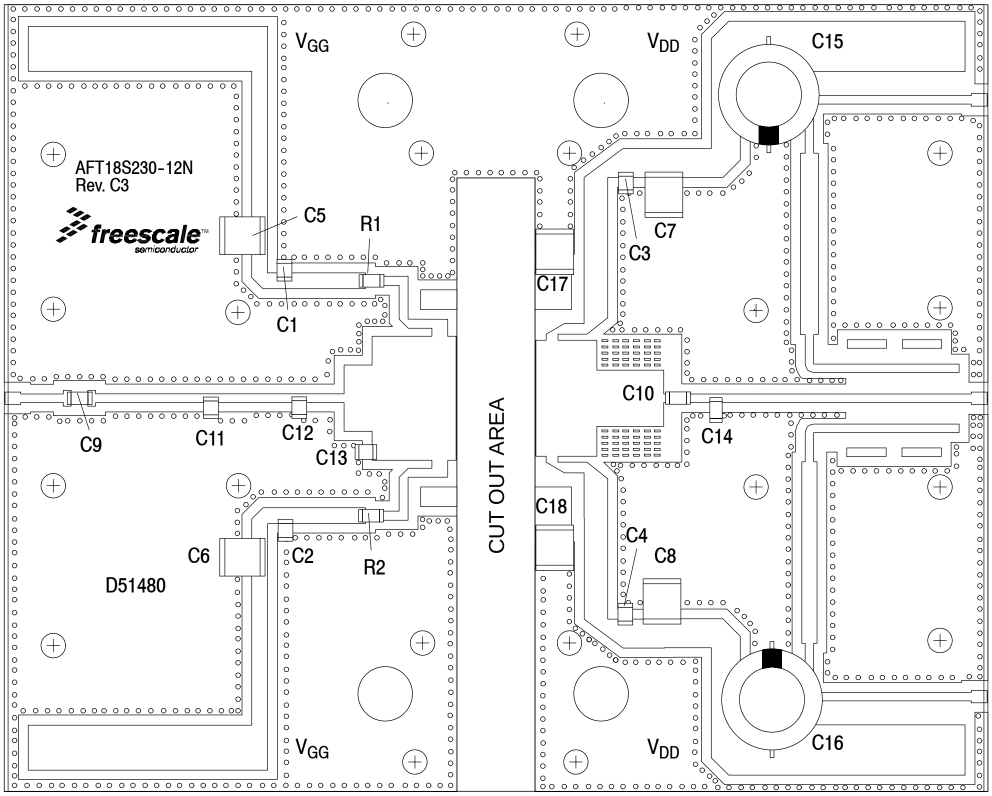

Figure 2. AFT18S230-12NR3 Test Circuit Component Layout

Table 7. AFT18S230-12NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C9	12 pF Chip Capacitors	ATC100B120FW1500XT	ATC
C5, C6, C7, C8, C17, C18	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C10	6.8 pF Chip Capacitor	ATC100B6R8BW1500XT	ATC
C11	1.1 pF Chip Capacitor	ATC100B1R1BW1500XT	ATC
C12	1.0 pF Chip Capacitor	ATC100B1R0BW1500XT	ATC
C13	0.4 pF Chip Capacitor	ATC100B0R4BW1500XT	ATC
C14	0.9 pF Chip Capacitor	ATC100B0R9BW1500XT	ATC
C15, C16	470 μF, 50 V Electrolytic Capacitors	477CKS050M	Illinois Capacitor
R1, R2	4.02 Ω, 1/4 W Chip Resistors	CRCW12064R02FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D51480	MTL

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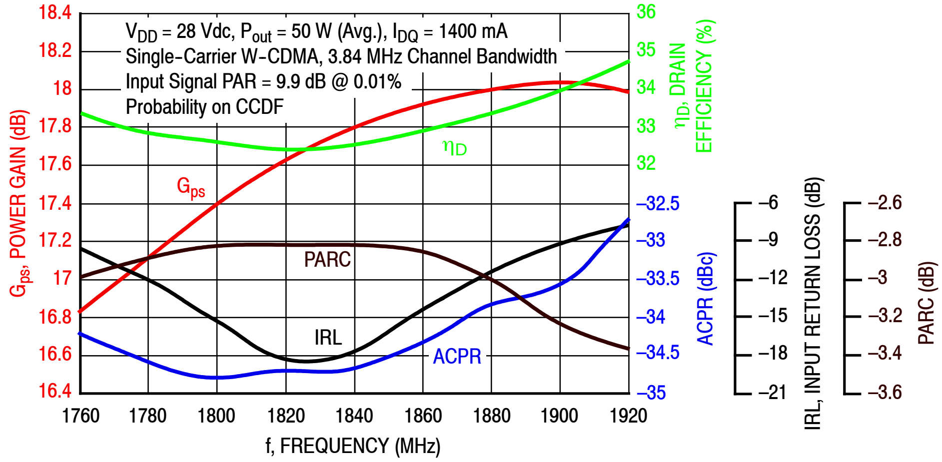

Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

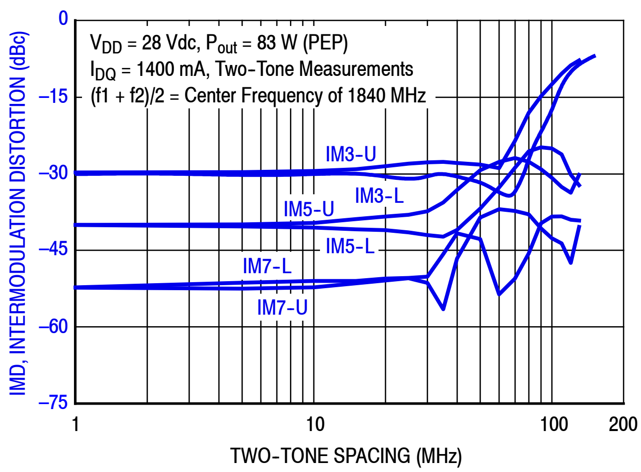

Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

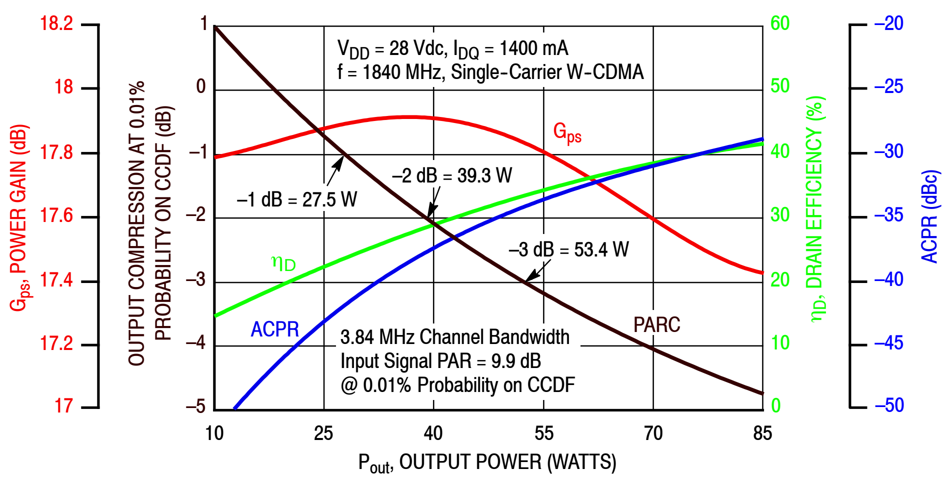

Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

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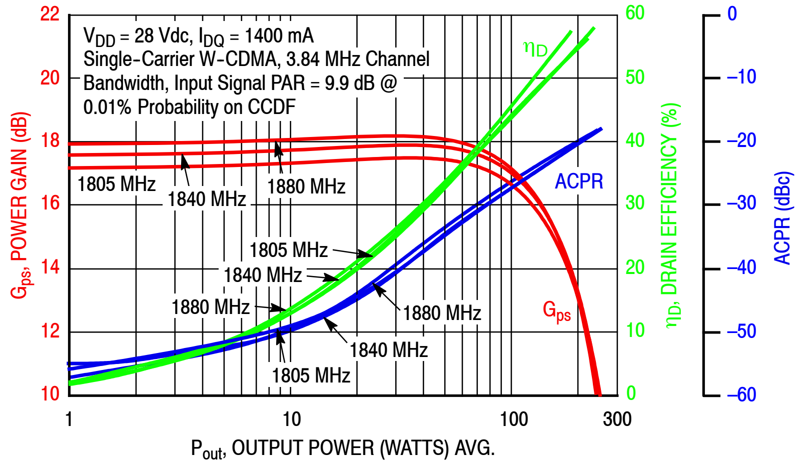

Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

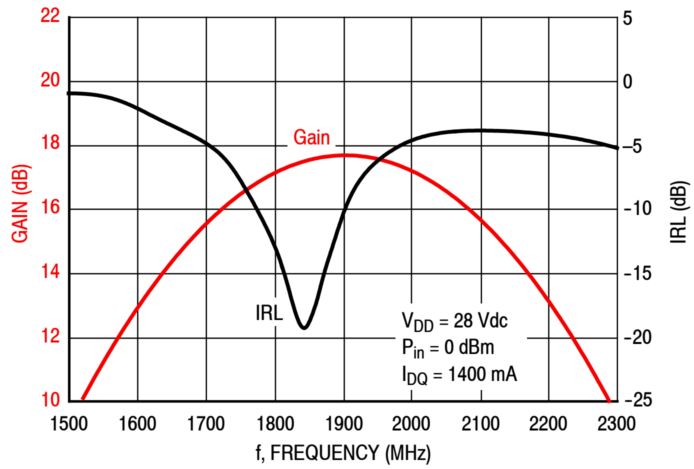

Figure 7. Broadband Frequency Response

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Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB					
			Z_{load} [(1)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.17 – j4.25	1.10 + j3.92	1.10 – j3.55	16.8	54.0	250	53.4	–12
1840	1.69 – j4.78	1.38 + j4.25	1.06 – j3.65	16.7	54.0	253	53.5	–13
1880	3.16 – j5.35	2.16 + j4.57	1.09 – j3.92	16.5	54.0	250	52.4	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB					
			Z_{load} [(2)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.17 – j4.25	1.07 + j4.03	1.10 – j3.61	14.7	54.7	298	55.8	–18
1840	1.69 – j4.78	1.39 + j4.39	1.13 – j3.80	14.6	54.8	299	56.1	–18
1880	3.16 – j5.35	2.25 + j4.78	1.16 – j4.07	14.3	54.7	296	54.3	–18

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

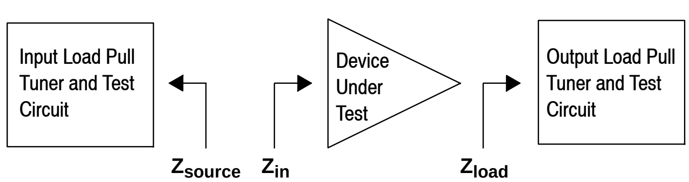
Table 9. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB					
			Z_{load} [(1)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.17 – j4.25	1.12 + j4.11	1.95 – j2.42	19.5	52.3	171	64.8	–19
1840	1.69 – j4.78	1.48 + j4.43	1.88 – j2.54	19.3	52.2	168	64.6	–20
1880	3.16 – j5.35	2.41 + j4.75	1.77 – j2.67	19.1	52.2	164	64.1	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB					
			Z_{load} [(2)] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	1.17 – j4.25	1.08 + j4.14	1.80 – j2.54	17.3	53.2	211	67.0	–26
1840	1.69 – j4.78	1.42 + j4.52	1.69 – j2.54	17.3	52.9	197	66.5	–28
1880	3.16 – j5.35	2.40 + j4.89	1.73 – j2.72	17.1	52.9	193	65.4	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



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P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

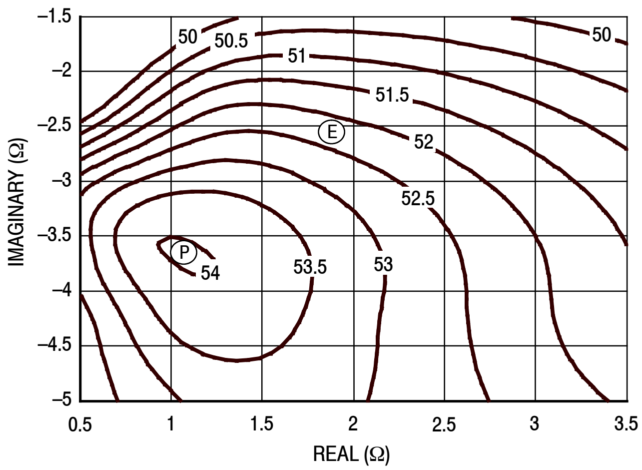

Figure 8. P1dB Load Pull Output Power Contours (dBm)

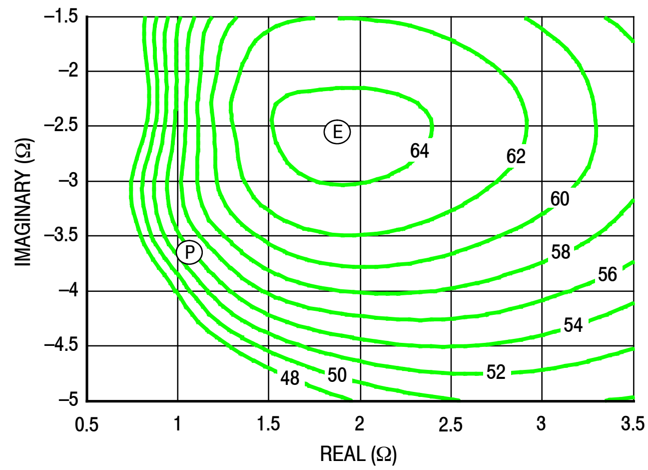

Figure 9. P1dB Load Pull Efficiency Contours (%)

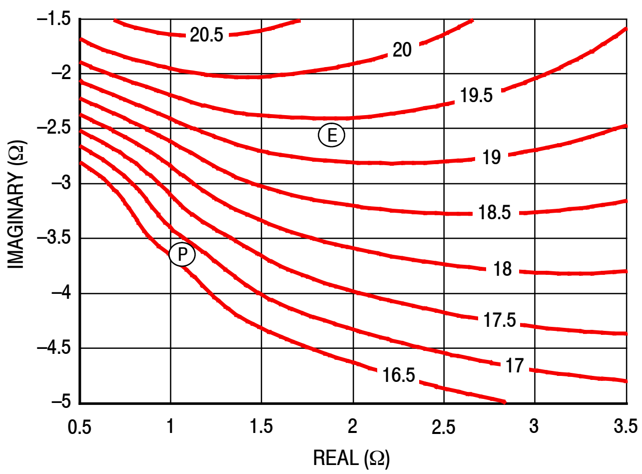

Figure 10. P1dB Load Pull Gain Contours (dB)

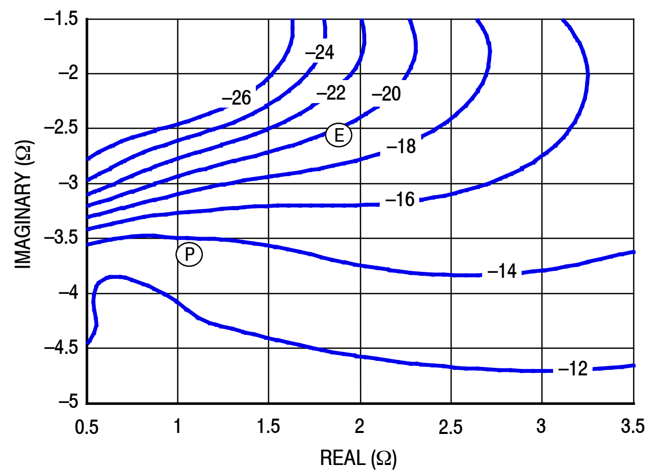

Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

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P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

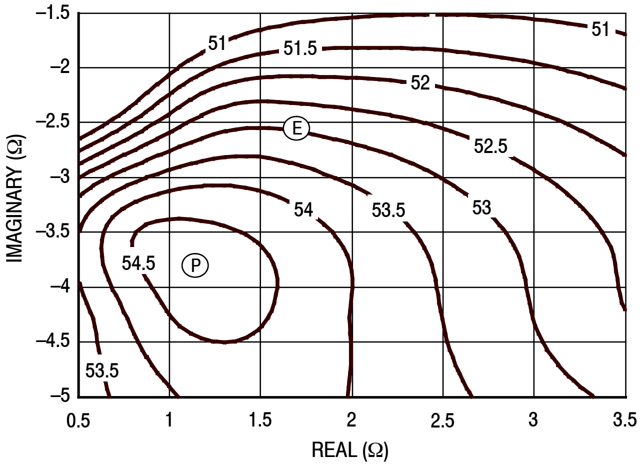

Figure 12. P3dB Load Pull Output Power Contours (dBm)

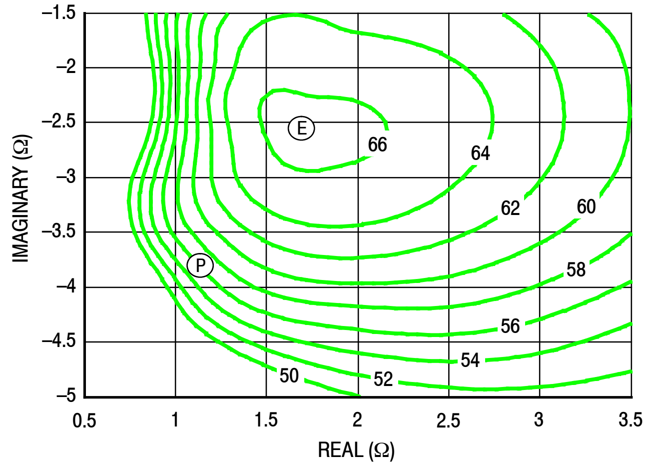

Figure 13. P3dB Load Pull Efficiency Contours (%)

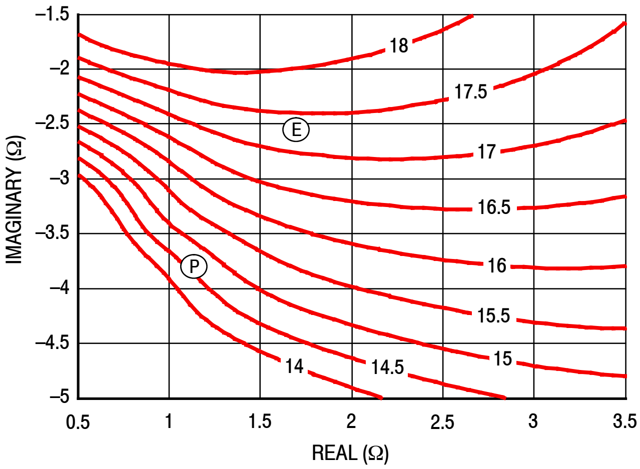

Figure 14. P3dB Load Pull Gain Contours (dB)

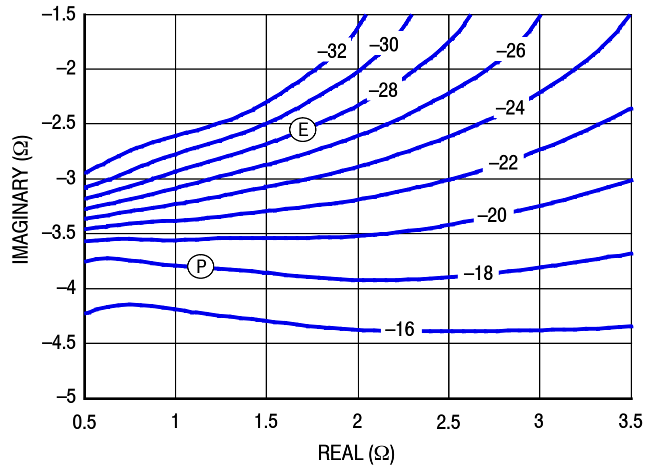

Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

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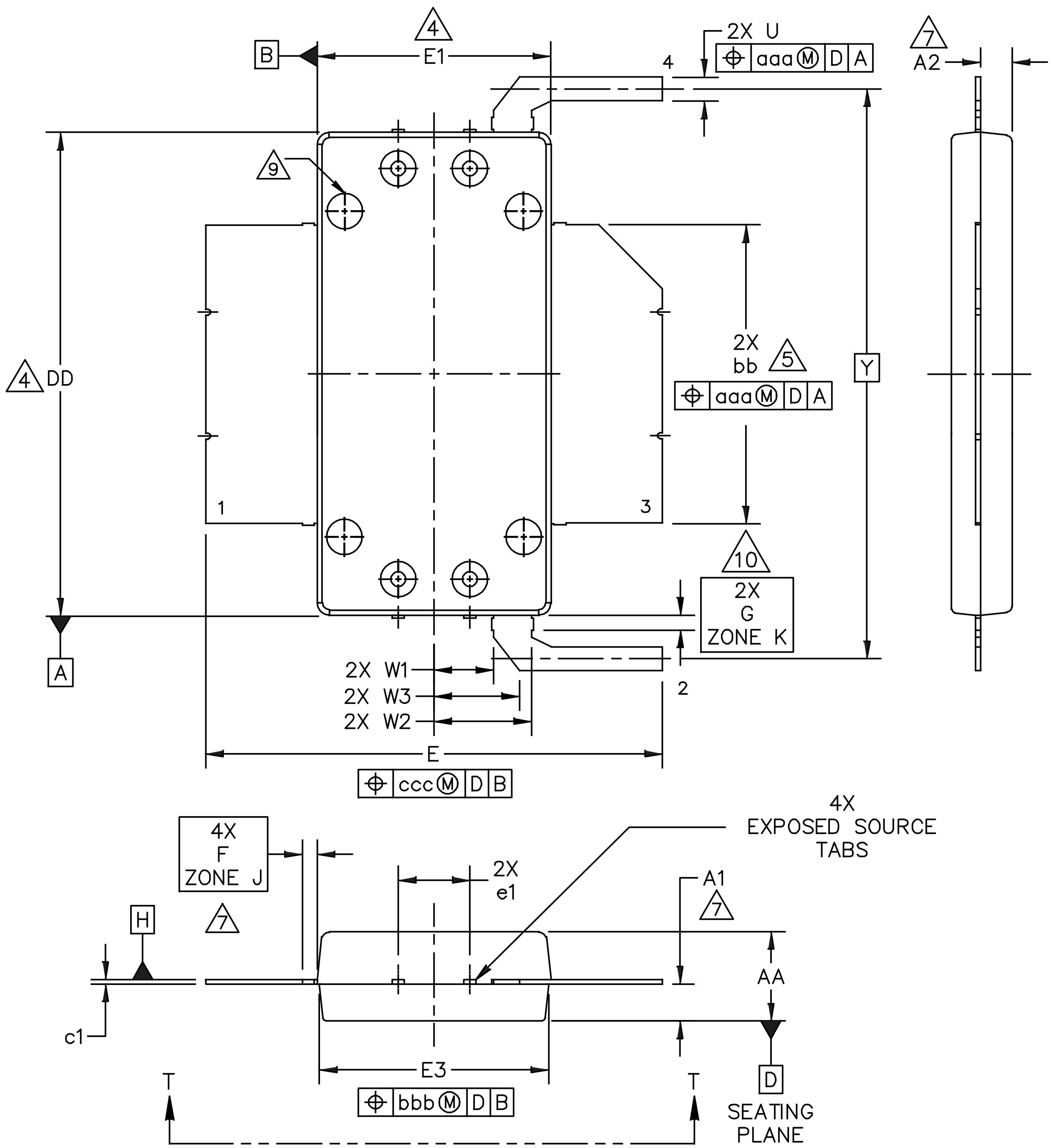

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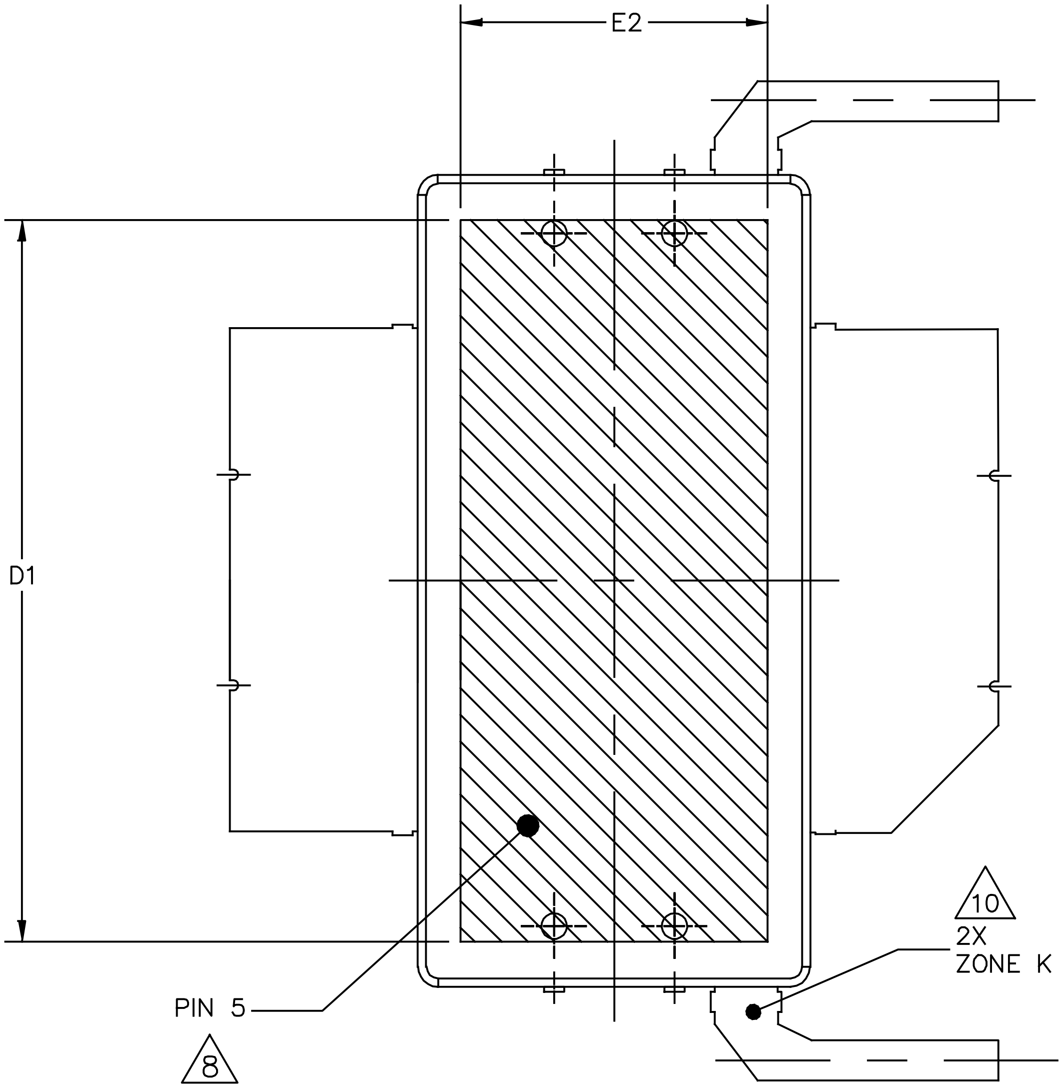

BOTTOM VIEW
VIEW T–T

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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1 AND 3. A2 APPLIES TO PINS 2 AND 4. TOLERANCES OF DIMENSIONS A1 AND A2 ARE TENTATIVE.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	W1	.095	.105	2.41	2.67
A1	.059	.065	1.50	1.65	W2	.158	.168	4.01	4.27
A2	.056	.068	1.42	1.73	W3	.138	.148	3.51	3.76
DD	.808	.812	20.52	20.62	U	.037	.043	0.94	1.09
D1	.720	----	18.29	----	Y	.956 BSC		24.28 BSC	
E	.762	.770	19.35	19.56	bb	.497	.503	12.62	12.78
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e1	.116	.124	2.95	3.15
E3	.383	.387	9.73	9.83	aaa	.004		0.10	
F	.025 BSC		0.64 BSC		bbb	.006		0.15	
G	.030 BSC		0.76 BSC		ccc	.010		0.25	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2015	• Initial Release of Data Sheet

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