BLF2043

UHF power LDMOS transistor

Rev. 7 — 1 September 2015

AMPLEON

Product data sheet

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In data sheets, where the previous Philips references is mentioned, please use the new links as shown below.

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Thank you for your cooperation and understanding,

Ampleon

UHF power LDMOS transistor BLF2043

FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 85 mA:
  - Output power = 10 W (PEP)
  - Gain = 12 dB
  - Efficiency = 36.5%
  - dim = –32 dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (HF to 2200 MHz)
- No internal matching for broadband operation.

APPLICATIONS

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the HF to 2200 MHz frequency range
- Broadcast drivers.

DESCRIPTION

10 W LDMOS power transistor for base station applications at frequencies from HF to 2200 MHz.

PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to mounting base

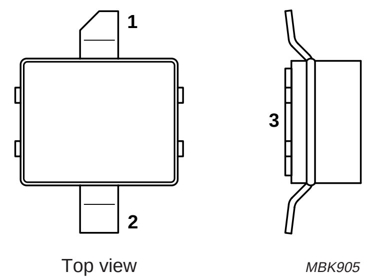


Fig.1 Simplified outline.

QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 2000; f_2 = 2000.1	26	10 (PEP)	12.5	36.5	–32

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	2.2	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_{mb} = 25 °C; note 1	9	K/W

Note

1. Thermal resistance is determined under RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.2 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 20 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	1.5	μA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	2.8	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	40	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.75 A	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.75 A	–	1.2	–	Ω
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	11	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	9	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	0.5	–	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 2000; f_2 = 2000.1	26	85	10 (PEP)	>11.8	>33	≤–26

Ruggedness in class-AB operation

The BLF2043 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 2000 MHz at rated load power.

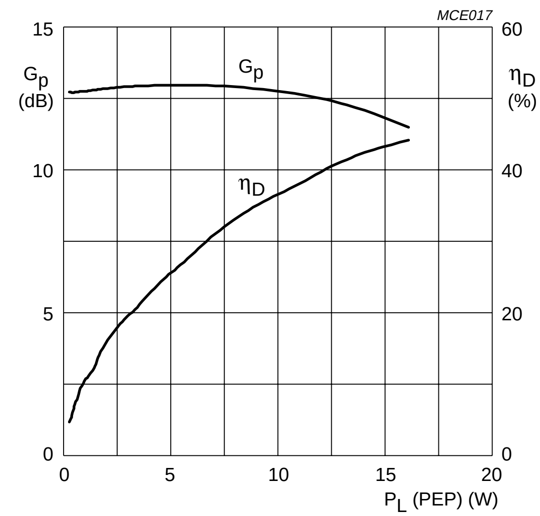


Fig.2 Power gain and efficiency as functions of peak envelope load power; typical values.

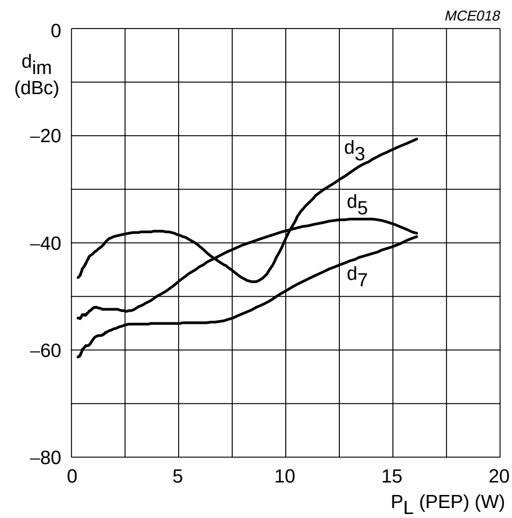
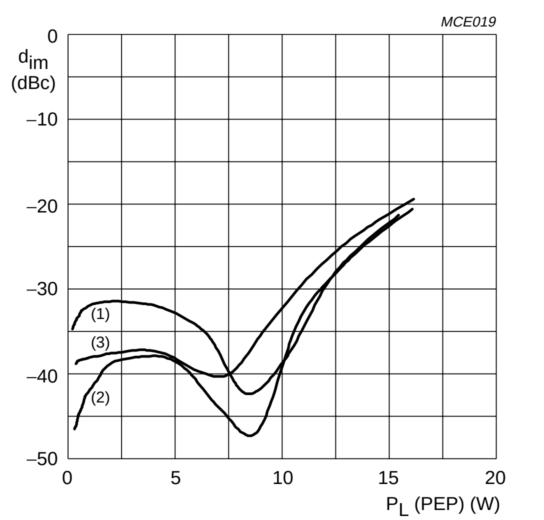
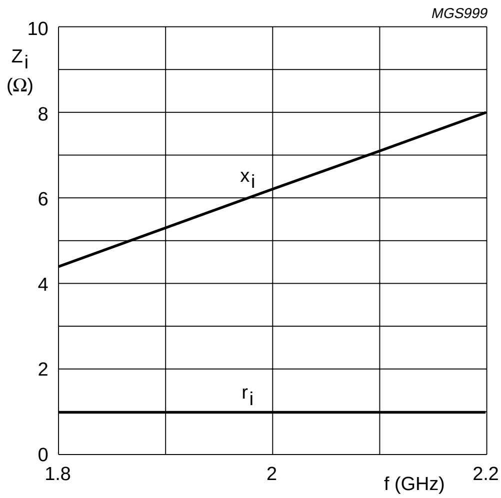


Fig.3 Intermodulation distortion as a function of peak envelope load power; typical values.



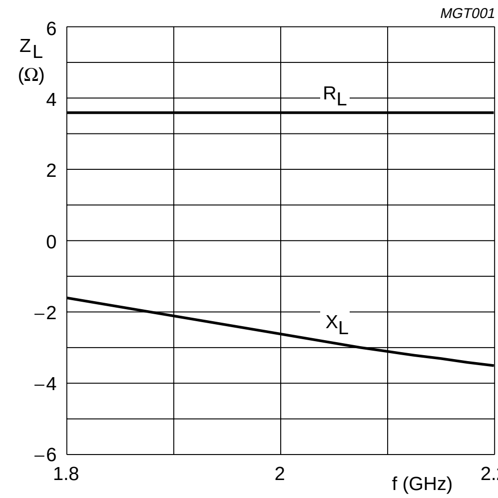
(1) I_{DQ} = 55 mA.
(2) I_{DQ} = 85 mA.
(3) I_{DQ} = 115 mA.

Fig.4 Third order intermodulation distortion as a function of peak envelope load power and I_{DQ} setting; typical values.



V_{DS} = 26 V; I_{DQ} = 25 mA; P_L = 10 W; $T_h \leq 25$ °C.
Impedance measured at reference planes (see Fig.7).

Fig.5 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 25 mA; P_L = 10 W; $T_h \leq 25$ °C.
Impedance measured at reference planes (see Fig.7).

Fig.6 Load impedance as a function of frequency (series components); typical values.

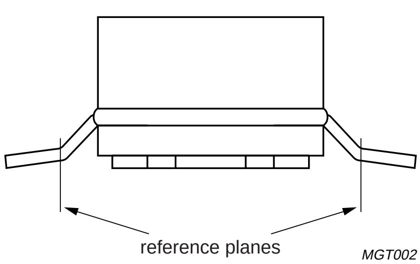


Fig.7 Measuring reference planes SOT538A.

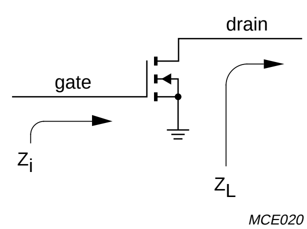


Fig.8 Definition of transistor impedance.

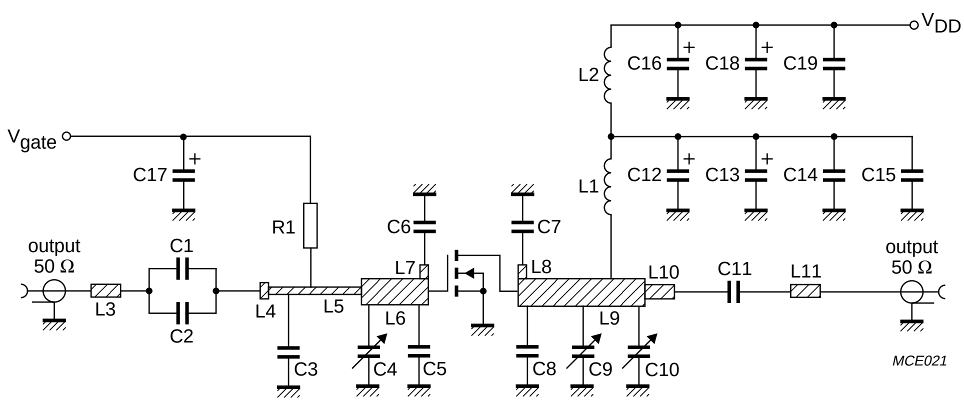


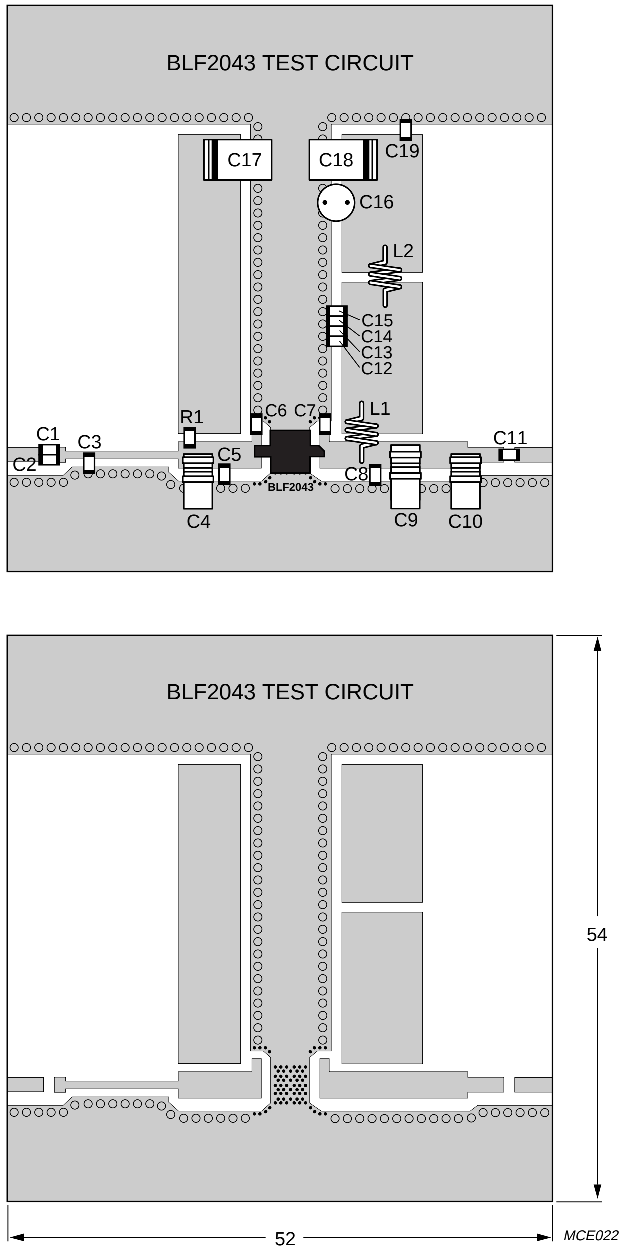
Fig.9 Class-AB test circuit for 2 GHz.

List of components (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	6.8 pF		
C3	multilayer ceramic chip capacitor; note 1	1.0 pF		
C4, C10, C11	tekelec variable capacitor; type 37271	0.6 to 4.5 pF		
C5, C7	multilayer ceramic chip capacitor; note 1	2.0 pF		
C6	multilayer ceramic chip capacitor; note 1	2.7 pF		
C8	multilayer ceramic chip capacitor; note 1	0.2 pF		
C9	multilayer ceramic chip capacitor; note 1	0.6 to 4.5 pF		
C12	multilayer ceramic chip capacitor; note 1	10 pF		
C13	multilayer ceramic chip capacitor; note 1	51 pF		
C14	multilayer ceramic chip capacitor; note 1	120 pF		
C15	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C16	electrolytic capacitor	100 μF; 63 V		2222 037 58101
C17, C18	tantalum SMD capacitor	10 μF; 35 V		
C19	multilayer ceramic chip capacitor; note 2	1 nF		
L1, L2	3 turns enamelled 0.5 mm copper wire		3 loops; d = 3 mm length = 3 mm	
L3	stripline; note 3	50 Ω	3.5 × 1.5 mm	
L4	stripline; note 3	50 Ω	1.0 × 1.5 mm	
L5	stripline; note 3	73.2 Ω	5 × 2 mm	
L6	stripline; note 3	31 Ω	11.0 × 0.8 mm	
L7, L8	stripline; note 3	64.7 Ω	1.5 × 1.0 mm	
L9	stripline; note 3	31 Ω	14.4 × 3.0 mm	
L10, L11	stripline; note 3	50 Ω	3.5 × 1.5 mm	
R1	metal film resistor	2.2 kΩ; 0.6 W		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Rogers 5880 dielectric (ε_r = 2.2); thickness 0.51 mm.



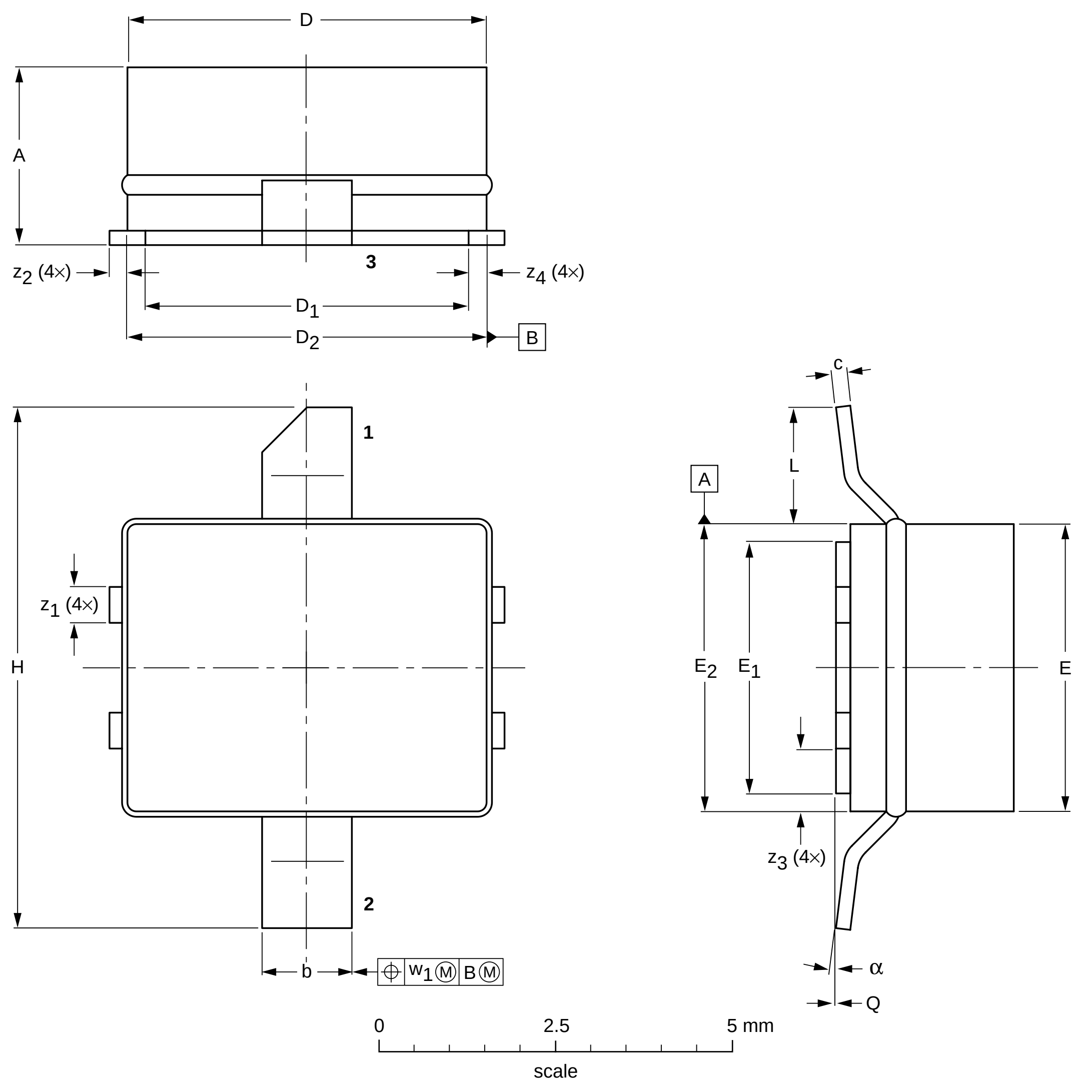
Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.51 mm.

Fig.10 Component layout for 2 GHz class-AB test circuit.

PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads **SOT538A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	Q	w_1	z_1	z_2	z_3	z_4	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.16 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	0.58 0.43	0.25 0.18	0.97 0.81	0.51 0.00	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.203 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	0.023 0.017	0.010 0.007	0.038 0.032	0.020 0.000	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT538A						~~00-03-03~~ 02-08-20

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SCA75

Printed in The Netherlands 613524/06/pp12 Date of release: 2003 Feb 10 Document order number: 9397 750 10917

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