



# PESD15VS2UAT-Q

Double ESD protection diode

10 June 2022

Product data sheet

## 1. General description

Unidirectional double ESD protection diode in common cathode configuration in a small SOT23 Surface-Mounted Device (SMD) plastic package, designed to protect up to two data lines against damage from ElectroStatic Discharge (ESD) and other transients.

## 2. Features and benefits

- Unidirectional ESD protection of up to two lines
- Common-cathode configuration
- Max. peak pulse power:  $P_{PPM} = 160 \text{ W}$  at  $t_p = 8/20 \mu\text{s}$
- Ultra-low reverse leakage current:  $I_{RM} = 1 \text{ nA}$
- ESD protection: 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge);  $I_{PP} = 5 \text{ A}$  at  $t_p = 8/20 \mu\text{s}$
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- Computers and peripherals
- Communication systems
- Audio and video equipment
- Data lines
- CAN bus protection

## 4. Quick reference data

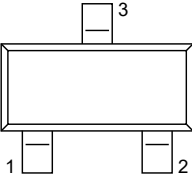
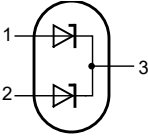
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage	$T_j = 25^\circ\text{C}$	[1]	-	-	15	V
$C_d$	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_j = 25^\circ\text{C}$	[1]	-	32	70	pF

[1] Measured across either pins 1 and 3 or pins 2 and 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A1	anode (diode 1)	 SOT23	 sym002
2	A2	anode (diode 2)		
3	CC	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD15VS2UAT-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD15VS2UAT-Q	% 7D

[1] % = placeholder for manufacturing site code

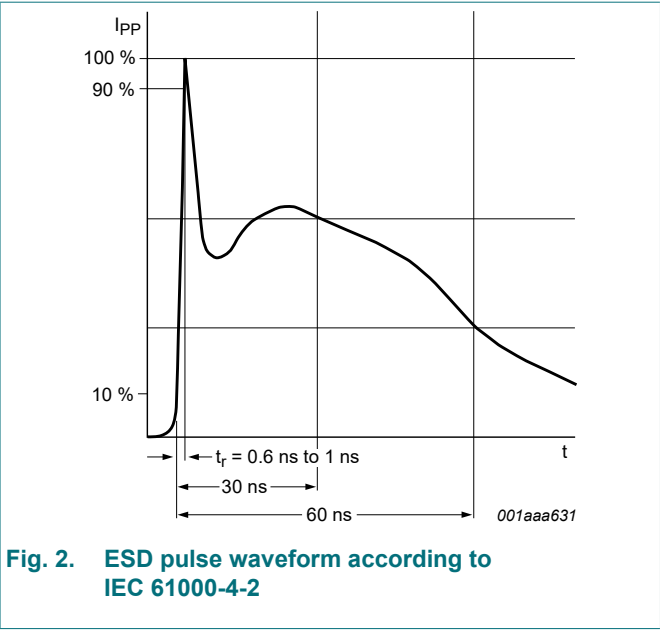
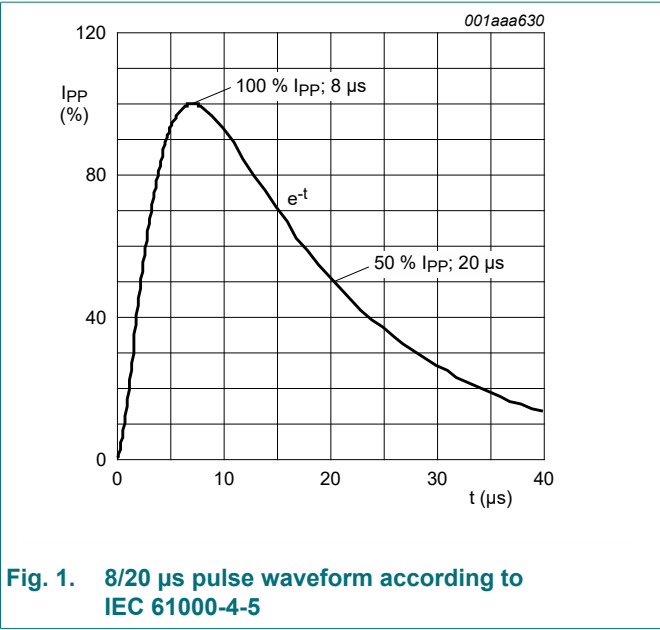
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>PPM</sub>	rated peak pulse power	t <sub>p</sub> = 8/20 μs	[1] [2]	-	160	W
I <sub>PPM</sub>	rated peak pulse current		[1] [2]	-	5	A
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
ESD maximum ratings						
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[3] [2]	-	30	kV
		IEC 61000-4-2; air discharge		-	15	kV
		MIL-STD-883; human body model (HBM)	[3] [2]	-	10	kV

- [1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.  
[2] Measured across either pins 1 and 3 or pins 2 and 3.  
[3] Device stressed with ten non-repetitive ESD pulses.

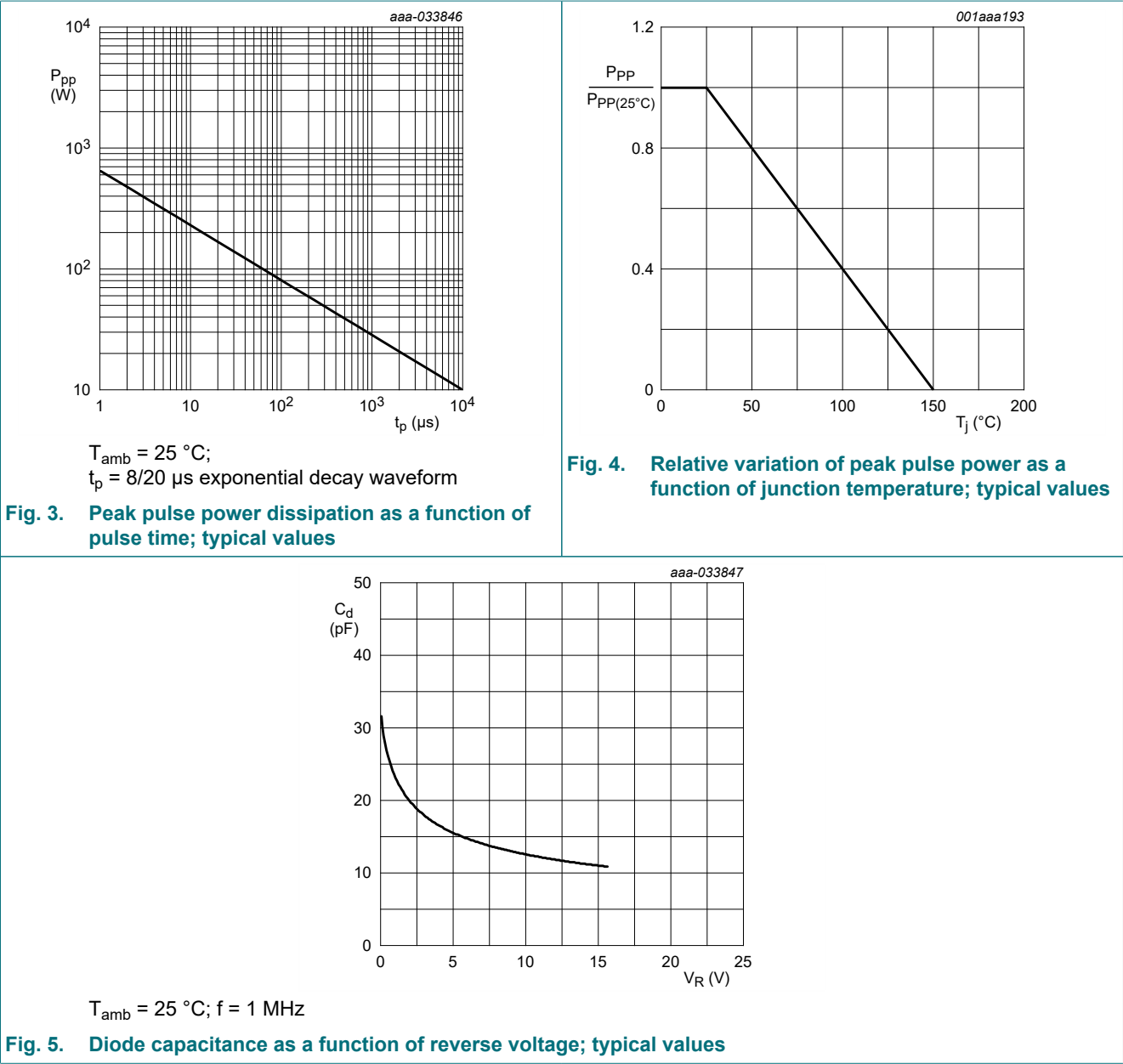


9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage	$T_j = 25\text{ }^{\circ}\text{C}$	[1]	-	-	15	V
$V_{BR}$	breakdown voltage	$I_R = 5\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$	[1]	17.6	18	18.4	V
$I_{RM}$	reverse leakage current	$V_{RWM} = 15\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	[1]	-	1	50	nA
$C_d$	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	[1]	-	32	70	pF
$V_{CL}$	clamping voltage	$I_{PP} = 1\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	[2] [1]	-	-	23	V
		$I_{PPM} = 5\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	[2] [1]	-	-	40	V
$R_{diff}$	differential resistance	$I_R = 1\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$	[1]	-	-	225	$\Omega$

- [1] Measured across either pins 1 and 3 or pins 2 and 3.  
[2] Non-repetitive current pulse 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.



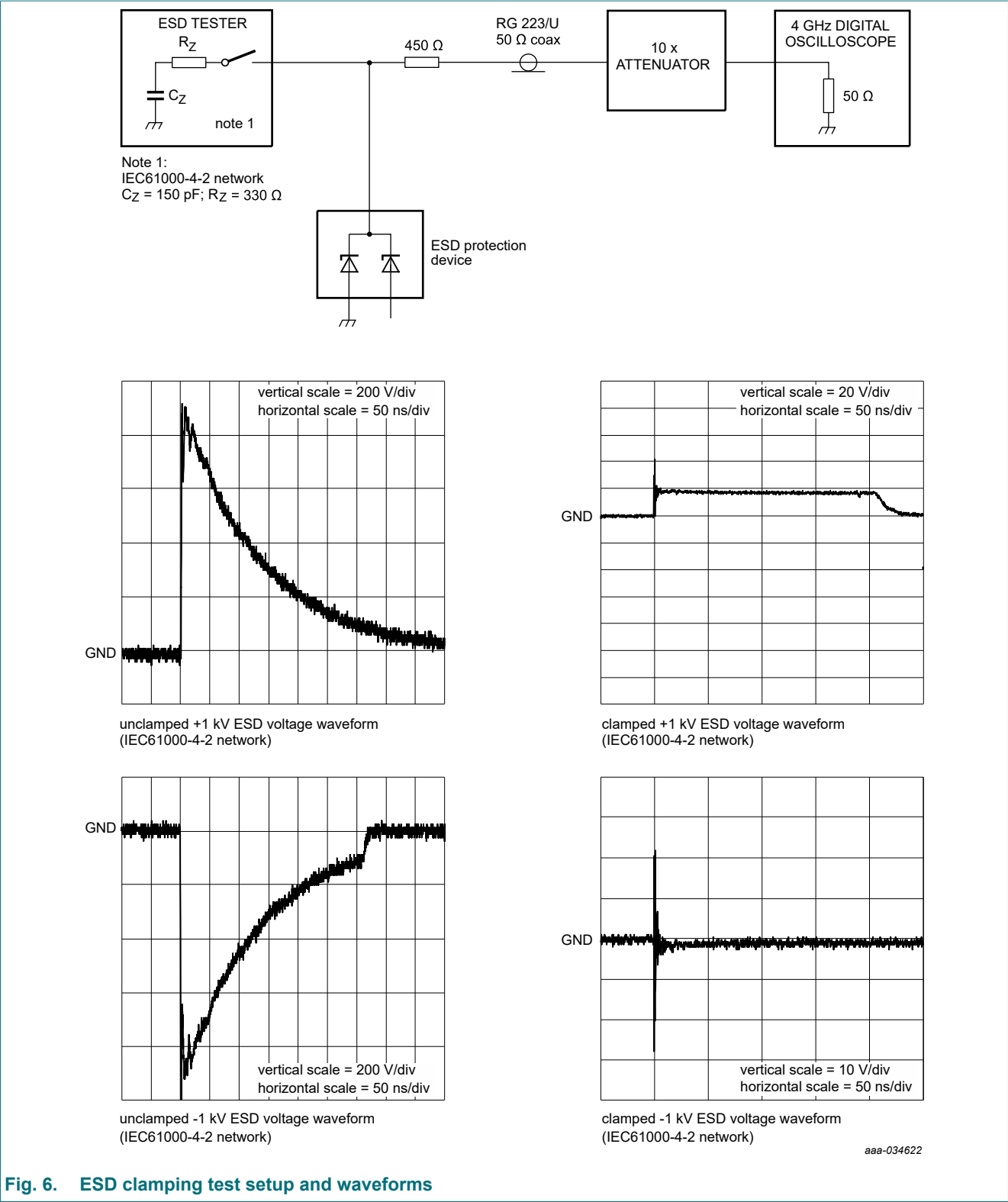


Fig. 6. ESD clamping test setup and waveforms

## 10. Application information

The device can protect up to two lines against damage caused by unidirectional ElectroStatic Discharge (ESD) and surge pulses. The device can protect lines whose signal polarities are below ground.

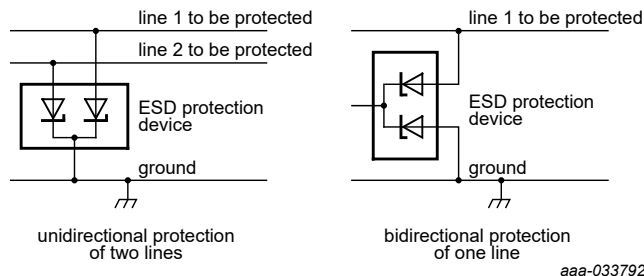


Fig. 7. Typical application: ESD protection of data lines

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.



13. Soldering

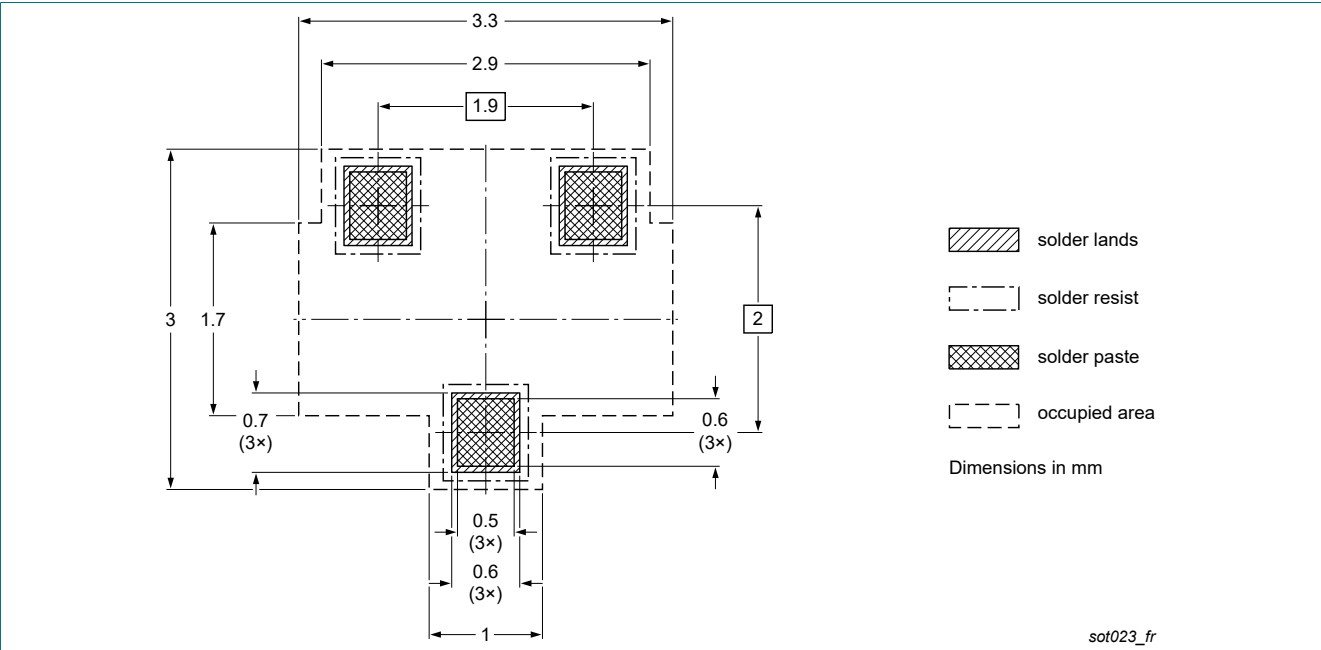


Fig. 9. Reflow soldering footprint for SOT23

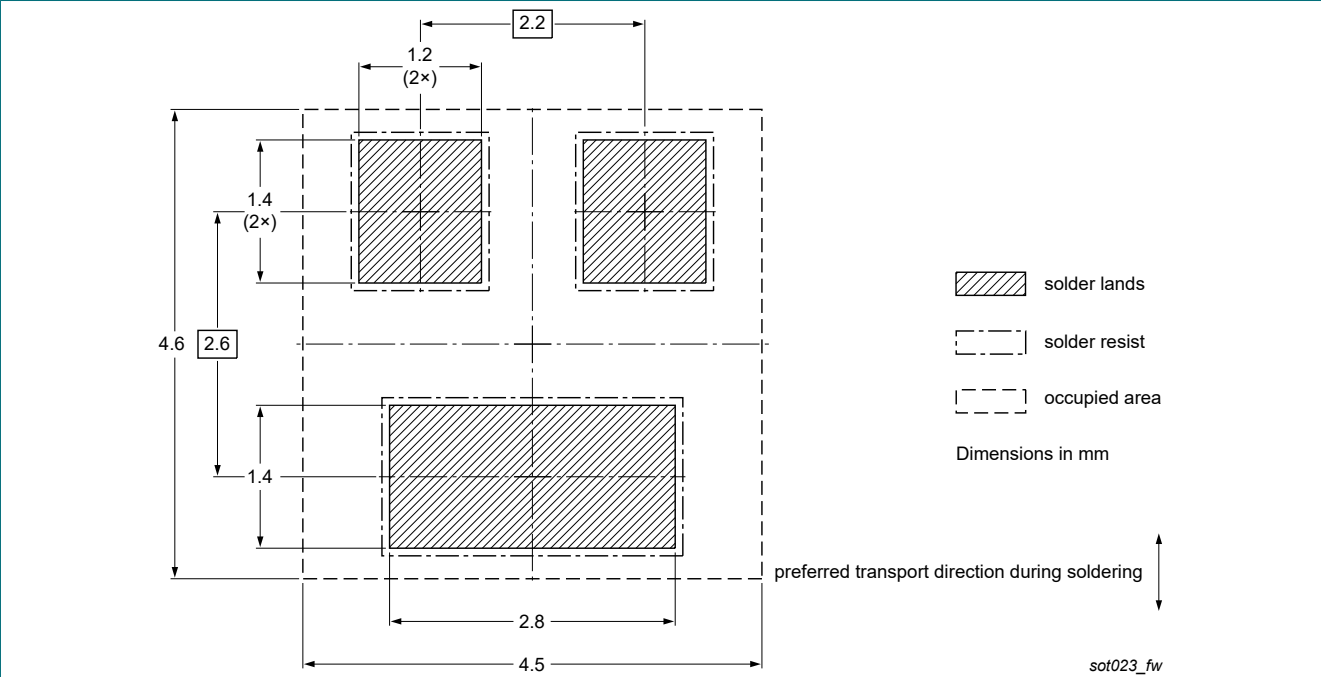


Fig. 10. Wave soldering footprint for SOT23



14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD15VS2UAT-Q v.1	20220610	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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