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Team Nexperia

# 74CBTLV16211

## 24-bit bus switch

Rev. 7 — 9 November 2016 Product data sheet

## 1. General description

The 74CBTLV16211 provides a dual 12-bit high-speed bus switch with separate output enable inputs ($1\overline{OE}$, $2\overline{OE}$). The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The switch is disabled (high-impedance OFF-state) when the output enable ($n\overline{OE}$) input is HIGH.

To ensure the high-impedance OFF-state during power-up or power-down, $1\overline{OE}$ and $2\overline{OE}$ should be tied to the $V_{CC}$ through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire $V_{CC}$ range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using $I_{OFF}$.
The $I_{OFF}$ circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- TSSOP56 packages: SOT364-1 and SOT481-2
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74CBTLV16211DGG | −40 °C to +125 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |
| 74CBTLV16211DGV | −40 °C to +125 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 4.4 mm | SOT481-2 |

## 4. Functional diagram

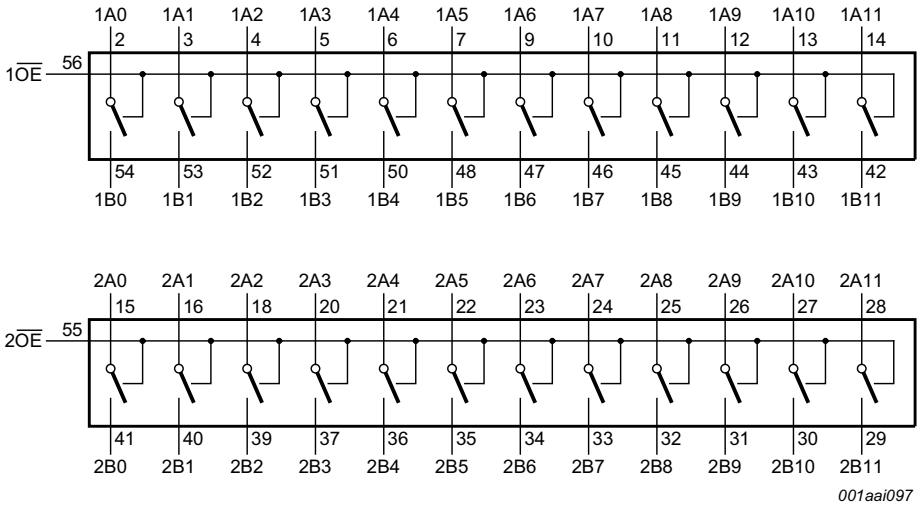



**Fig 1. Logic symbol**

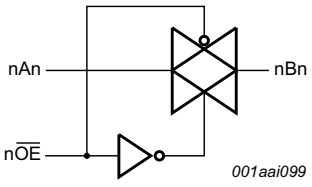



**Fig 2. Logic diagram (one switch)**

# 5. Pinning information

## 5.1 Pinning

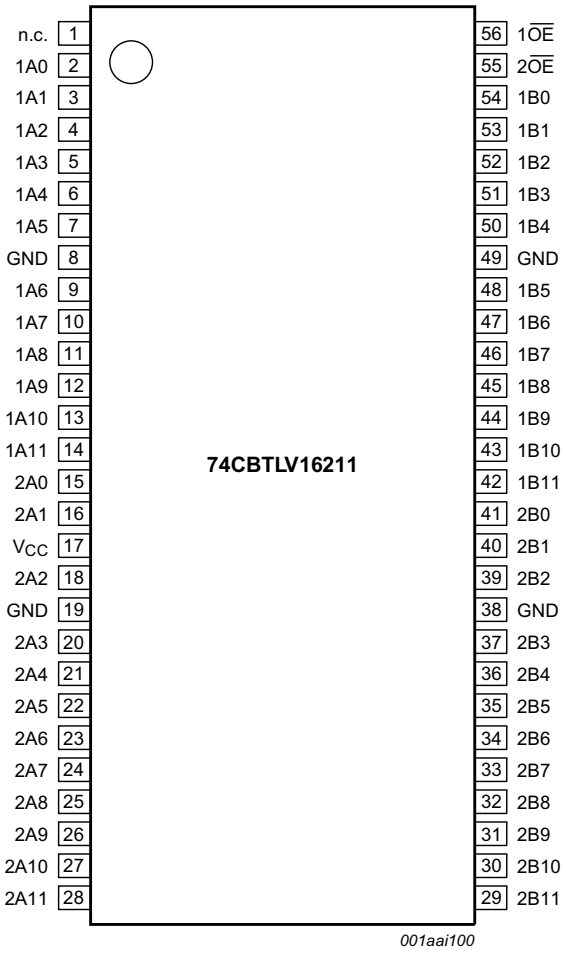



**Fig 3. Pin configuration (SOT364-1 and SOT481-2)**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| n.c. | 1 | not connected |
| 1A0 to 1A11 | 2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14 | independent input or output |
| 2A0 to 2A11 | 15, 16, 18, 20, 21, 22, 23, 24, 25, 26, 27, 28 | independent input or output |
| GND | 8, 19, 38, 49 | ground (0 V) |
| $V_{CC}$ | 17 | supply voltage |
| 2B0 to 2B11 | 41, 40, 39, 37, 36, 35, 34, 33, 32, 31, 30, 29 | independent input or output |

**Table 2. Pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| 1B0 to 1B11 | 54, 53, 52, 51, 50, 48, 47, 46, 45, 44, 43, 42 | independent input or output |
| $2\overline{OE}$ | 55 | output enable input (active-LOW) |
| $1\overline{OE}$ | 56 | output enable input (active-LOW) |

## 6. Functional description

**Table 3. Function table[1]**

| Output enable input $\overline{OE}$ | Function switch |
|---|---|
| L | ON-state |
| H | OFF-state |

[1] H = HIGH voltage level; L = LOW voltage level.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | −0.5 | +4.6 | V |
| $V_I$ | input voltage | [1] | −0.5 | +4.6 | V |
| $V_{SW}$ | switch voltage | enable and disable mode [1] | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | input clamping current | $V_I$ < −0.5 V | −50 | - | mA |
| $I_{SK}$ | switch clamping current | $V_I$ < −0.5 V | −50 | - | mA |
| $I_{SW}$ | switch current | $V_{SW}$ = 0 V to $V_{CC}$ | - | ±128 | mA |
| $I_{CC}$ | supply current | | - | +100 | mA |
| $I_{GND}$ | ground current | | −100 | - | mA |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C [2] | - | 600 | mW |

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP56 packages: above 55 °C the value of $P_{tot}$ derates linearly with 8.0 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.3 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 3.6 | V |
| $V_{SW}$ | switch voltage | enable and disable mode | 0 | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | −40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 2.3 V to 3.6 V [1] | 0 | 200 | ns/V |

[1] Applies to control signal levels.

# 9. Static characteristics

**Table 6. Static characteristics**

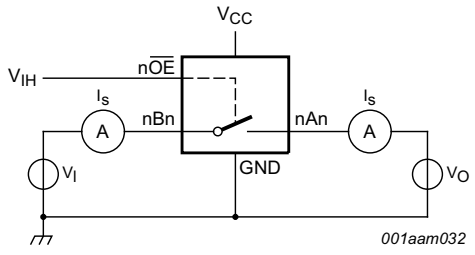
*At recommended operating conditions voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = –40 °C to +85 °C | | | $T_{amb}$ = –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 0.9 | - | 0.9 | V |
| $I_I$ | input leakage current | pin $n\overline{OE}$; $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.6 V | - | - | ±1.0 | - | ±20 | µA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 3.6 V; see Figure 4 | - | - | ±1 | - | ±20 | µA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 3.6 V; see Figure 5 | - | - | ±1 | - | ±20 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 0 V to 3.6 V; $V_{CC}$ = 0 V | - | - | ±10 | - | ±50 | µA |
| $I_{CC}$ | supply current | $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A; $V_{SW}$ = GND or $V_{CC}$; $V_{CC}$ = 3.6 V | - | - | 10 | - | 50 | µA |
| $\Delta I_{CC}$ | additional supply current | pin $n\overline{OE}$; $V_I$ = $V_{CC}$ – 0.6 V; $V_{SW}$ = GND or $V_{CC}$; $V_{CC}$ = 3.6 V [2] | - | - | 300 | - | 2000 | µA |
| $C_I$ | input capacitance | pin $n\overline{OE}$; $V_{CC}$ = 3.3 V; $V_I$ = 0 V to 3.3 V | - | 0.9 | - | - | - | pF |
| $C_{S(OFF)}$ | OFF-state capacitance | $V_{CC}$ = 3.3 V; $V_I$ = 0 V to 3.3 V | - | 5.2 | - | - | - | pF |
| $C_{S(ON)}$ | ON-state capacitance | $V_{CC}$ = 3.3 V; $V_I$ = 0 V to 3.3 V | - | 14.3 | - | - | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

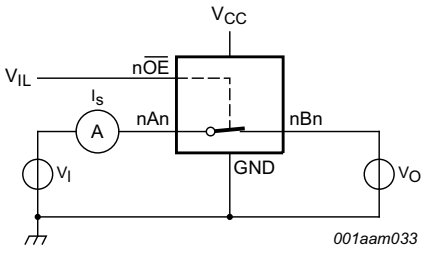
[2] One input at 3 V, other inputs at $V_{CC}$ or GND.

## 9.1 Test circuits




$V_I$ = $V_{CC}$ or GND and $V_O$ = GND or $V_{CC}$.

**Fig 4. Test circuit for measuring OFF-state leakage current (one channel)**




$V_I$ = $V_{CC}$ or GND and $V_O$ = open circuit.

**Fig 5. Test circuit for measuring ON-state leakage current (one channel)**

## 9.2 ON resistance

**Table 7. Resistance $R_{ON}$**

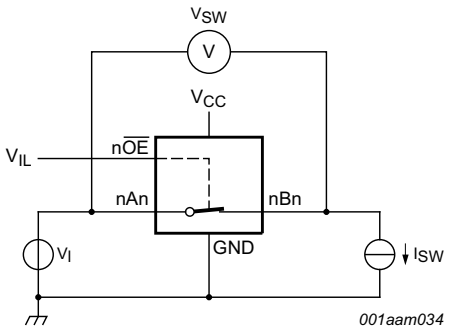
*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.*

| Symbol | Parameter | Conditions | | $T_{amb}$ = –40 °C to +85 °C | | | $T_{amb}$ = –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $R_{ON}$ | ON resistance | $V_{CC}$ = 2.3 V to 2.7 V; see Figure 7 to Figure 9 | [2] | | | | | | |
| | | $I_{SW}$ = 64 mA; $V_I$ = 0 V | | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | $I_{SW}$ = 24 mA; $V_I$ = 0 V | | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | $I_{SW}$ = 15 mA; $V_I$ = 1.7 V | | - | 8.4 | 40 | - | 60.0 | Ω |
| | | $V_{CC}$ = 3.0 V to 3.6 V; see Figure 10 to Figure 12 | | | | | | | |
| | | $I_{SW}$ = 64 mA; $V_I$ = 0 V | | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | $I_{SW}$ = 24 mA; $V_I$ = 0 V | | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | $I_{SW}$ = 15 mA; $V_I$ = 2.4 V | | - | 6.2 | 15 | - | 25.5 | Ω |

[1] Typical values are measured at $T_{amb}$ = 25 °C and nominal $V_{CC}$.

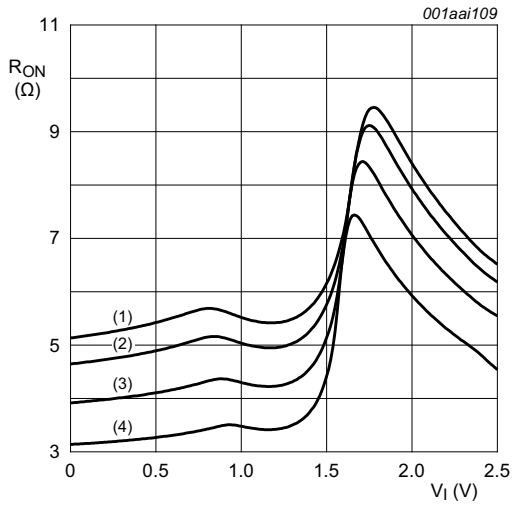
[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 9.3 ON resistance test circuit and graphs



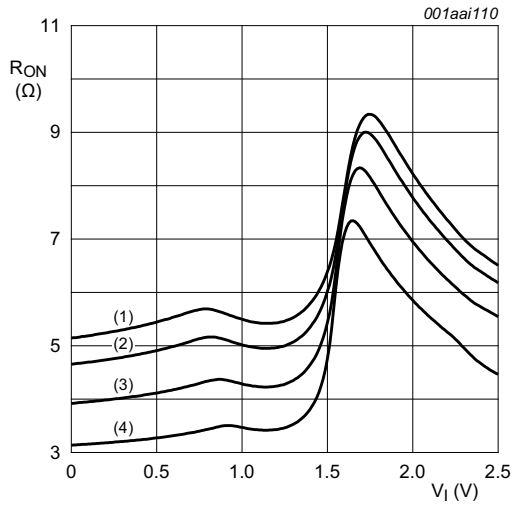

$R_{ON} = V_{SW} / I_{SW}$.

**Fig 6. Test circuit for measuring ON resistance (one channel)**



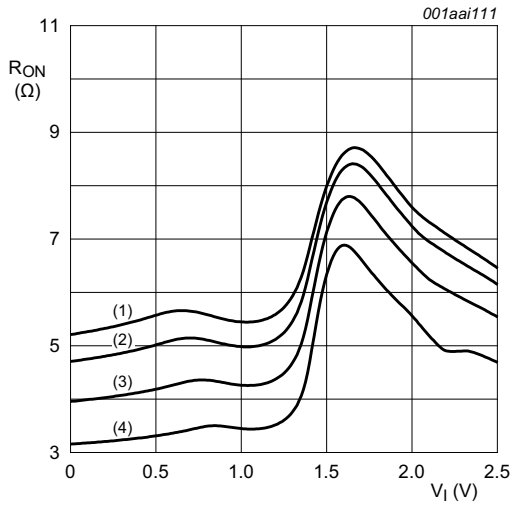

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = –40 °C.

**Fig 7. ON resistance as a function of input voltage; $V_{CC}$ = 2.5 V; $I_{SW}$ = 15 mA**



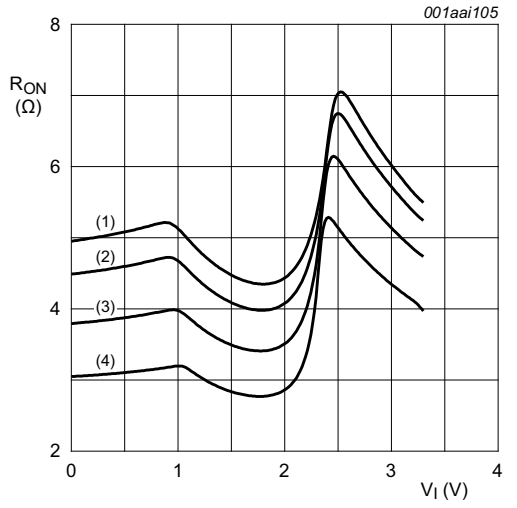

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = −40 °C.

**Fig 8. ON resistance as a function of input voltage; $V_{CC}$ = 2.5 V; $I_{SW}$ = 24 mA**



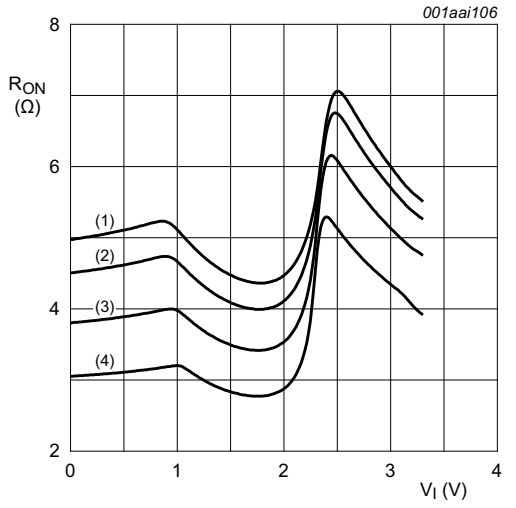

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = −40 °C.

**Fig 9. ON resistance as a function of input voltage; $V_{CC}$ = 2.5 V; $I_{SW}$ = 64 mA**



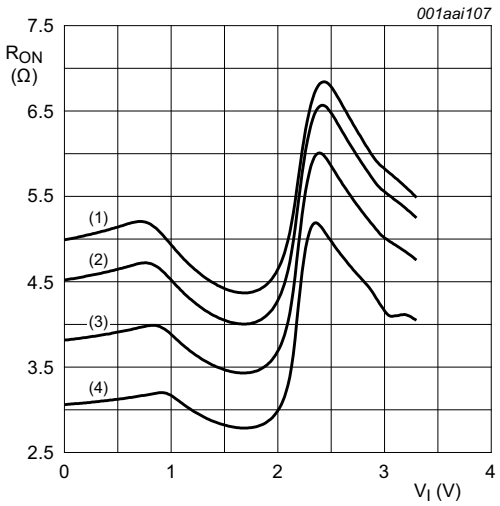

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = −40 °C.

**Fig 10. ON resistance as a function of input voltage; $V_{CC}$ = 3.3 V; $I_{SW}$ = 15 mA**




(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = −40 °C.

**Fig 11. ON resistance as a function of input voltage; $V_{CC}$ = 3.3 V; $I_{SW}$ = 24 mA**




(1) $T_{amb}$ = 125 °C.

(2) $T_{amb}$ = 85 °C.

(3) $T_{amb}$ = 25 °C.

(4) $T_{amb}$ = −40 °C.

**Fig 12. ON resistance as a function of input voltage; $V_{CC}$ = 3.3 V; $I_{SW}$ = 64 mA**

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

*GND = 0 V; for test circuit see Figure 15*

| Symbol | Parameter | Conditions | $T_{amb}$ = –40 °C to +85 °C | | | $T_{amb}$ = –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | nAn to nBn or nBn to nAn; see Figure 13 [2][3] | | | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.13 | - | 0.2 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 0.2 | - | 0.31 | ns |
| $t_{en}$ | enable time | $n\overline{OE}$ to nAn or nBn; see Figure 14 [4] | | | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.0 | 7.0 | 1.0 | 7.8 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 1.7 | 6.2 | 1.0 | 6.8 | ns |
| $t_{dis}$ | disable time | $n\overline{OE}$ to nAn or nBn; see Figure 14 [5] | | | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.6 | 7.2 | 1.0 | 8.1 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.0 | 7.7 | 1.0 | 8.8 | ns |

[1] All typical values are measured at $T_{amb}$ = 25 °C and at nominal $V_{CC}$.

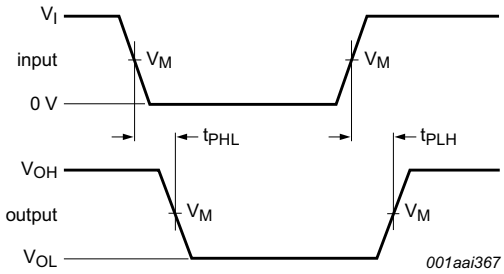
[2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

[3] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[4] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[5] $t_{dis}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.

## 11. Waveforms



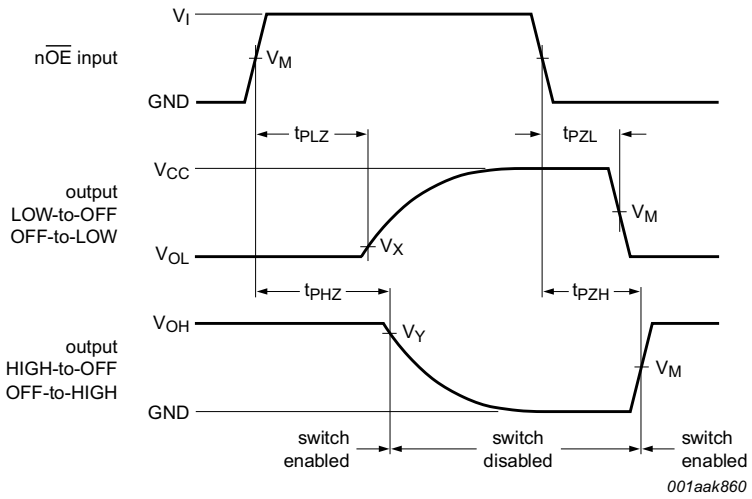

Measurement points are given in Table 9.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 13. The data input (nAn or nBn) to output (nBn or nAn) propagation delays**

**Table 9. Measurement points**

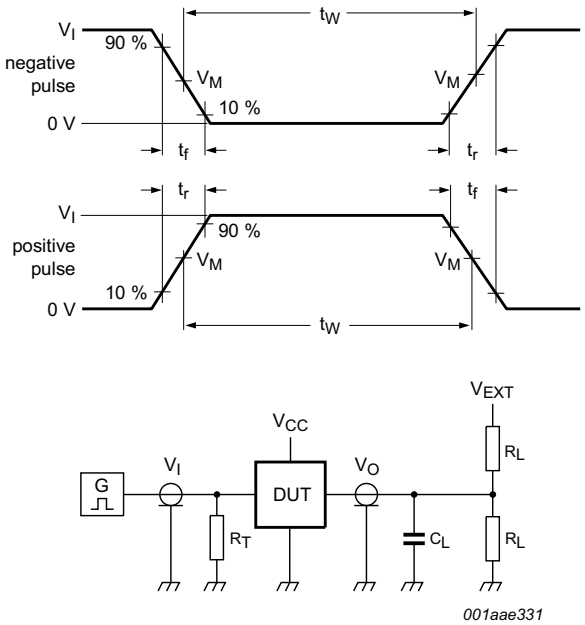
| Supply voltage | Input | | | Output | | |
|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_I$ | $t_r = t_f$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $V_{CC}$ | ≤ 2.0 ns | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ − 0.15 V |
| 3.0 V to 3.6 V | $0.5V_{CC}$ | $V_{CC}$ | ≤ 2.0 ns | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |




Measurement points are given in Table 9.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 14. Enable and disable times**




Test data is given in Table 10.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 15. Test circuit for measuring switching times**

**Table 10. Test data**

| Supply voltage | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 2.3 V to 2.7 V | 30 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 3.0 V to 3.6 V | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |

## 11.1 Additional dynamic characteristics

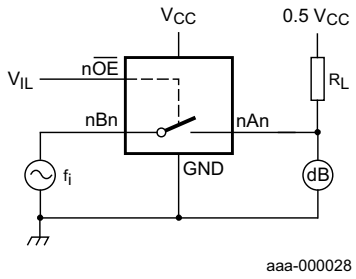
**Table 11. Additional dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I$ = GND or $V_{CC}$ (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.*

| Symbol | Parameter | Conditions | $T_{amb}$ = 25 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{(-3dB)}$ | −3 dB frequency response | $V_{CC}$ = 3.3 V; $R_L$ = 50 Ω; see Figure 16 [1] | - | 458 | - | MHz |

[1] $f_i$ is biased at $0.5V_{CC}$.

## 11.2 Test circuits

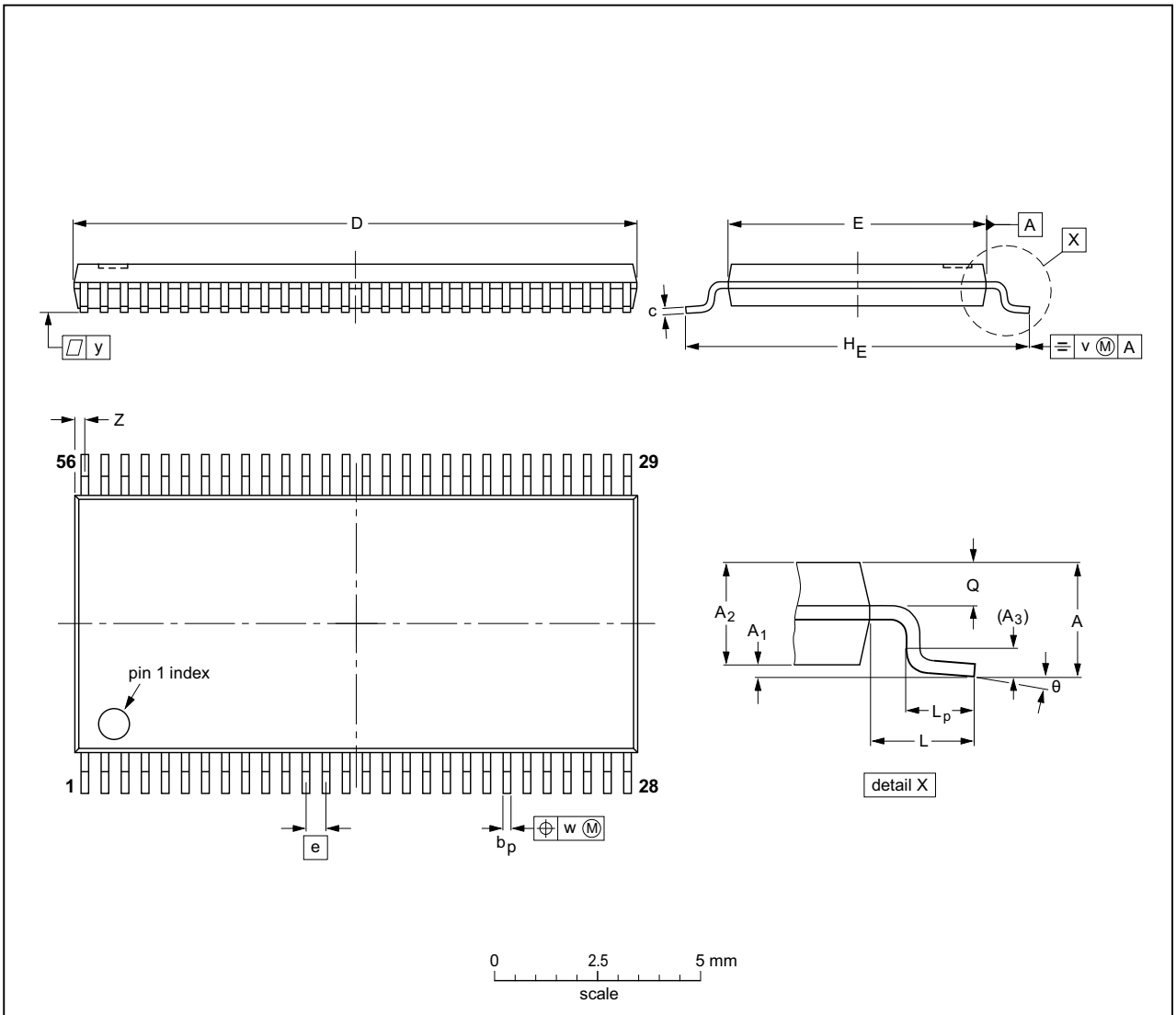



nOE connected to GND; Adjust $f_i$ voltage to obtain 0 dBm level at output. Increase $f_i$ frequency until dB meter reads −3 dB.

**Fig 16. Test circuit for measuring the frequency response when channel is in ON-state**

## 12. Package outline

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | **0.2**<br>**0.1** | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | $8^o$<br>$0^o$ |

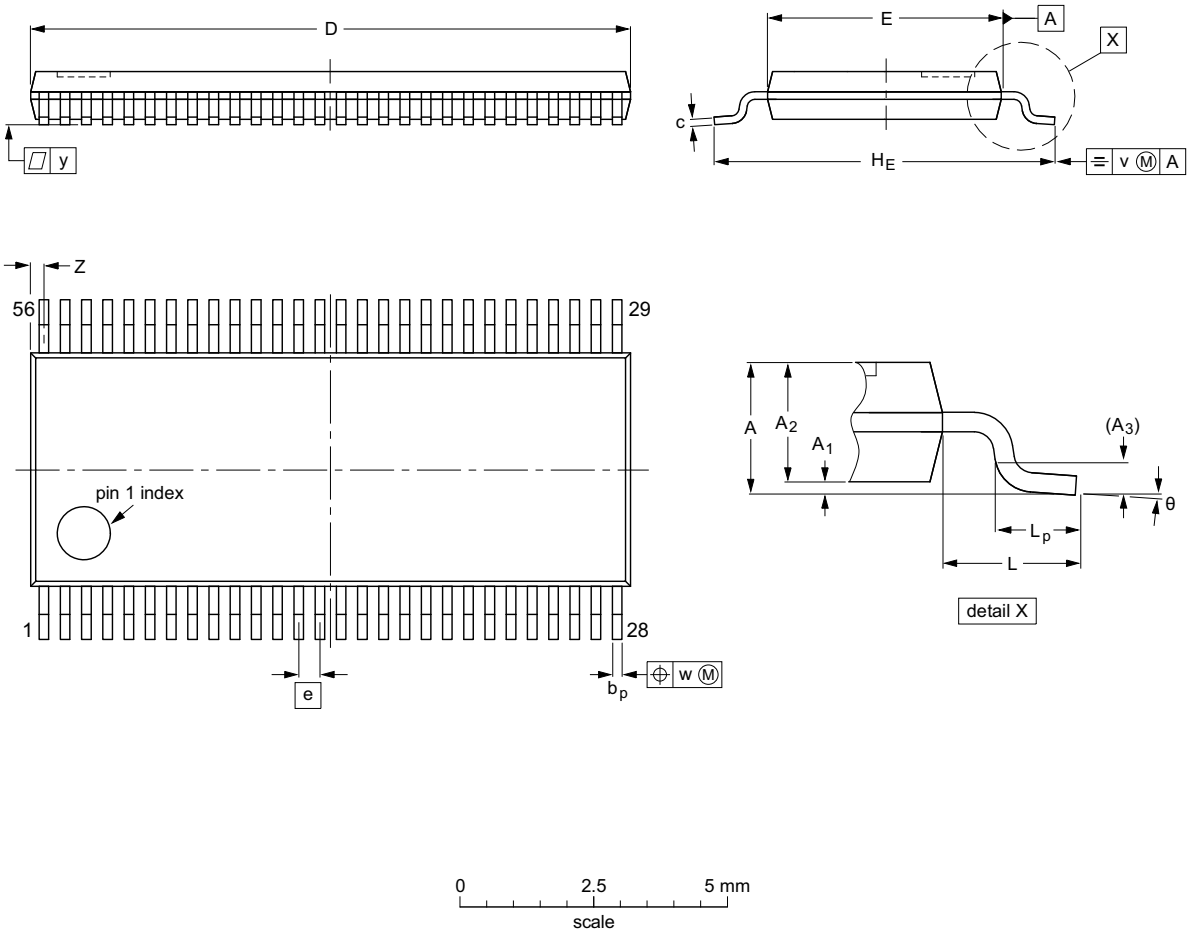
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT364-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 17. Package outline SOT364-1 (TSSOP56)**

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 4.4 mm** **SOT481-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.80 | 0.25 | 0.23<br>0.13 | 0.20<br>0.09 | 11.4<br>11.2 | 4.5<br>4.3 | 0.4 | 6.6<br>6.2 | 1 | 0.75<br>0.45 | 0.2 | 0.07 | 0.08 | 0.4<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT481-2 | - - - | MO-194 | - - - | | | 01-11-24 |

**Fig 18. Package outline SOT481-2 (TSSOP56)**

## 13. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

## 14. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74CBTLV16211 v.7 | 20161109 | Product data sheet | - | 74CBTLV16211 v.6 |
| Modifications: | • Section 11.1 and Section 11.2 added. | | | |
| 74CBTLV16211 v.6 | 20111215 | Product data sheet | - | 74CBTLV16211 v.5 |
| Modifications: | • Legal pages updated. | | | |
| 74CBTLV16211 v.5 | 20101230 | Product data sheet | - | 74CBTLV16211 v.4 |
| 74CBTLV16211 v.4 | 20100816 | Product data sheet | - | 74CBTLV16211 v.3 |
| 74CBTLV16211 v.3 | 20100112 | Product data sheet | - | 74CBTLV16211 v.2 |
| 74CBTLV16211 v.2 | 20090826 | Product data sheet | - | 74CBTLV16211 v.1 |
| 74CBTLV16211 v.1 | 20080620 | Product data sheet | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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