

# 74ALVC16245; 74ALVCH16245

16-bit transceiver with direction pin; 3-state

Rev. 5 — 16 October 2020

Product data sheet

## 1. General description

The 74ALVC16245; 74ALVCH16245 is a 16-bit transceiver with 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables (1OE and 2OE) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

The 74ALVCH16245 has an active bushold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V<sub>CC</sub> and GND pins for minimize noise and ground bounce
- Overvoltage tolerant inputs to 5.5 V
- Direct interface with TTL levels
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- All data inputs have bushold (74ALVCH16245 only)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at V<sub>CC</sub> = 3.0 V.
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC16245DL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ALVC16245DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ALVCH16245DGG				

4. Functional diagram

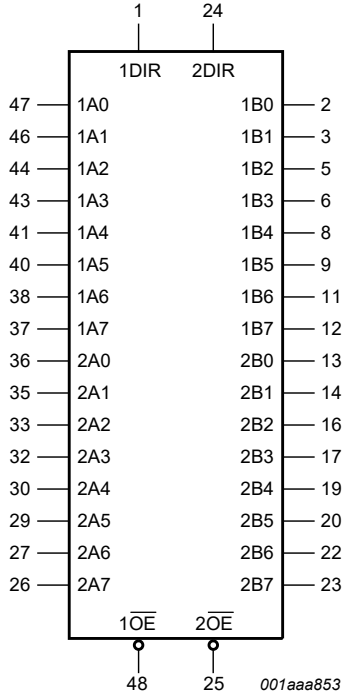


Fig. 1. Logic symbol

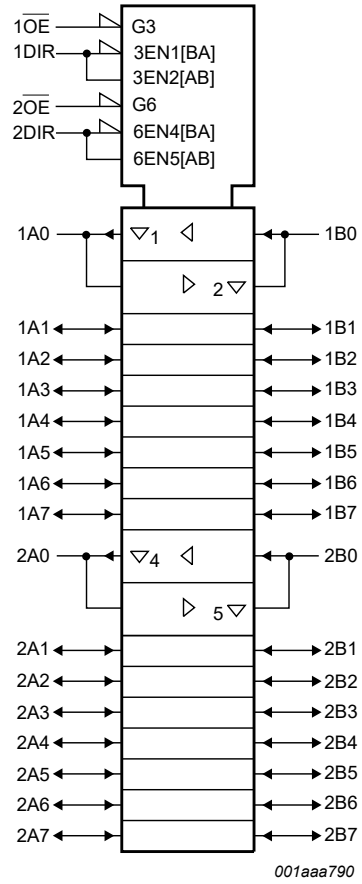


Fig. 2. IEC logic symbol

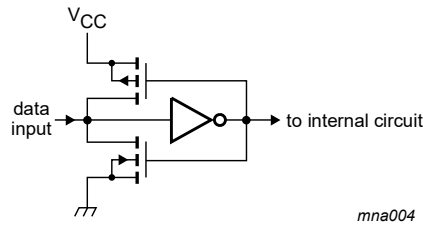


Fig. 3. Bushold circuit

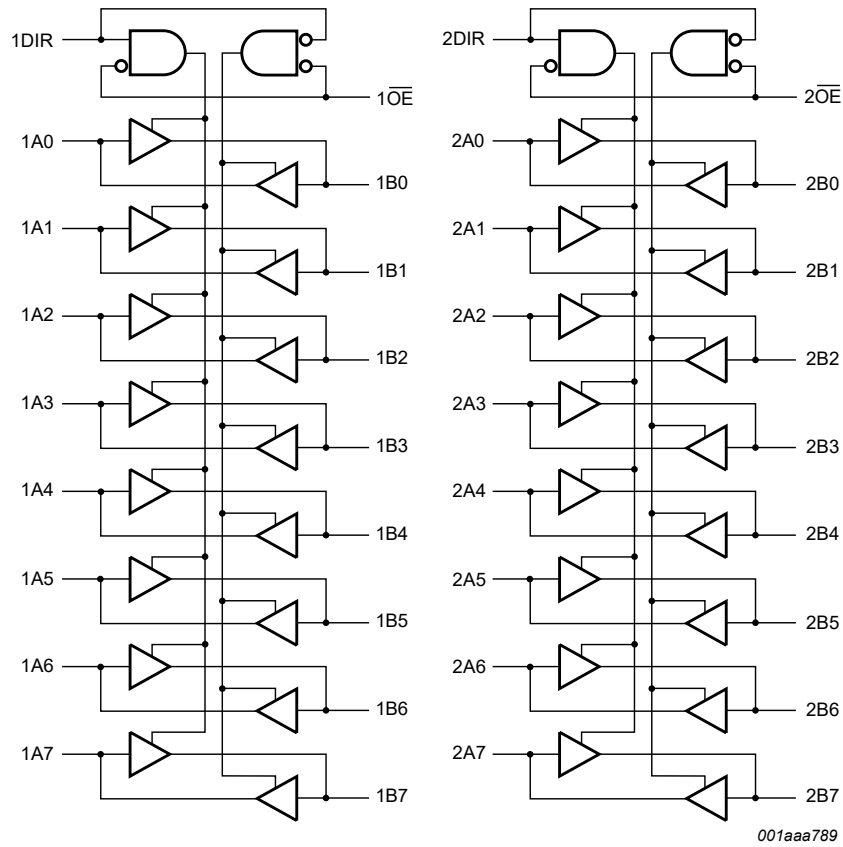


Fig. 4. Logic diagram

## 5. Pinning information

### 5.1. Pinning

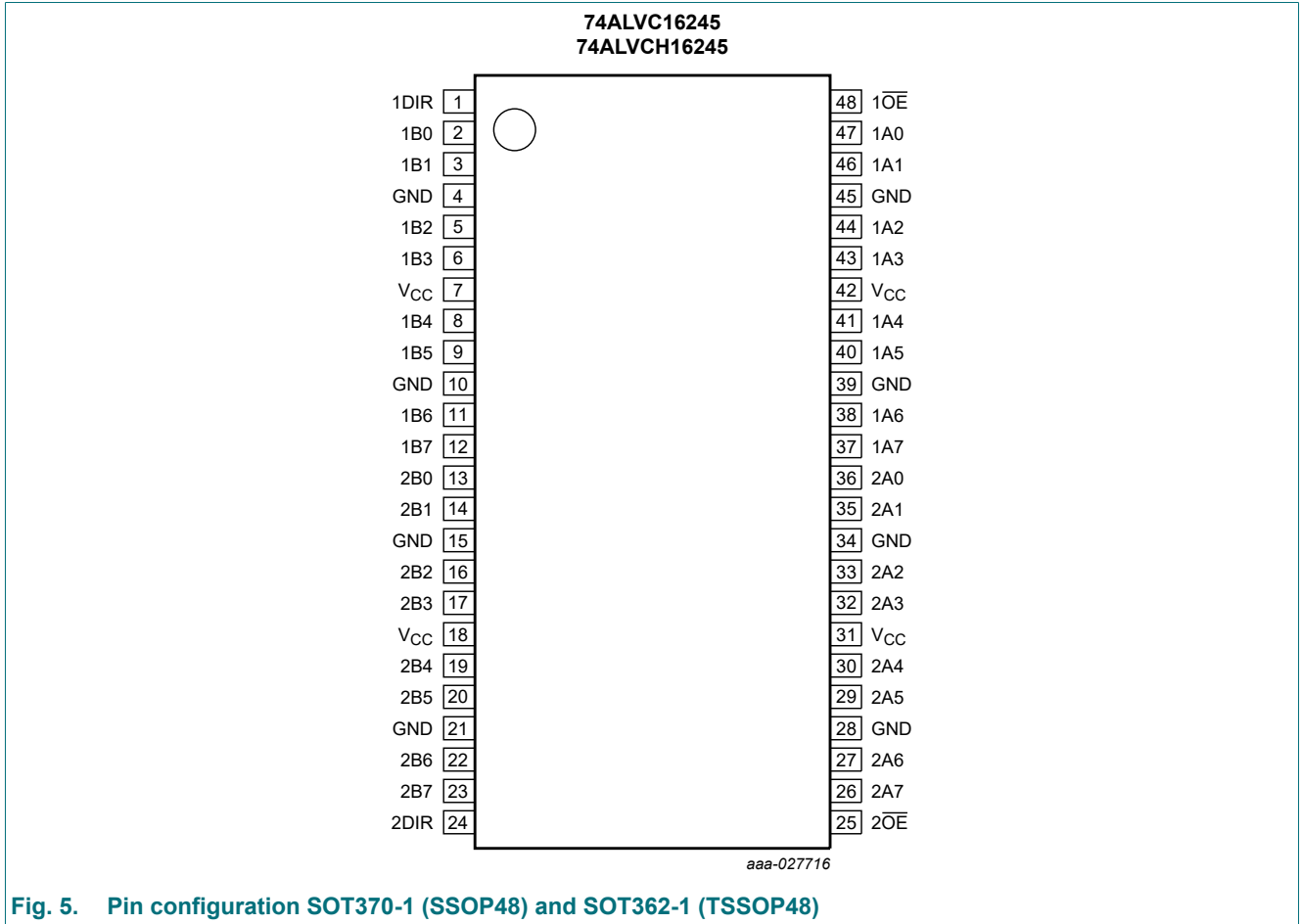


Fig. 5. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control inputs
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data output or input
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	positive supply voltage
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data output or input
1OE, 2OE	48, 25	output enable input (active LOW)
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input or output
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input or output

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Input or output	
nOE	nDIR	nAn	nBn
L	L	output nAn = nBn	input
L	H	input	output nBn = nAn
H	X	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage	data inputs with bushold [1]	-0.5	V <sub>CC</sub> + 0.5	V
		data inputs without bushold [1]	-0.5	+4.6	V
		control pins [1]	-0.5	+4.6	V
V <sub>O</sub>	output voltage	[1]	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	maximum speed performance				
		C <sub>L</sub> = 30 pF	2.3	-	2.7	V
		C <sub>L</sub> = 50 pF	3.0	-	3.6	V
		low-voltage applications	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.3 V to 3.0 V	-	-	20	ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	GND	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.70	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	10	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	40	μA
ΔI <sub>CC</sub>	additional supply current	74ALVCH16245; per data I/O pin; V <sub>CC</sub> = 2.3 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	150	750	μA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V [2]	45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V [2]	75	150	-	μA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V [2]	-45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V [2]	-75	-175	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 3.6 V [2]	500	-	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6 V [2]	-500	-	-	μA
C <sub>I</sub>	input capacitance		-	4.0	-	pF
C <sub>I/O</sub>	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] Valid for data inputs of bushold parts.

## 10. Dynamic characteristics

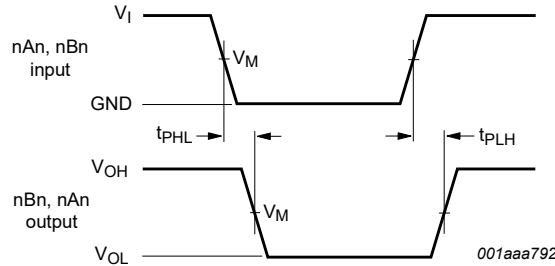
**Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see Fig. 6 [2]				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.0	3.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.1	3.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	1.9	3.0	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn; n $\overline{\text{OE}}$ to nBn; see Fig. 7 [3]				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.7	5.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.0	5.4	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.3	4.4	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn; n $\overline{\text{OE}}$ to nBn; see Fig. 7 [4]				
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.2	5.2	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.1	4.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.8	4.1	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; V <sub>I</sub> = GND to V <sub>CC</sub> [5]				
		outputs enabled	-	29	-	pF
		outputs disabled	-	5	-	pF

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C  
 Typical values for V<sub>CC</sub> = 2.3 V to 2.7 V are measured at V<sub>CC</sub> = 2.5 V.  
 Typical values for V<sub>CC</sub> = 3.0 V to 3.6 V are measured at V<sub>CC</sub> = 3.3 V.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.
- [4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in Volts;  
 N = total load switching outputs;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

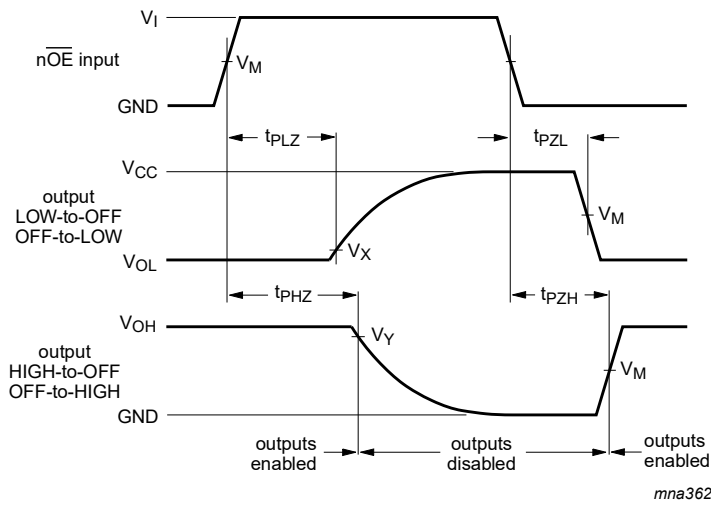
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 6. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Measurement points are given in Table 8.

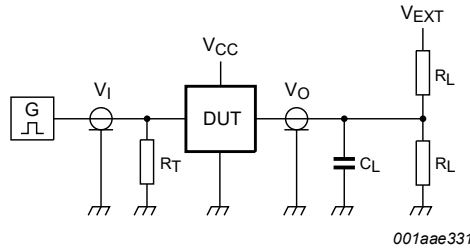
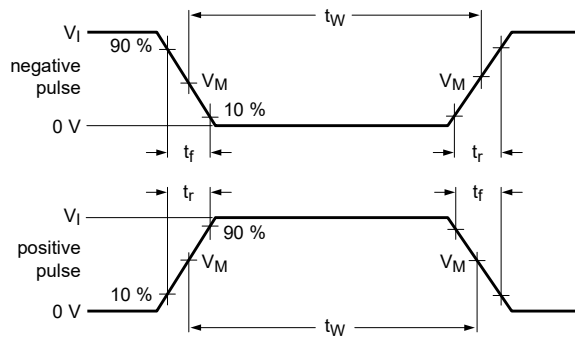
$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
$\geq 2.7 \text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$





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Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance includes jig and probe capacitance.

$R_T$  = Termination resistance should be equal to  $Z_o$  of pulse generator.

$V_{EXT}$  = Test voltage for switching times.

**Fig. 8. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$
< 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$

11. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

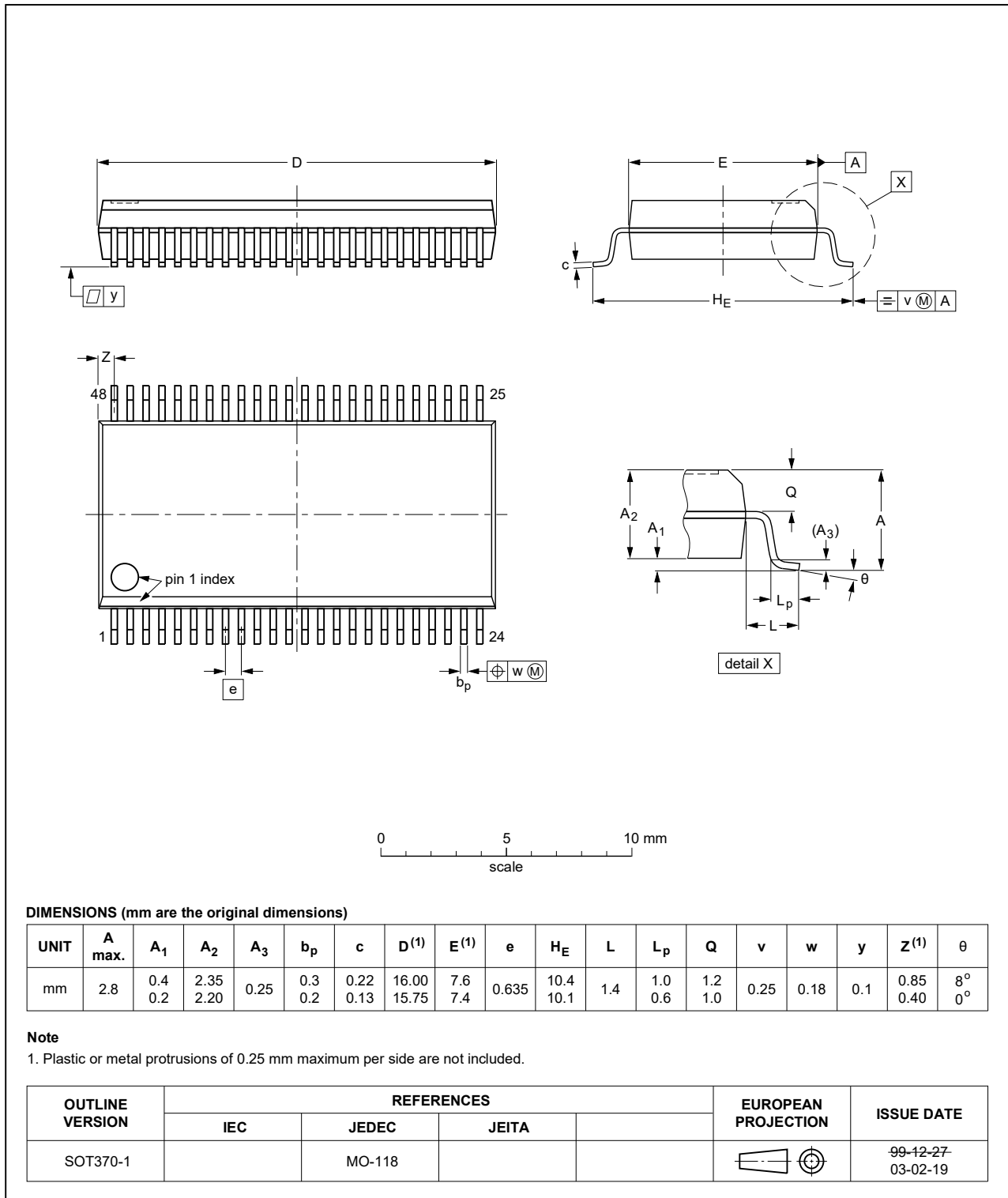


Fig. 9. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

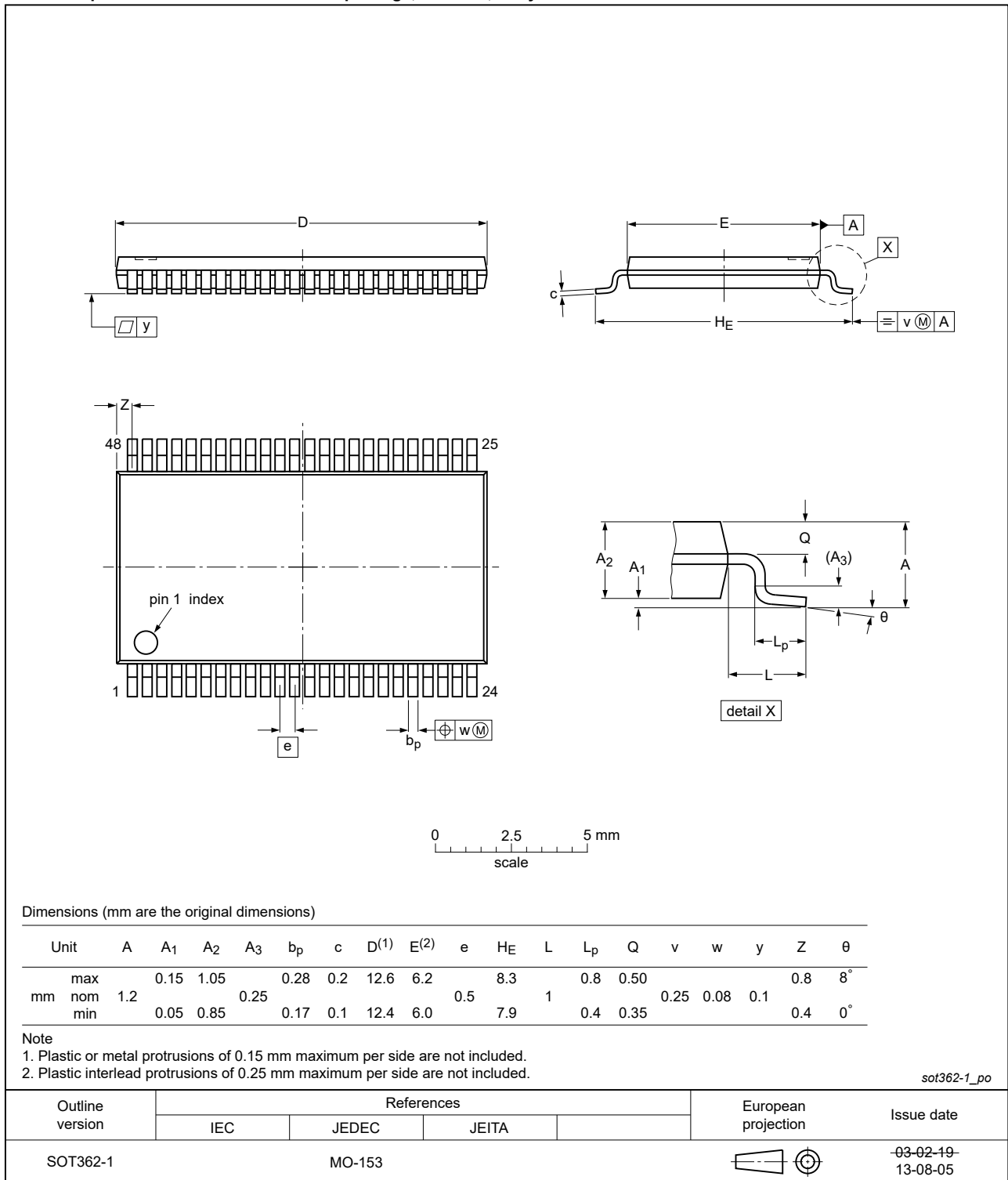


Fig. 10. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC_ALVCH16245 v.5	20201016	Product data sheet	-	74ALVC_ALVCH16245 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74ALVCH16245DL (SOT370-1 / SSOP48) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for P<sub>tot</sub> total power dissipation updated.</li> </ul>			
74ALVC_ALVCH16245 v.4	20171121	Product data sheet	-	74ALVC_ALVCH16245 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ALVC_ALVCH16245 v.3	20040512	Product data sheet	-	74ALVCH16245 v.2 74ALVC16245_ 74ALVCH16245 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 1</a>: General description updated.</li> </ul>			
74ALVCH16245 v.2	19980629	Product specification	-	74ALVCH16245 v.1
74ALVC16245_ 74ALVCH16245 v.1	19980325	Product specification	-	-
74ALVCH16245 v.1	19950102	Preliminary specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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