

# 74LVC2G3157

Dual 10  $\Omega$  single-pole double-throw analog switch

Rev. 3 — 25 March 2019

Product data sheet

## 1. General description

The 74LVC2G3157 is a dual low-ohmic single-pole double-throw analog switch suitable for use as an analog or digital 2:1 multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ).

Schmitt trigger action at the select inputs makes the circuit tolerant of slower input rise and fall times across the entire  $V_{CC}$  range from 1.65 V to 5.5 V.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
  - 10.4  $\Omega$  (typical) at  $V_{CC} = 2.7$  V
  - 7.8  $\Omega$  (typical) at  $V_{CC} = 3.3$  V
  - 6.2  $\Omega$  (typical) at  $V_{CC} = 5$  V
- Switch current capability of 32 mA
- Break-before-make switching
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - MM JESD22-A115-C exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Select input accepts voltages up to 5.5 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G3157DP	-40 °C to +125 °C	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1
74LVC2G3157GM	-40 °C to +125 °C	XQFN10	plastic extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm	SOT1049-3

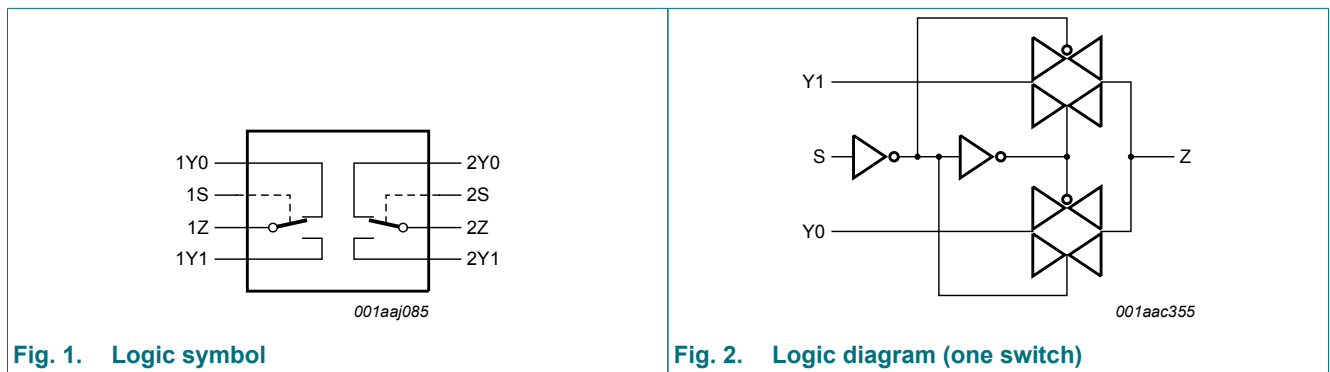
## 4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC2G3157DP	YJ
74LVC2G3157GM	YJ

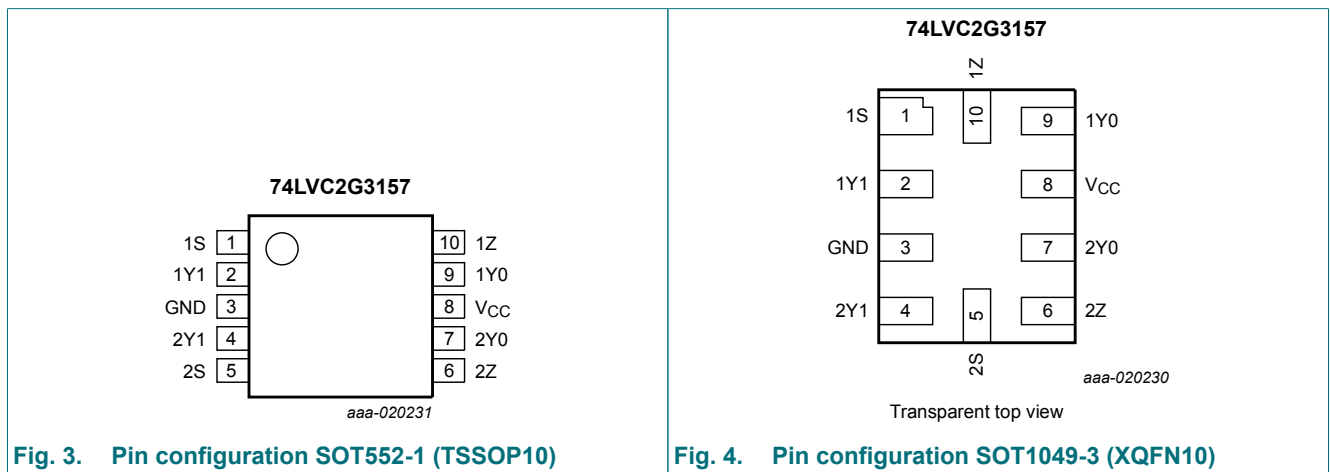
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



## 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1S	1	select input
1Y1	2	independent input or output
GND	3	ground (0 V)
2Y1	4	independent input or output
2S	5	select input
2Z	6	common output or input
2Y0	7	independent input or output
V <sub>CC</sub>	8	supply voltage
1Y0	9	independent input or output
1Z	10	common output or input

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nS	Channel on
L	nY0
H	nY1

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
V <sub>I</sub>	input voltage	[1]	-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	-50	-	mA
I <sub>SK</sub>	switch clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V	-	±50	mA
V <sub>SW</sub>	switch voltage	enable and disable mode [2]	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>SW</sub>	switch current	V <sub>SW</sub> > -0.5 V or V <sub>SW</sub> < V <sub>CC</sub> + 0.5 V	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [3]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For TSSOP10 package: above 120°C the value of P<sub>tot</sub> derates linearly with 8.3 mW/K.

For XQFN10 package: above 90°C the value of P<sub>tot</sub> derates linearly with 4.2 mW/K.

## 9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_{SW}$	switch voltage	enable and disable mode [1]	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$ [2]	-	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$ [2]	-	-	10	ns/V

- [1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.
- [2] Applies to control signal levels.

## 10. Static characteristics

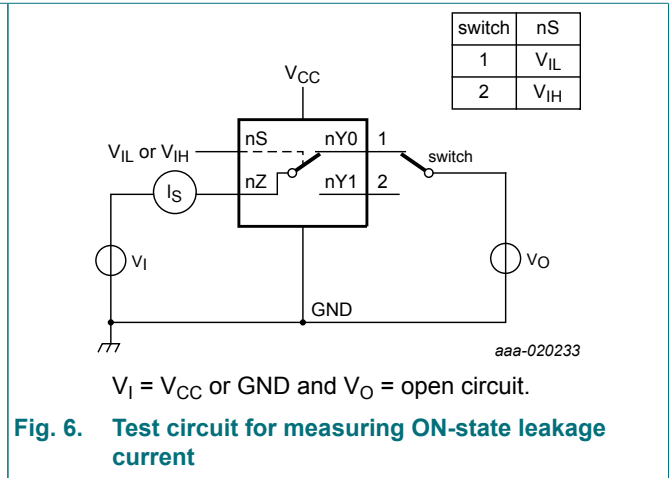
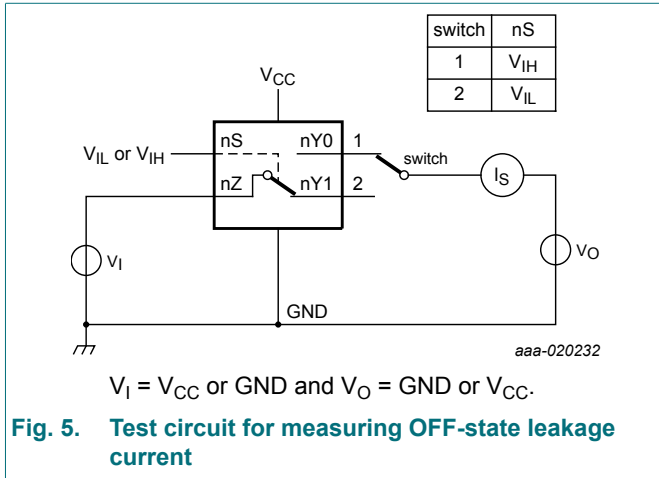
Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$			-40 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
$I_I$	input leakage current	pin nS; $V_I = 5.5 \text{ V or GND}$ ; $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$ [2]	-	$\pm 0.1$	$\pm 1$	-	$\pm 1$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC} = 5.5 \text{ V}$ ; see Fig. 5 [2]	-	$\pm 0.1$	$\pm 0.2$	-	$\pm 0.5$	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$V_{CC} = 5.5 \text{ V}$ ; see Fig. 6 [2]	-	$\pm 0.1$	$\pm 1$	-	$\pm 2$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = 5.5 \text{ V or GND}$ ; $V_{SW} = \text{GND or } V_{CC}$ ; $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ [2]	-	0.1	4	-	4	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	pin nS; $V_I = V_{CC} - 0.6 \text{ V}$ ; $V_{CC} = 5.5 \text{ V}$ ; $V_{SW} = \text{GND or } V_{CC}$ [2]	-	5	500	-	500	$\mu\text{A}$
$C_I$	input capacitance		-	2.5	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	6.0	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	18	-	-	-	pF

- [1] Typical values are measured at  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .
- [2] These typical values are measured at  $V_{CC} = 3.3 \text{ V}$

10.1. Test circuits



10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Fig. 8 to Fig. 13.

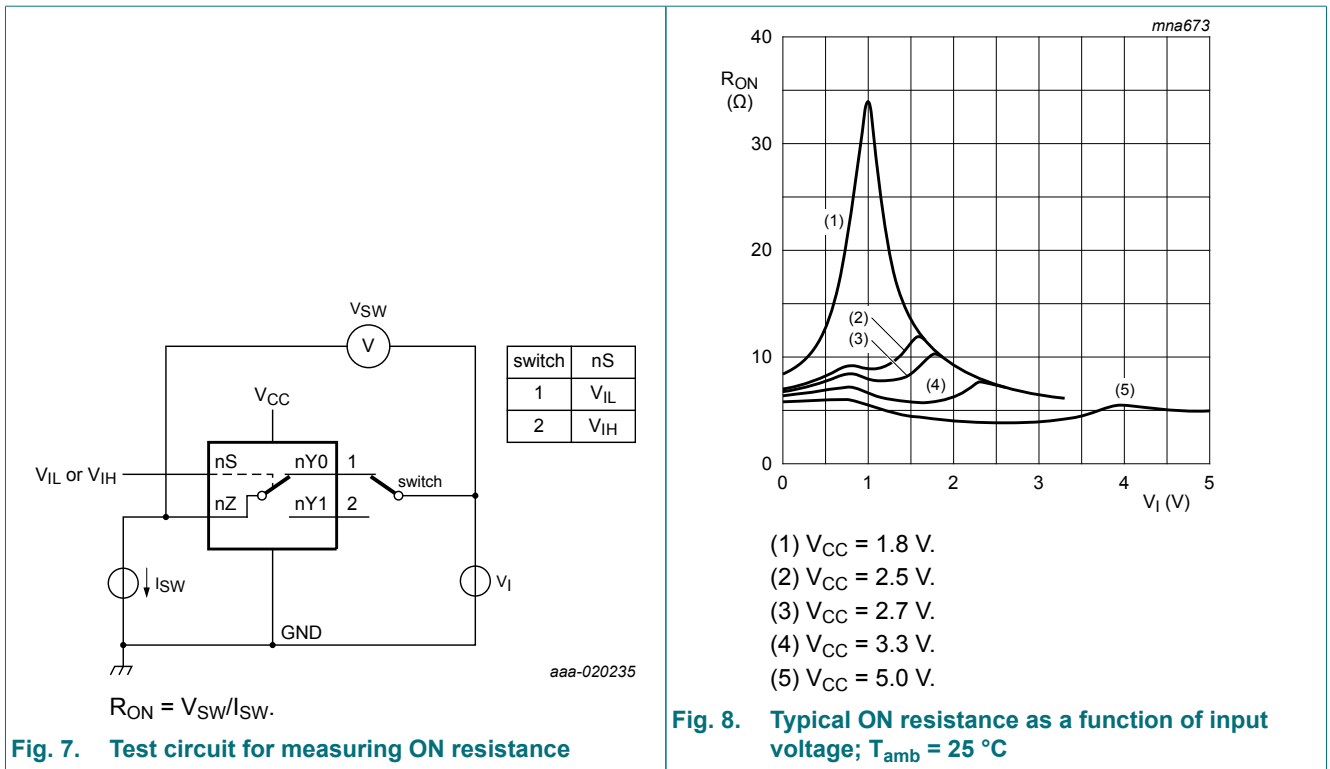
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
RON(peak)	ON resistance (peak)	$V_I =$ GND to $V_{CC}$ ; see Fig. 7						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	34.0	130	-	195	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	12.0	30	-	45	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	10.4	25	-	38	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	7.8	20	-	30	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	6.2	15	-	23	Ω
RON(rail)	ON resistance (rail)	$V_I =$ GND; see Fig. 7						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	8.2	18	-	27	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	7.1	16	-	24	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	6.9	14	-	21	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	6.5	12	-	18	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	5.8	10	-	15	Ω
		$V_I = V_{CC}$ ; see Fig. 7						
		$I_{SW} = 4$ mA; $V_{CC} = 1.65$ V to 1.95 V	-	10.4	30	-	45	Ω
		$I_{SW} = 8$ mA; $V_{CC} = 2.3$ V to 2.7 V	-	7.6	20	-	30	Ω
		$I_{SW} = 12$ mA; $V_{CC} = 2.7$ V	-	7.0	18	-	27	Ω
		$I_{SW} = 24$ mA; $V_{CC} = 3.0$ V to 3.6 V	-	6.1	15	-	23	Ω
		$I_{SW} = 32$ mA; $V_{CC} = 4.5$ V to 5.5 V	-	4.9	10	-	15	Ω

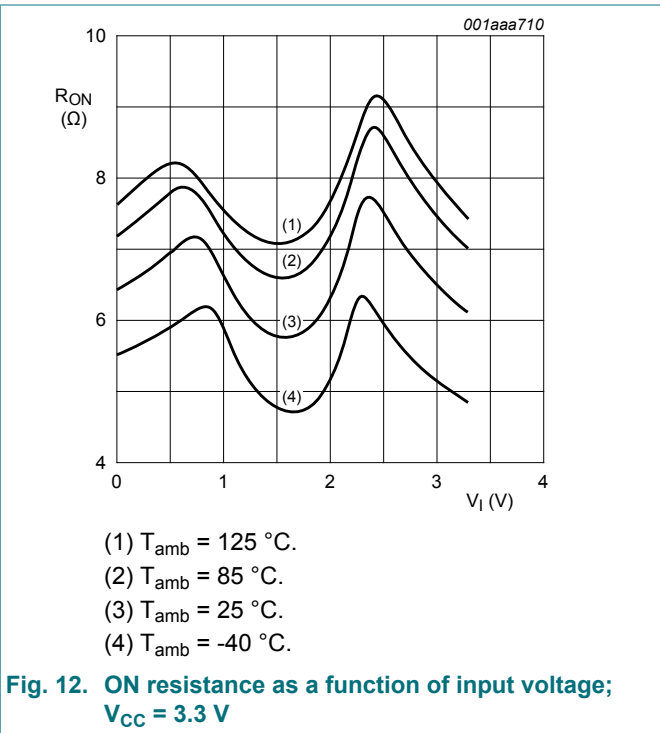
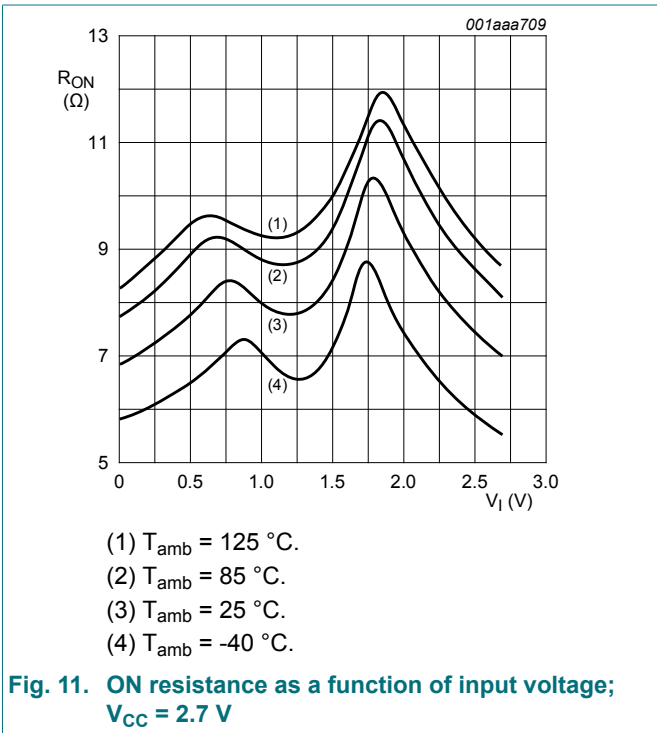
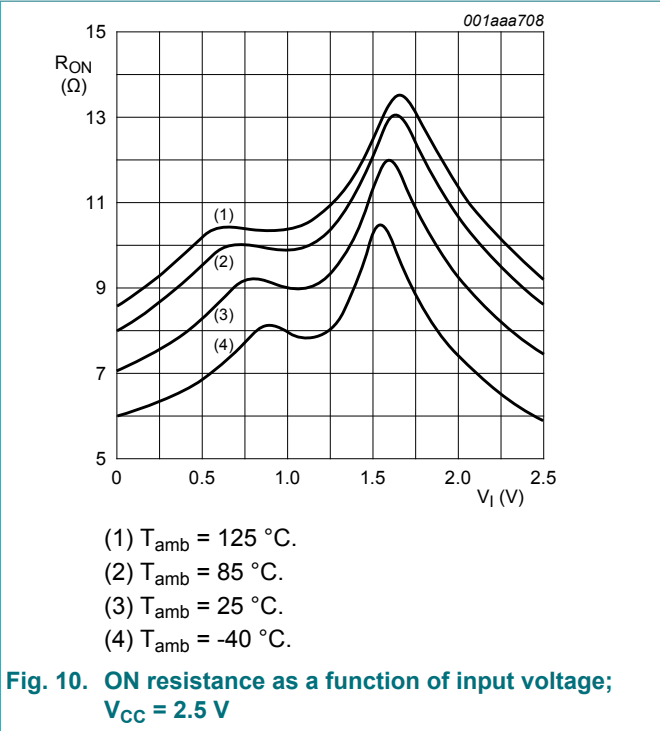
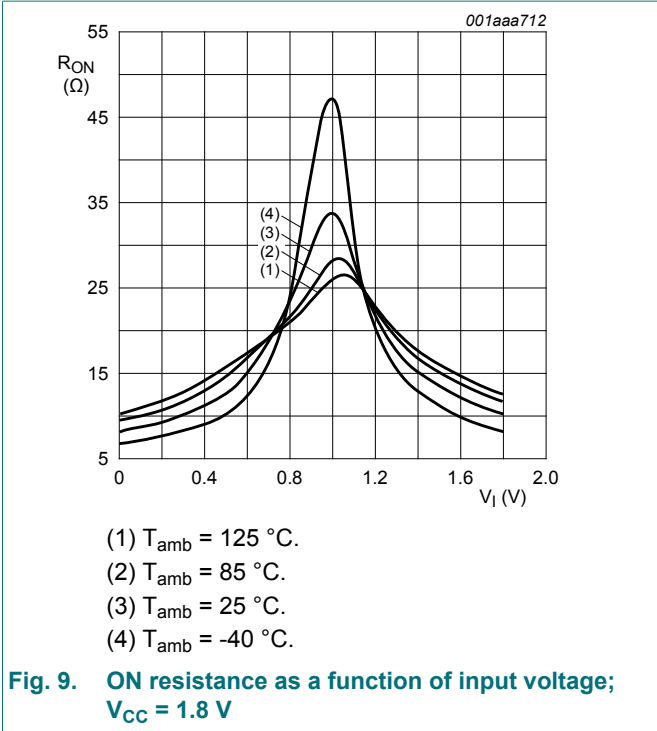
Dual 10 Ω single-pole double-throw analog switch

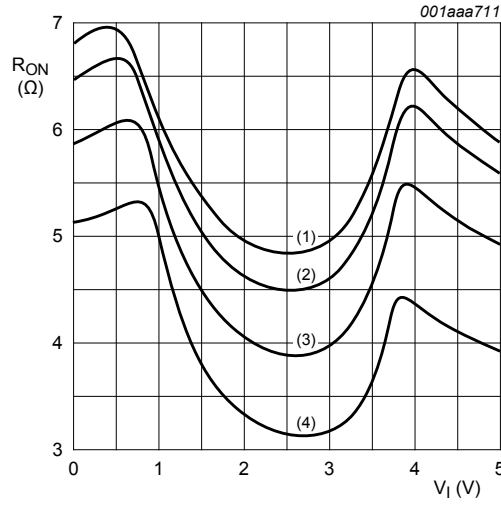
Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ[1]	Max	Min		Max
R <sub>ON(flat)</sub>	ON resistance (flatness)	V <sub>I</sub> = GND to V <sub>CC</sub> [2]						
		I <sub>SW</sub> = 4 mA; V <sub>CC</sub> = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I <sub>SW</sub> = 8 mA; V <sub>CC</sub> = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I <sub>SW</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	3.5	-	-	-	Ω
		I <sub>SW</sub> = 24 mA; V <sub>CC</sub> = 3.0 V to 3.6 V	-	2.0	-	-	-	Ω
		I <sub>SW</sub> = 32 mA; V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and nominal V<sub>CC</sub>.
- [2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V<sub>CC</sub> and temperature.

10.3. ON resistance test circuit and graphs







- (1)  $T_{amb} = 125\text{ °C}$ .
- (2)  $T_{amb} = 85\text{ °C}$ .
- (3)  $T_{amb} = 25\text{ °C}$ .
- (4)  $T_{amb} = -40\text{ °C}$ .

Fig. 13. ON resistance as a function of input voltage;  $V_{CC} = 5.0\text{ V}$



## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 17.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	nYn to nZ or nZ to nYn; see Fig. 14 [2][3]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	2	-	3.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	1.2	-	2.0	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	1.0	-	1.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	1.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.6	-	1.0	ns
$t_{en}$	enable time	nS to nYn; see Fig. 15 [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1	8.7	24	1	26.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1	5.3	14	1	15.5	ns
		$V_{CC} = 2.7 \text{ V}$	1	4.9	14	1	15.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0.5	4	7.6	0.5	8.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	3	5.7	0.5	6.6	ns
$t_{dis}$	disable time	nS to nYn; see Fig. 15 [5]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.5	6	13	2.5	14.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2	4.4	7.5	2	8.5	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	4.2	7.5	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.6	5.3	1.5	6	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.8	2.9	3.8	0.8	4.5	ns
$t_{b-m}$	break-before-make time	$C_L = 35 \text{ pF}$ ; $R_L = 50 \Omega$ ; see Fig. 16 [6]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0.5	-	-	0.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.5	-	-	0.5	-	ns

[1] Typical values are measured at  $T_{amb} = 25 \text{ °C}$  and nominal  $V_{CC}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

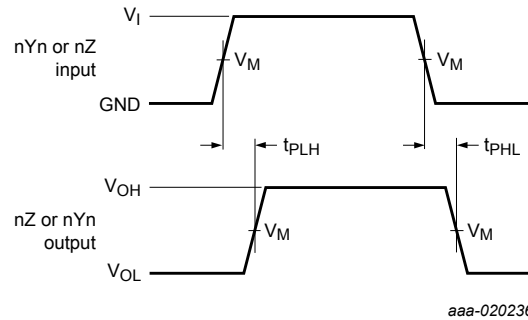
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[5]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[6] Break-before-make specified by design.

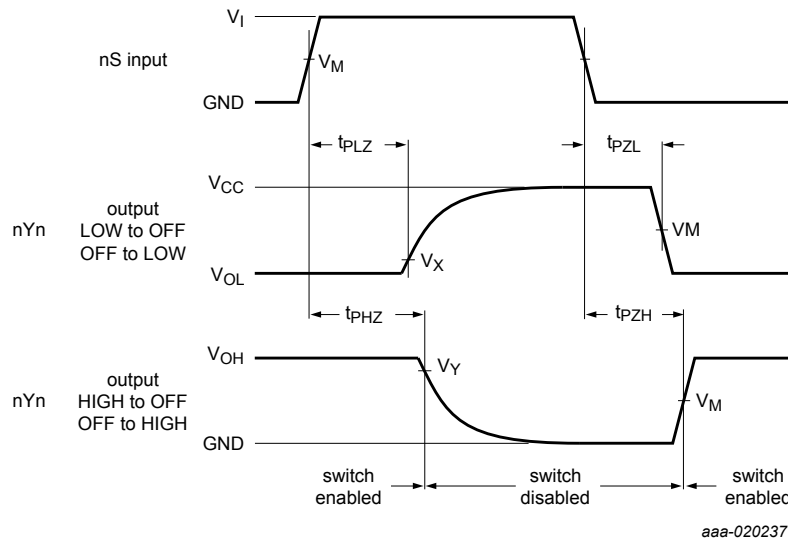
11.1. Waveforms and test circuits



Measurement points are given in [Table 10](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 14. Input (nYn or nZ) to output (nZ or nYn) propagation delays**



Measurement points are given in [Table 10](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 15. Enable and disable times**

**Table 10. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.65 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

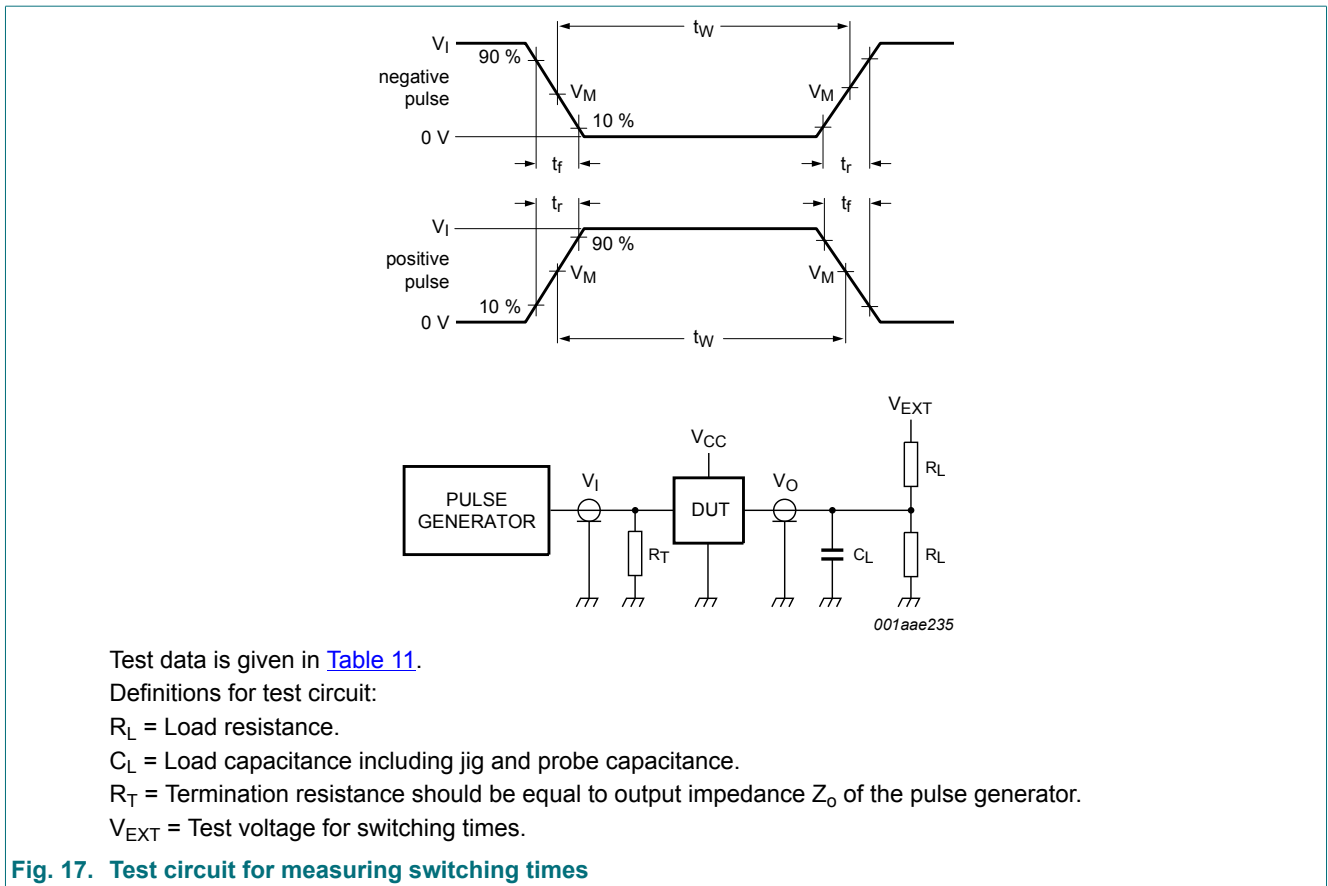
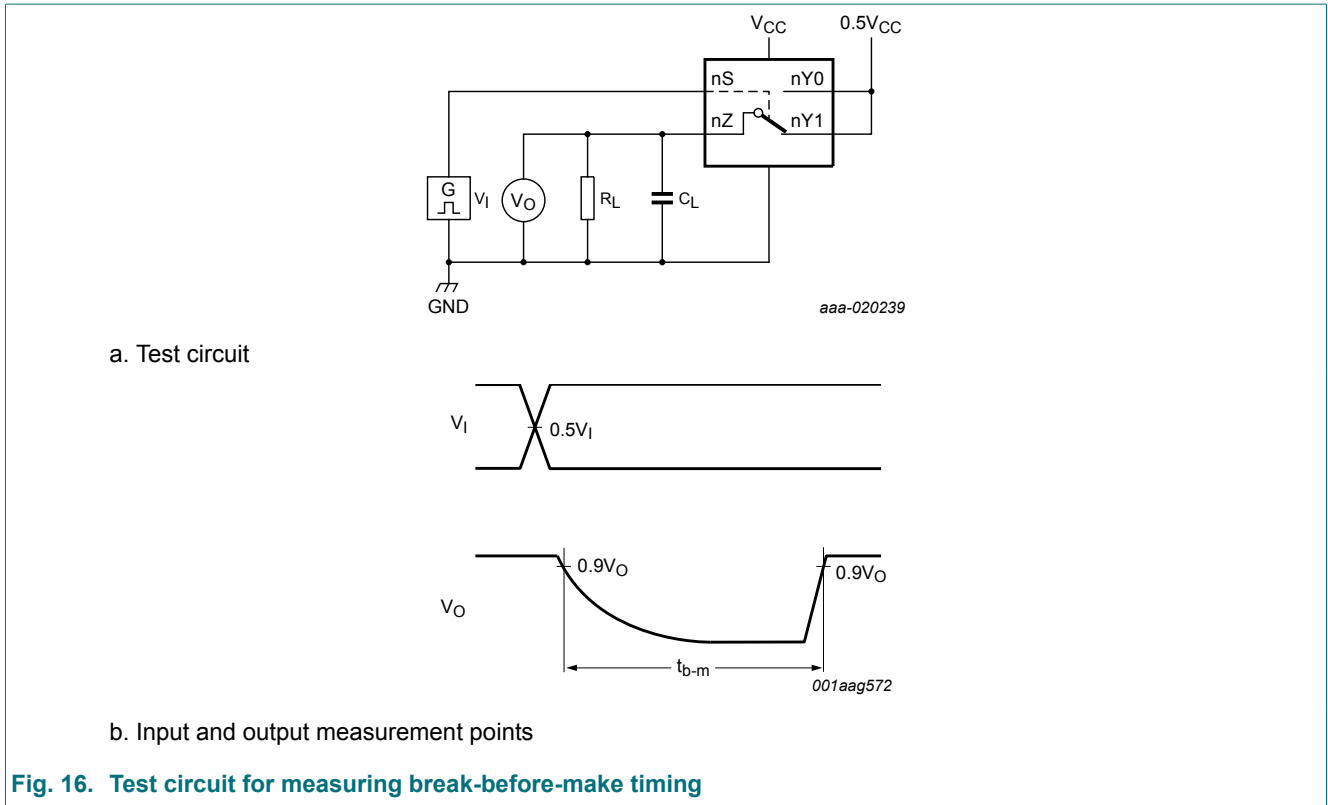


Table 11. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$
2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$
3 V to 3.6 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	GND	$2V_{CC}$

## 11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25$  °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 600$ Hz to 20 kHz; $R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $V_I = 0.5$ V (p-p); see Fig. 18				
		$V_{CC} = 1.65$ V	-	0.260	-	%
		$V_{CC} = 2.3$ V	-	0.078	-	%
		$V_{CC} = 3.0$ V	-	0.078	-	%
		$V_{CC} = 4.5$ V	-	0.078	-	%
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50$ $\Omega$ ; see Fig. 19				
		$V_{CC} = 1.65$ V	-	200	-	MHz
		$V_{CC} = 2.3$ V	-	300	-	MHz
		$V_{CC} = 3.0$ V	-	300	-	MHz
		$V_{CC} = 4.5$ V	-	300	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	$R_L = 50$ $\Omega$ ; $C_L = 5$ pF; $f_i = 10$ MHz; see Fig. 20				
		$V_{CC} = 1.65$ V	-	-42	-	dB
		$V_{CC} = 2.3$ V	-	-42	-	dB
		$V_{CC} = 3.0$ V	-	-40	-	dB
		$V_{CC} = 4.5$ V	-	-40	-	dB
Xtalk	crosstalk	between switches; $f_i = 10$ MHz; see Fig. 21				
		$V_{CC} = 1.65$ V	-	-54	-	dB
		$V_{CC} = 2.3$ V	-	-54	-	dB
		$V_{CC} = 3.0$ V	-	-54	-	dB
		$V_{CC} = 4.5$ V	-	-54	-	dB
$Q_{inj}$	charge injection	$C_L = 0.1$ nF; $V_{gen} = 0$ V; $R_{gen} = 0$ $\Omega$ ; $f_i = 1$ MHz; $R_L = 1$ M $\Omega$ ; see Fig. 22				
		$V_{CC} = 1.8$ V	-	3.3	-	pC
		$V_{CC} = 2.5$ V	-	4.1	-	pC
		$V_{CC} = 3.3$ V	-	5.0	-	pC
		$V_{CC} = 4.5$ V	-	6.4	-	pC
		$V_{CC} = 5.5$ V	-	7.5	-	pC

11.3. Test circuits

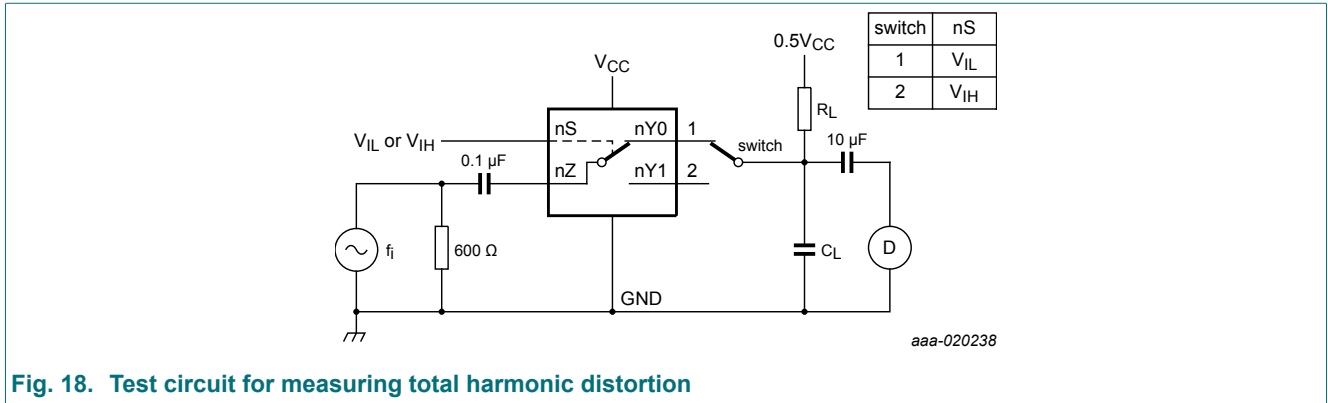
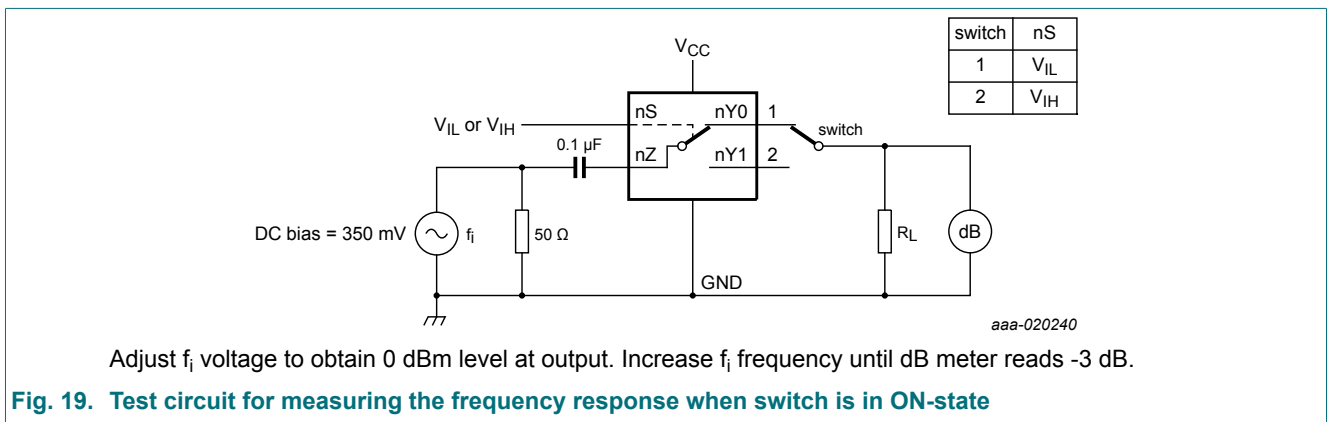
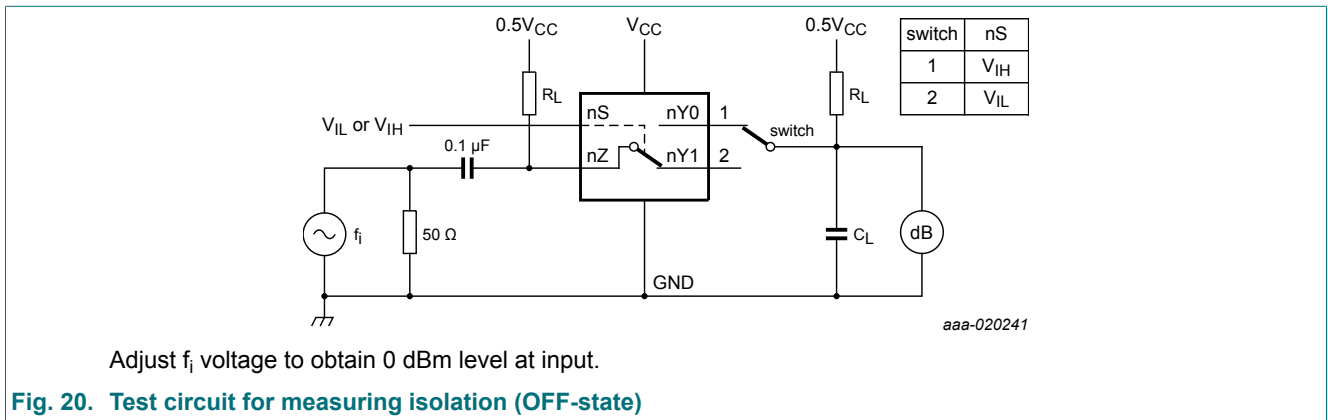


Fig. 18. Test circuit for measuring total harmonic distortion



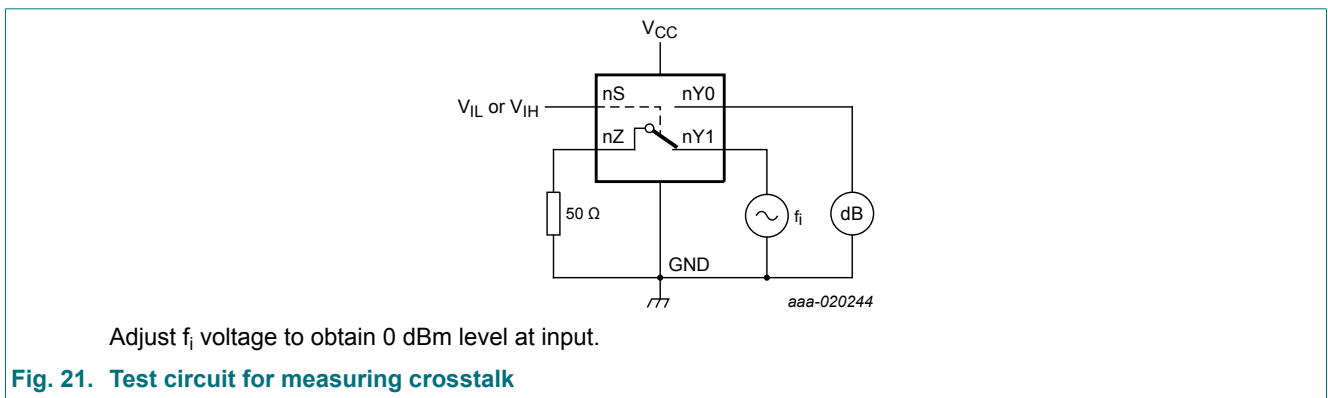
Adjust  $f_i$  voltage to obtain 0 dBm level at output. Increase  $f_i$  frequency until dB meter reads -3 dB.

Fig. 19. Test circuit for measuring the frequency response when switch is in ON-state



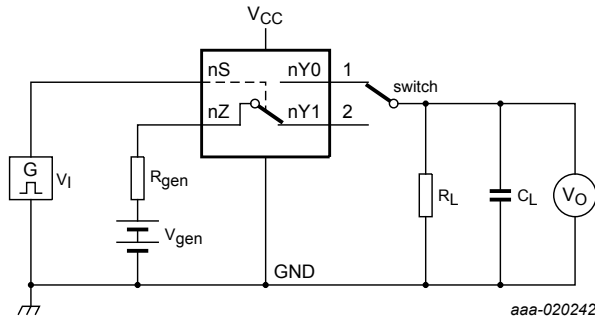
Adjust  $f_i$  voltage to obtain 0 dBm level at input.

Fig. 20. Test circuit for measuring isolation (OFF-state)

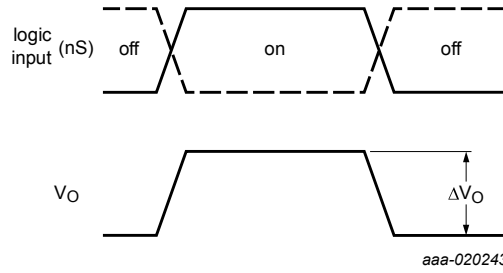


Adjust  $f_i$  voltage to obtain 0 dBm level at input.

Fig. 21. Test circuit for measuring crosstalk



a. Test circuit



b. Input and output pulse definitions

$$Q_{inj} = \Delta V_O \times C_L$$

$\Delta V_O$  = output voltage variation.

$R_{gen}$  = generator resistance.

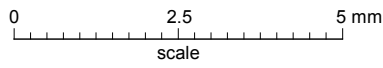
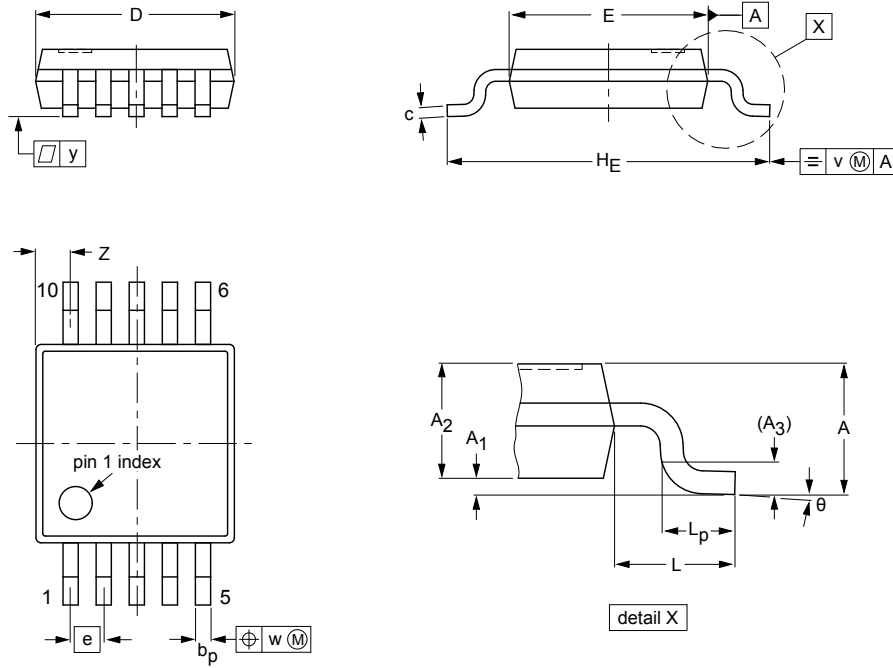
$V_{gen}$  = generator voltage.

Fig. 22. Test circuit for measuring charge injection

12. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

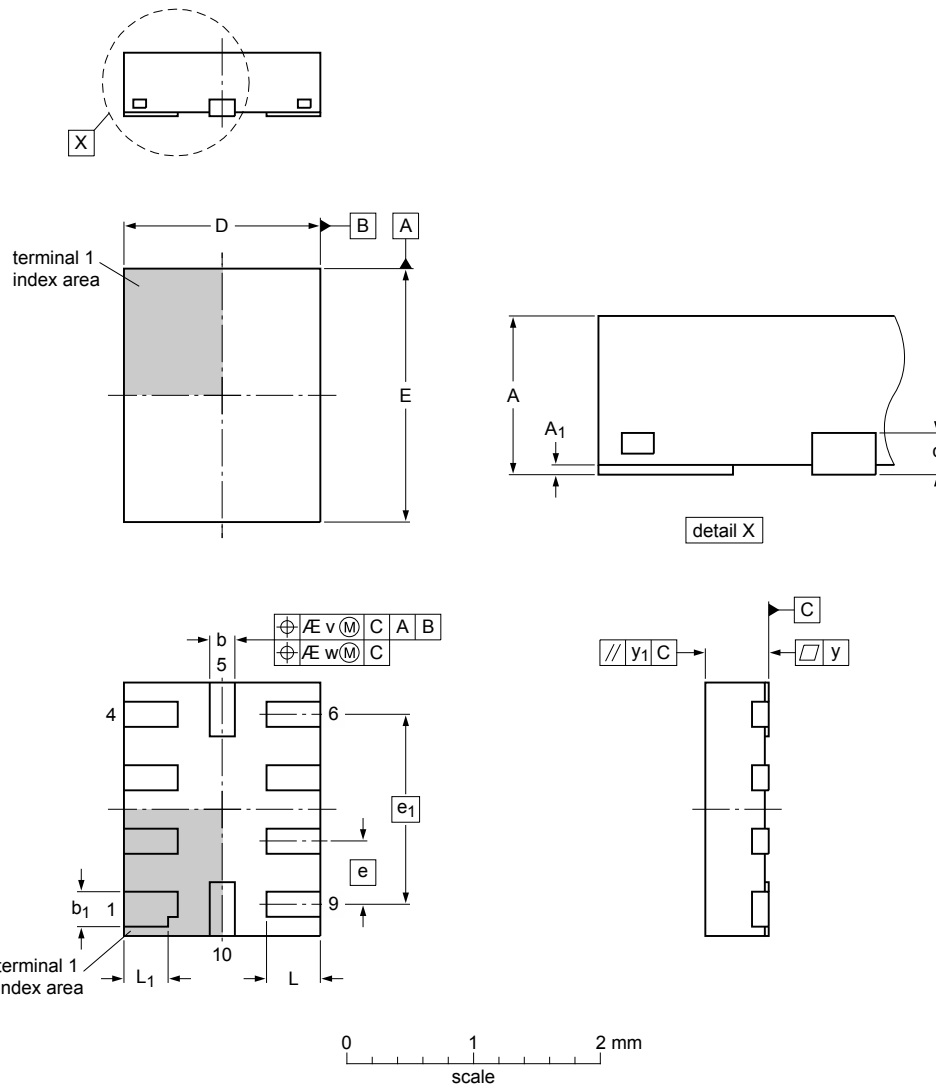
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						-99-07-29 03-02-18

Fig. 23. Package outline SOT552-1 (TSSOP10)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.55 x 2.00 x 0.50 mm

SOT1049-3



Dimensions

Unit <sup>(1)</sup>	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>	v	w	y	y <sub>1</sub>
max	0.5	0.05	0.25	0.33	0.127	1.65	2.1	0.5	1.5	0.48	0.40	0.1	0.05	0.05	0.05
mm	nom		0.20	0.28	1.55	2.0		0.43	0.35						
min		0.00	0.15	0.23	1.45	1.9		0.38	0.30						

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1049-3\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1049-3	---	MO255	---		10-12-06 11-03-30

Fig. 24. Package outline SOT1049-3 (XQFN10)



## 13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G3157 v.3	20190325	Product data sheet	-	74LVC2G3157 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVC2G3157 v.2	20161215	Product data sheet	-	74LVC2G3157 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC2G3157 v.1	20151214	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 25 March 2019