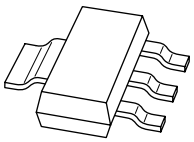


# BT1308W series D

## Triacs logic level

Rev. 01 — 27 February 2008 Product data sheet

## 1. Product profile

### 1.1 General description

Passivated sensitive gate triacs in a SOT223 surface-mountable plastic package

### 1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- Gate triggering in four quadrants
- Direct interfacing to low-power gate drive circuits

### 1.3 Applications

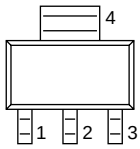
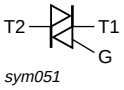
- General purpose switching and phase control
- Low-power AC fan speed controllers

### 1.4 Quick reference data

- $V_{DRM} \leq 400$ V (BT1308W-400D)
- $V_{DRM} \leq 600$ V (BT1308W-600D)
- $I_{TSM} \leq 9$ A (t = 20 ms)
- $I_{GT} \leq 5$ mA
- $I_{GT} \leq 7$ mA (T2– G+)
- $I_{T(RMS)} \leq 0.8$ A

## 2. Pinning information

**Table 1. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| 1 | main terminal 1 (T1) |  |  |
| 2 | main terminal 2 (T2) | | |
| 3 | gate (G) | | |
| 4 | mounting base; main terminal 2 (T2) | | |



**SOT223**



*sym051*

## 3. Ordering information

**Table 2. Ordering information**

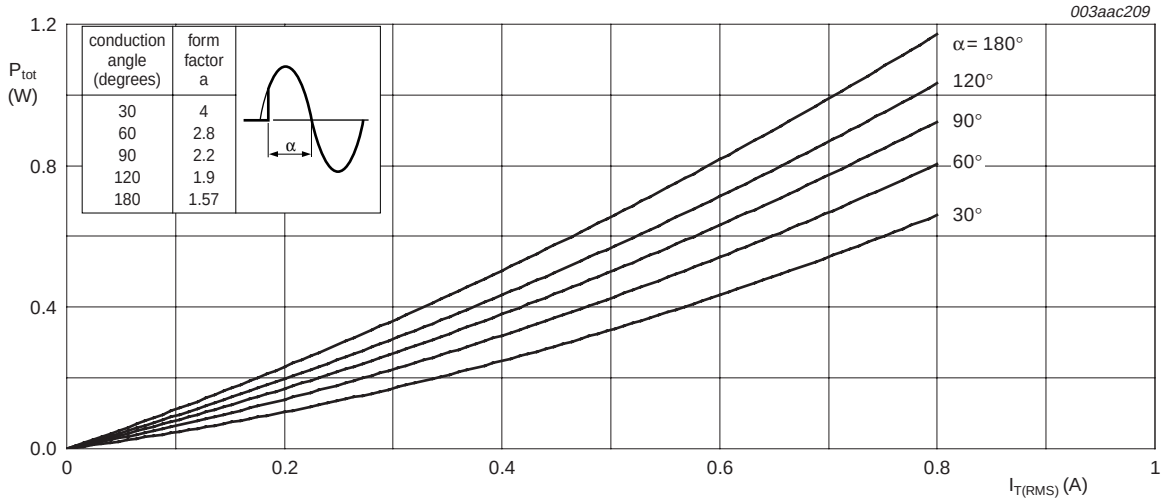
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BT1308W-400D | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |
| BT1308W-600D | | | |

## 4. Limiting values

**Table 3. Limiting values**

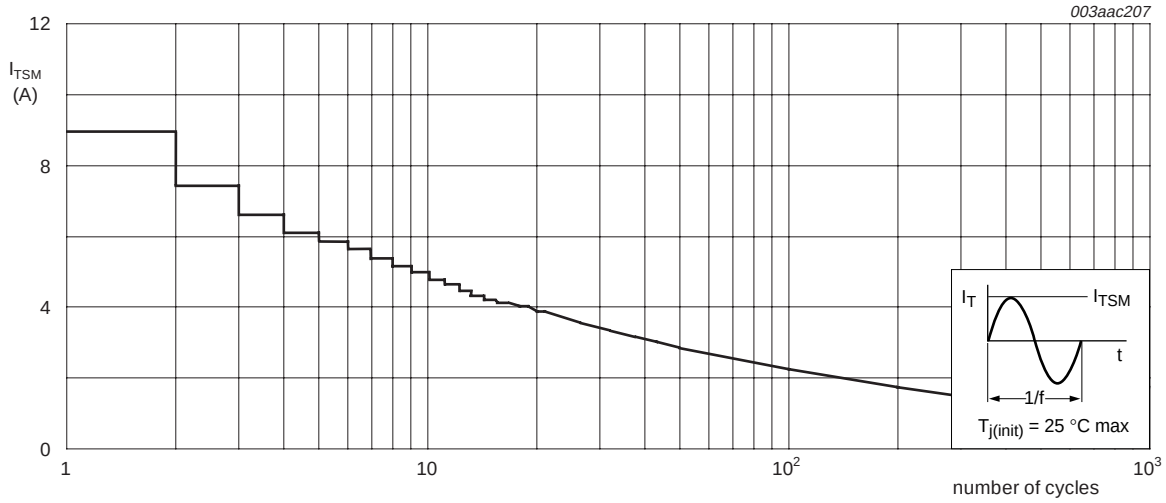
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | BT1308W-400D | - | 400 | V |
| | | BT1308W-600D | - | 600 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq 107.4$ °C; see Figure 4 and 5 | - | 0.8 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3 | | | |
| | | t = 20 ms | - | 9 | A |
| | | t = 16.7 ms | - | 10 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p = 10$ ms | - | 0.32 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_{TM} = 1$ A; $I_G = 20$ mA; $dI_G/dt = 0.2$ A/µs | | | |
| | | T2+ G+ | - | 50 | A/µs |
| | | T2+ G– | - | 50 | A/µs |
| | | T2– G– | - | 50 | A/µs |
| | | T2– G+ | - | 10 | A/µs |
| $I_{GM}$ | peak gate current | | - | 1 | A |
| $P_{GM}$ | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| $T_{stg}$ | storage temperature | | –40 | +150 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |



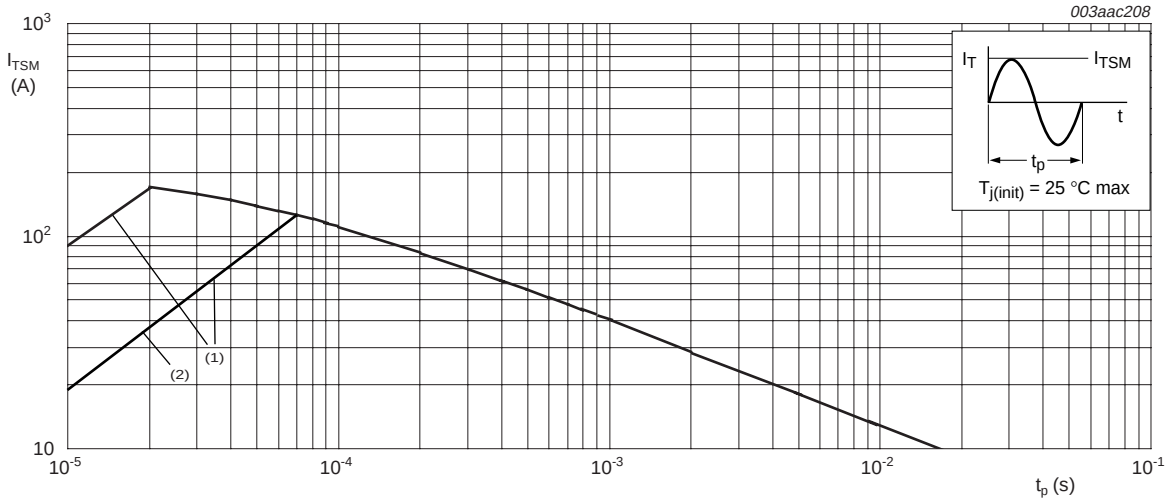

α = conduction angle

**Fig 1. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

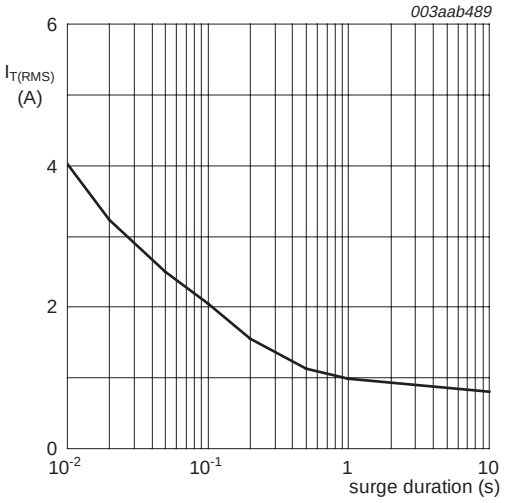



$t_p \leq 20$ ms

(1) $dI_T/dt$ limit

(2) T2– G+ quadrant limit

**Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values**




f = 50 Hz

$T_{sp}$ = 107.4 °C

**Fig 4. RMS on-state current as a function of surge duration; maximum values**

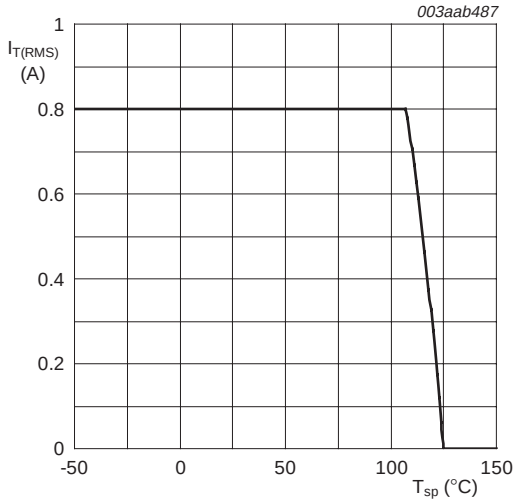



**Fig 5. RMS on-state current as a function of solder point temperature; maximum values**

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle; see Figure 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | full cycle | | | | |
| | | for minimum footprint; see Figure 13 | - | 156 | - | K/W |
| | | for pad area; see Figure 14 | - | 70 | - | K/W |

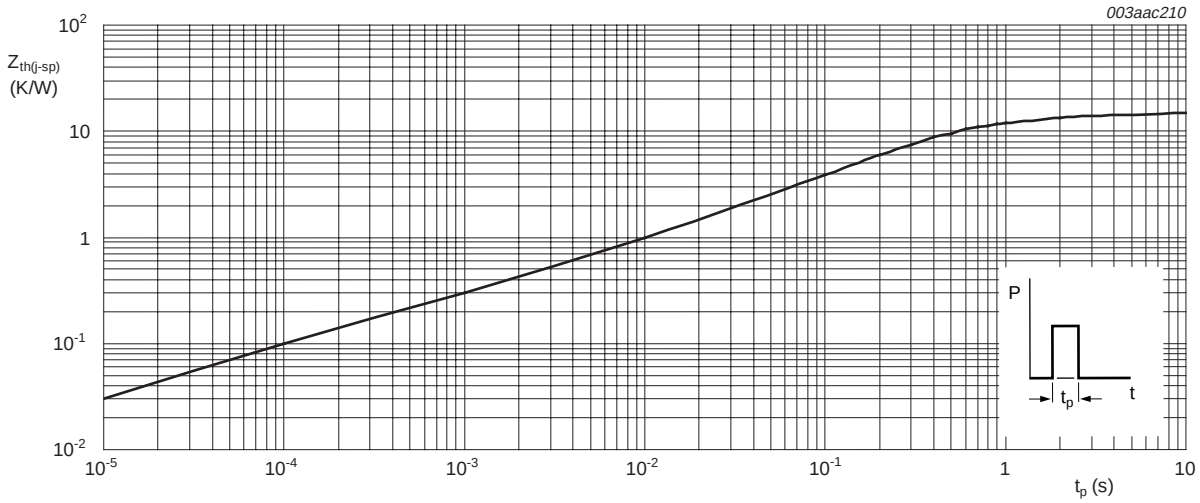



**Fig 6. Transient thermal impedance from junction to solder point as a function of pulse width**

## 6. Characteristics

**Table 5. Characteristics**

*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; see Figure 8 | | | | |
| | | T2+ G+ | - | 1 | 5 | mA |
| | | T2+ G– | - | 2 | 5 | mA |
| | | T2– G– | - | 2 | 5 | mA |
| | | T2– G+ | - | 4 | 7 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; see Figure 10 | | | | |
| | | T2+ G+ | - | 1 | 10 | mA |
| | | T2+ G– | - | 5 | 10 | mA |
| | | T2– G– | - | 1 | 10 | mA |
| | | T2– G+ | - | 2 | 10 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $I_G$ = 0.1 A; see Figure 11 | - | 1 | 10 | mA |
| $V_T$ | on-state voltage | $I_T$ = 0.85 A; see Figure 9 | - | 1.35 | 1.6 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; see Figure 7 | - | 0.9 | 2 | V |
| | | $V_D = V_{DRM}$; $I_T$ = 0.1 A; $T_j$ = 110 °C | 0.1 | 0.7 | - | V |
| $I_D$ | off-state current | $V_D = V_{DRM(max)}$; $T_j$ = 125 °C | - | 0.1 | 0.5 | mA |
| **Dynamic characteristics** | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j$ = 110 °C; exponential waveform; gate open circuit | 30 | 45 | - | V/µs |
| $dV_{com}/dt$ | rate of change of commutating voltage | $V_{DM} = V_{DRM(max)}$; $T_j$ = 50 °C; $I_{TM}$ = 0.84 A; $dI_{com}/dt$ = 0.3 A/ms | - | 5 | - | V/µs |
| $t_{gt}$ | gate-controlled turn-on time | $I_{TM}$ = 1 A; $V_D = V_{DRM(max)}$; $I_G$ = 25 mA; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

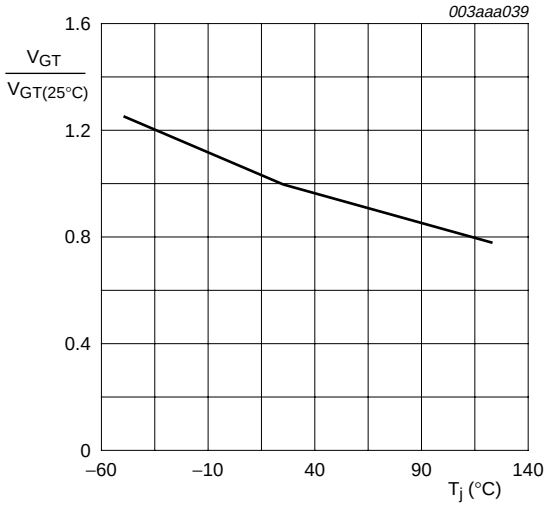
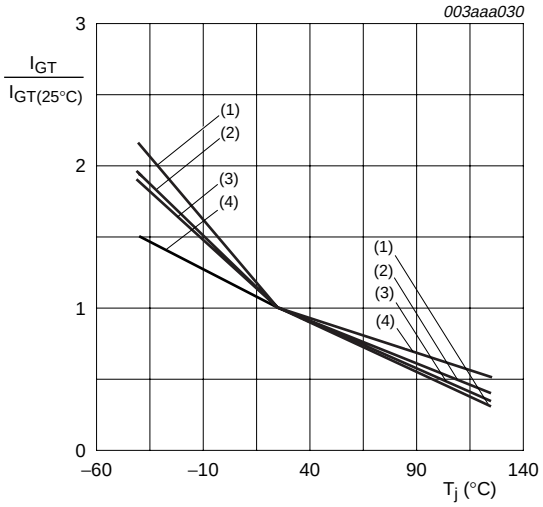
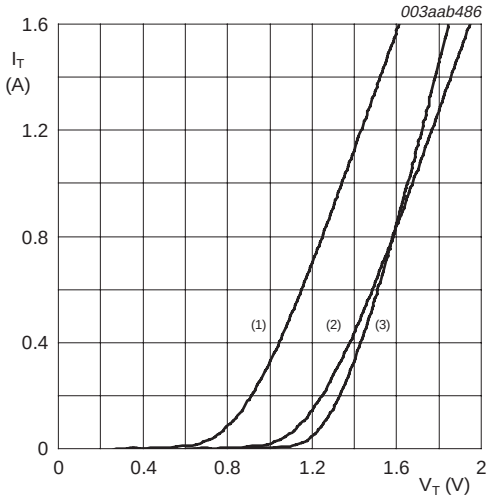



**Fig 7. Normalized gate trigger voltage as a function of junction temperature**




(1) T2+ G+
(2) T2− G+
(3) T2− G−
(4) T2+ G−

**Fig 8. Normalized gate trigger current as a function of junction temperature**




$V_o$ = 1.171 V

$R_s$ = 0.5125 Ω

(1) $T_j$ = 125 °C; typical values

(2) $T_j$ = 125 °C; maximum values

(3) $T_j$ = 25 °C; maximum values

**Fig 9. On-state current as a function of on-state voltage**

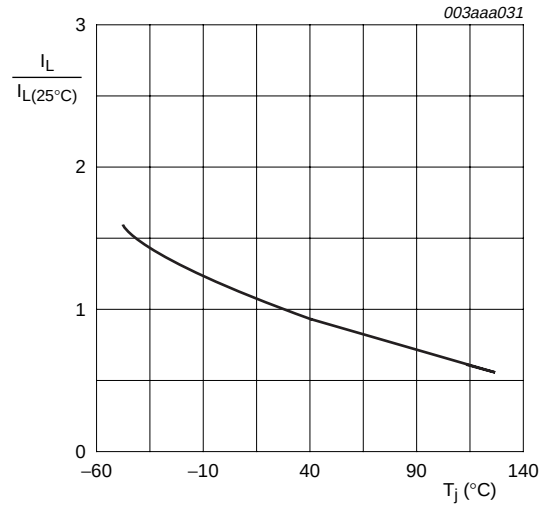



**Fig 10. Normalized latching current as a function of junction temperature**

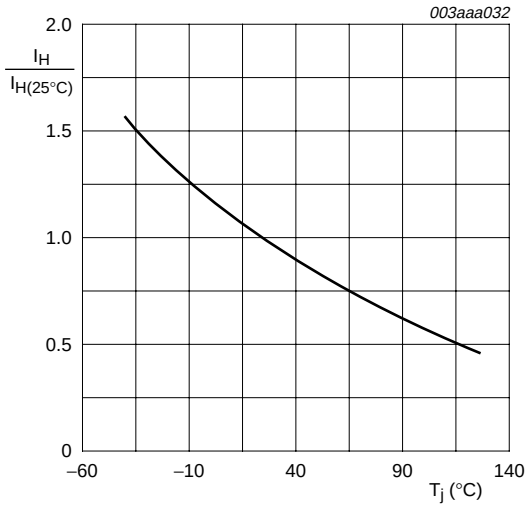
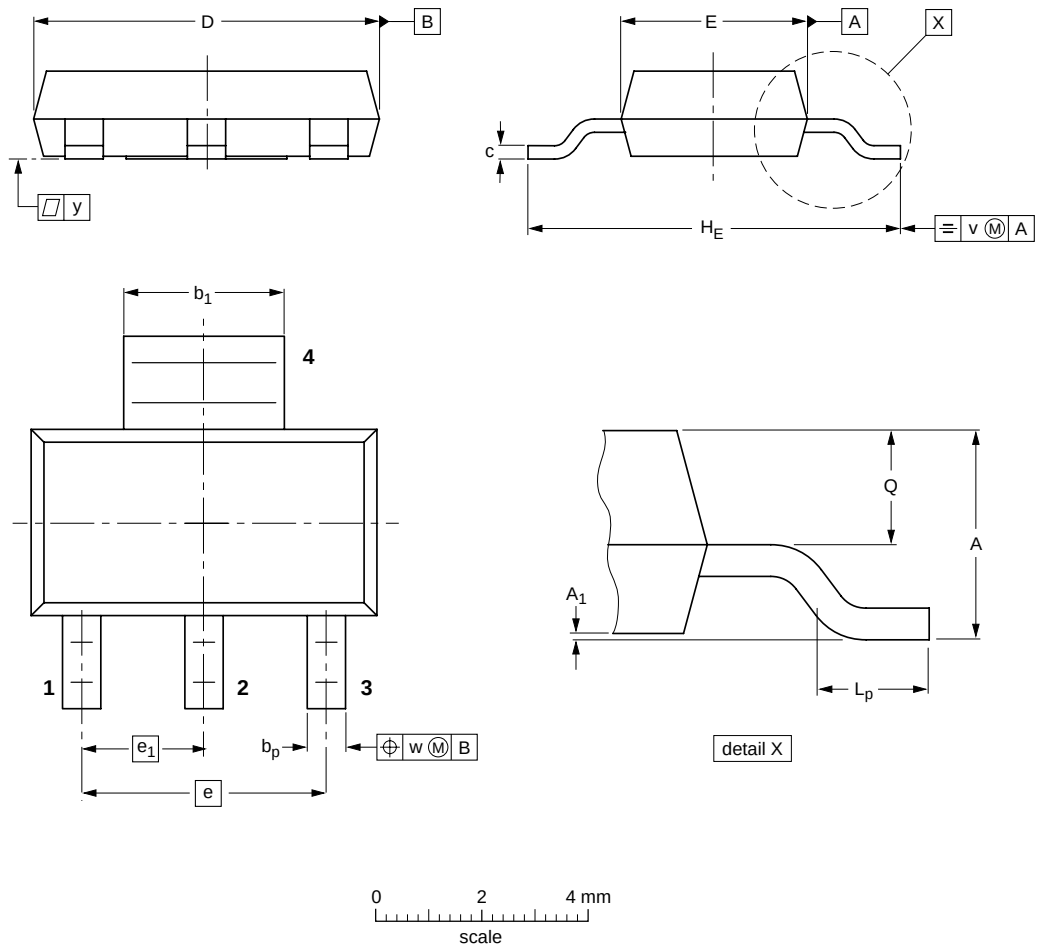



**Fig 11. Normalized holding current as a function of junction temperature**

## 7. Package outline

**Plastic surface-mounted package with increased heatsink; 4 leads** **SOT223**



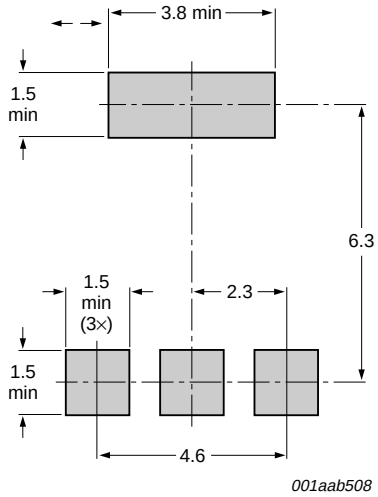

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | $b_1$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.8<br>1.5 | 0.10<br>0.01 | 0.80<br>0.60 | 3.1<br>2.9 | 0.32<br>0.22 | 6.7<br>6.3 | 3.7<br>3.3 | 4.6 | 2.3 | 7.3<br>6.7 | 1.1<br>0.7 | 0.95<br>0.85 | 0.2 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT223 | | | SC-73 | | | ~~04-11-10~~<br>06-03-16 |

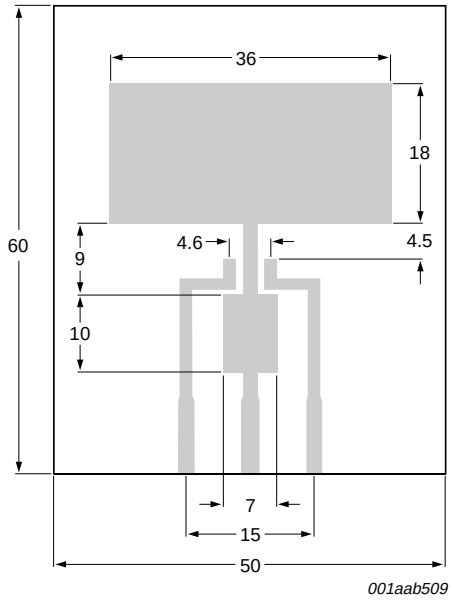
**Fig 12. Package outline SOT223 (SC-73)**

## 8. Mounting




All dimensions are in mm.

**Fig 13. Minimum footprint SOT223**




All dimensions are in mm.

Printed circuit board: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

**Fig 14. Printed circuit board pad area SOT223**

## 9. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BT1308W_SER_D_1 | 20080227 | Product data sheet | - | - |

# 10. Legal information

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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