

BLF248

VHF push-pull power MOS transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

IMPORTANT NOTICE

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As of December 7th, 2015 BL RF Power of NXP Semiconductors will operate as an independent company under the new trade name Ampleon, which will be used in future data sheets together with new contact details.

In data sheets, where the previous Philips references is mentioned, please use the new links as shown below.

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Thank you for your cooperation and understanding,

Ampleon

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FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

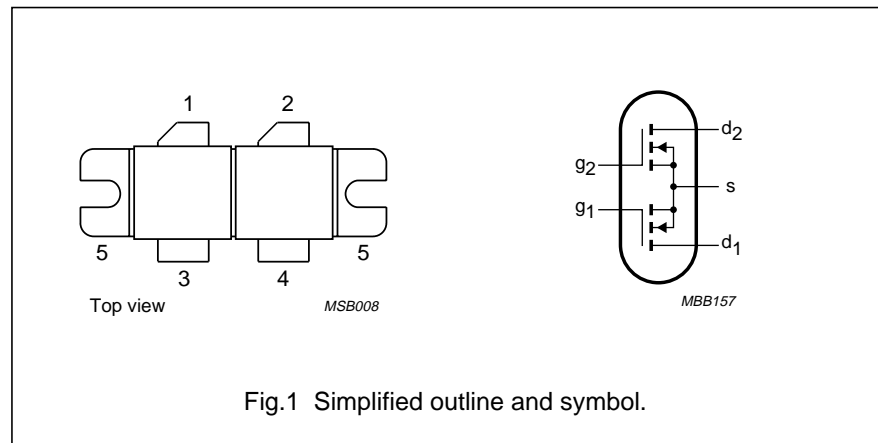
Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262 A1 balanced flange package, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262 A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION



CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25\text{ }^\circ\text{C}$ in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
class-AB	225	28	300	>10	>55
	175	28	300	typ. 13	typ. 67

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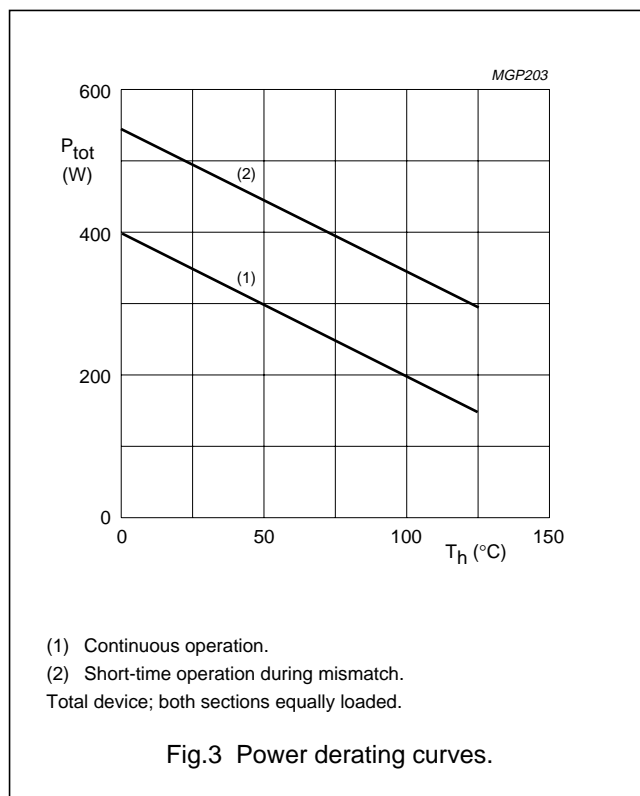
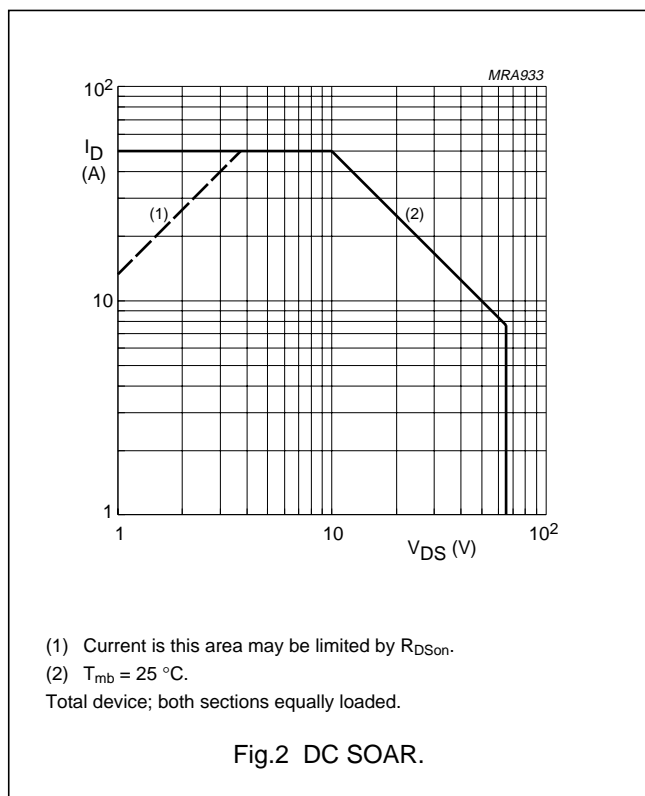
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	± 20	V
I_D	drain current (DC)		–	25	A
P_{tot}	total power dissipation	$T_{mb} \leq 25\text{ }^\circ\text{C}$ total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	0.35	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	0.15	K/W



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CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

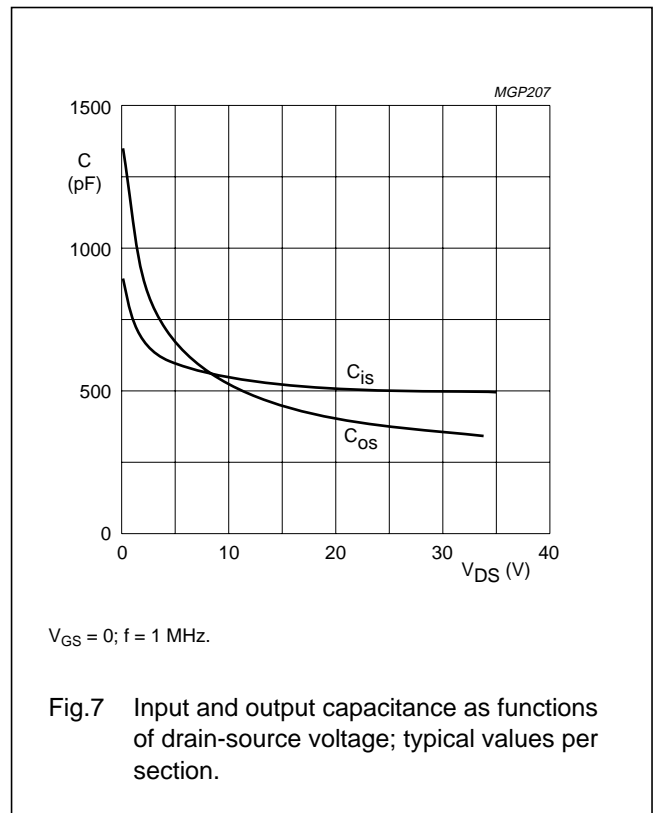
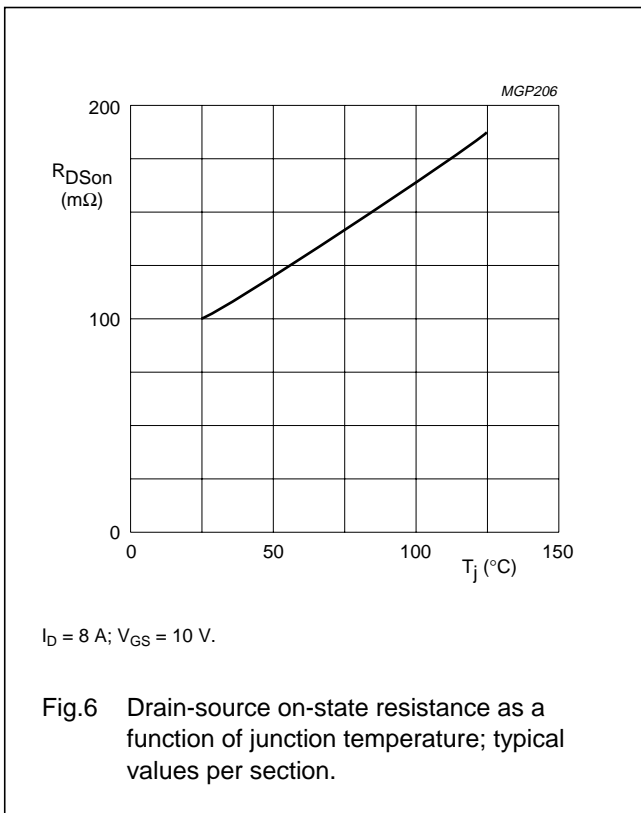
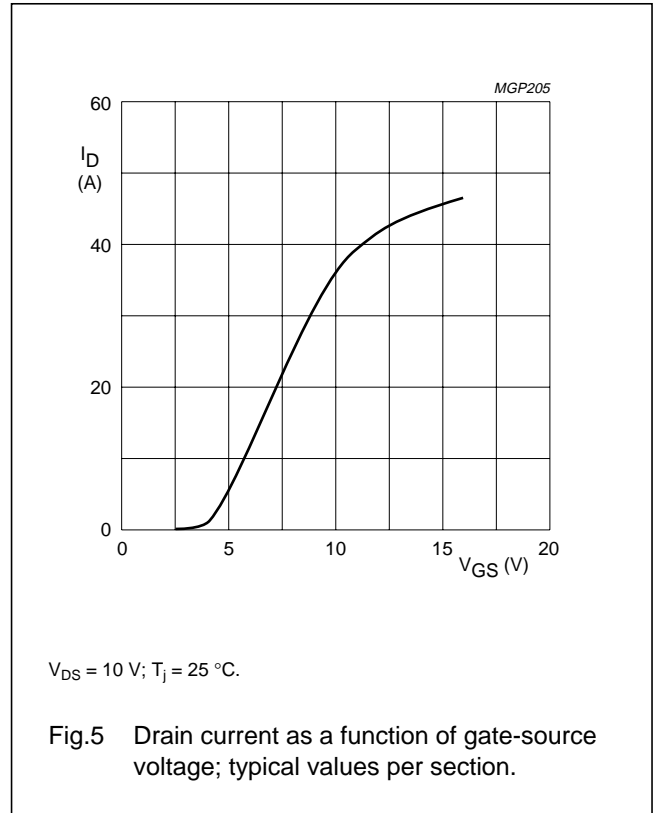
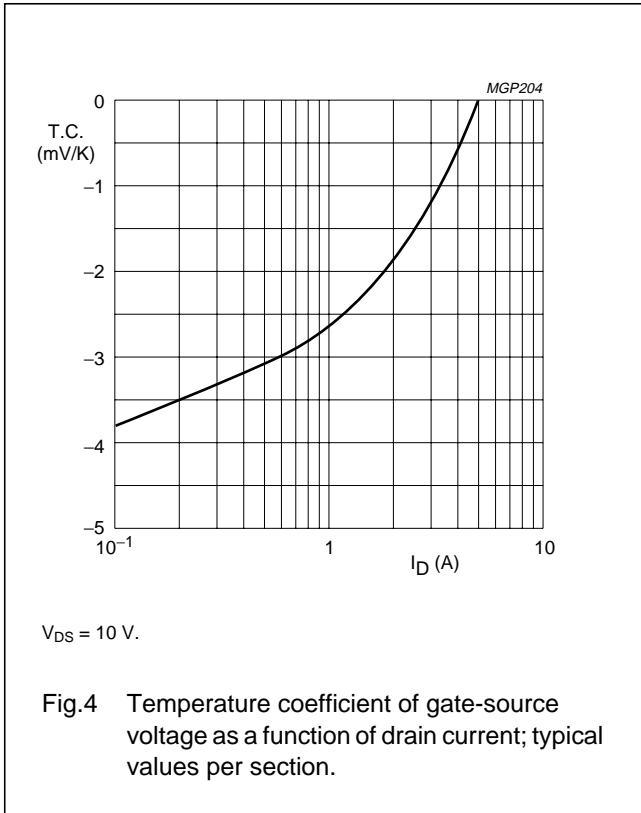
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 100\text{ mA}$	65	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	5	mA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$I_D = 100\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	$I_D = 100\text{ mA}; V_{DS} = 10\text{ V}$	–	–	100	mV
g_{fs}	forward transconductance	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	$I_D = 8\text{ A}; V_{GS} = 10\text{ V}$	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	37	–	A
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	500	–	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	360	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	46	–	pF

 V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

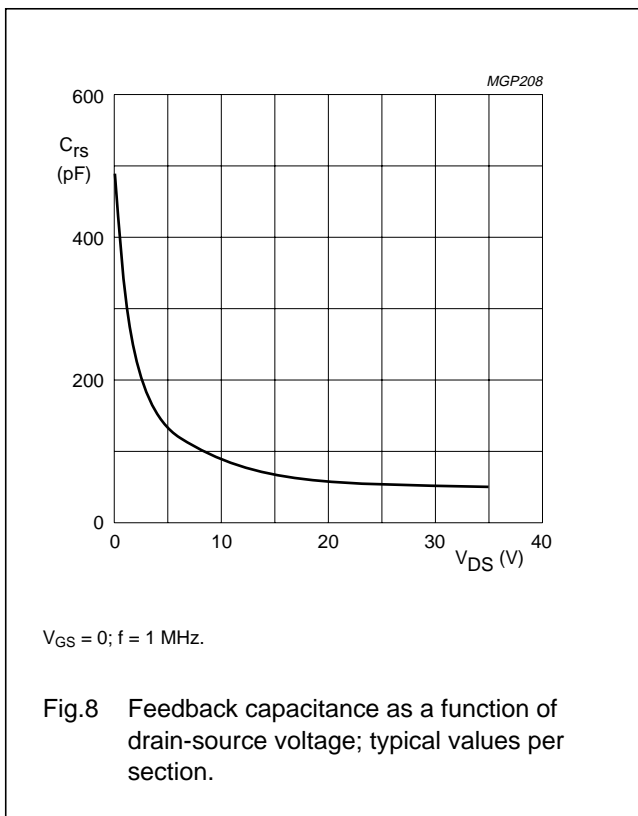
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APPLICATION INFORMATION FOR CLASS-AB OPERATION

$T_h = 25 \text{ }^\circ\text{C}; R_{th\ mb-h} = 0.15 \text{ K/W}$, unless otherwise specified.

RF performance in a linear amplifier in a common source class-AB circuit.

$R_{GS} = 536 \text{ } \Omega$ per section; optimum load impedance per section = $0.79 - j0.11 \text{ } \Omega$.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
class-AB	225	28	300	>10 typ. 11.5	>55 typ. 65
	175	28	300	typ. 13	typ. 67

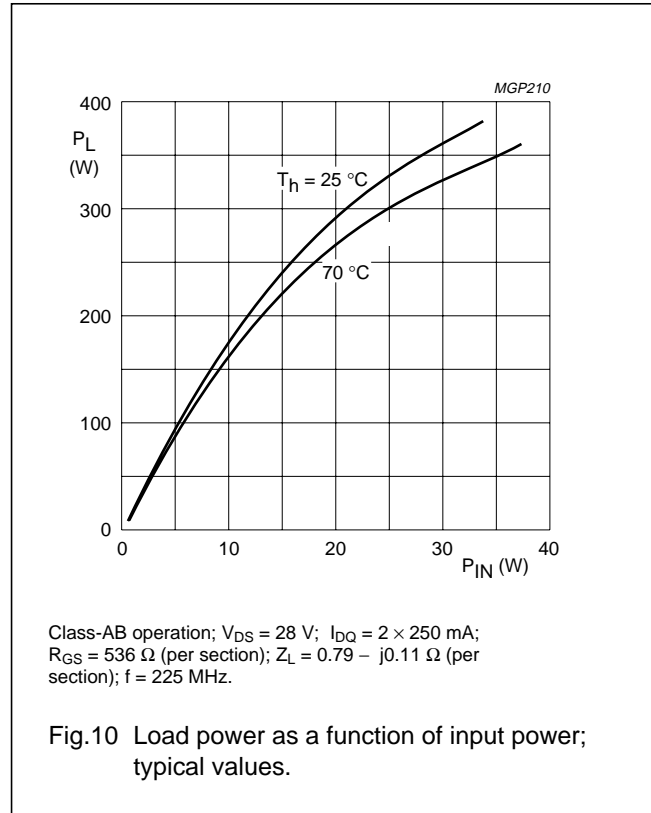
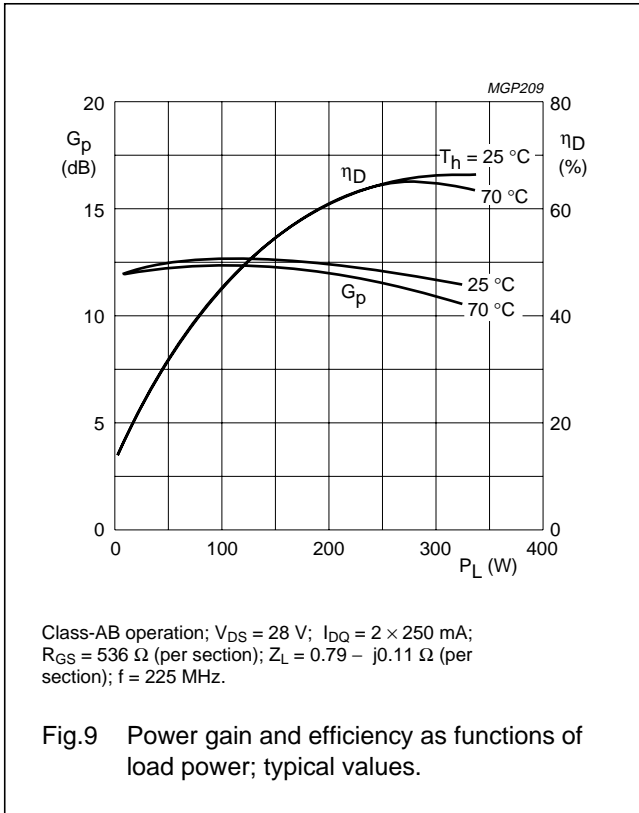
Ruggedness in class-AB operation

The BLF248 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 50$ through all phases under the following conditions:

$V_{DS} = 28 \text{ V}; f = 225 \text{ MHz}$ at rated output power.

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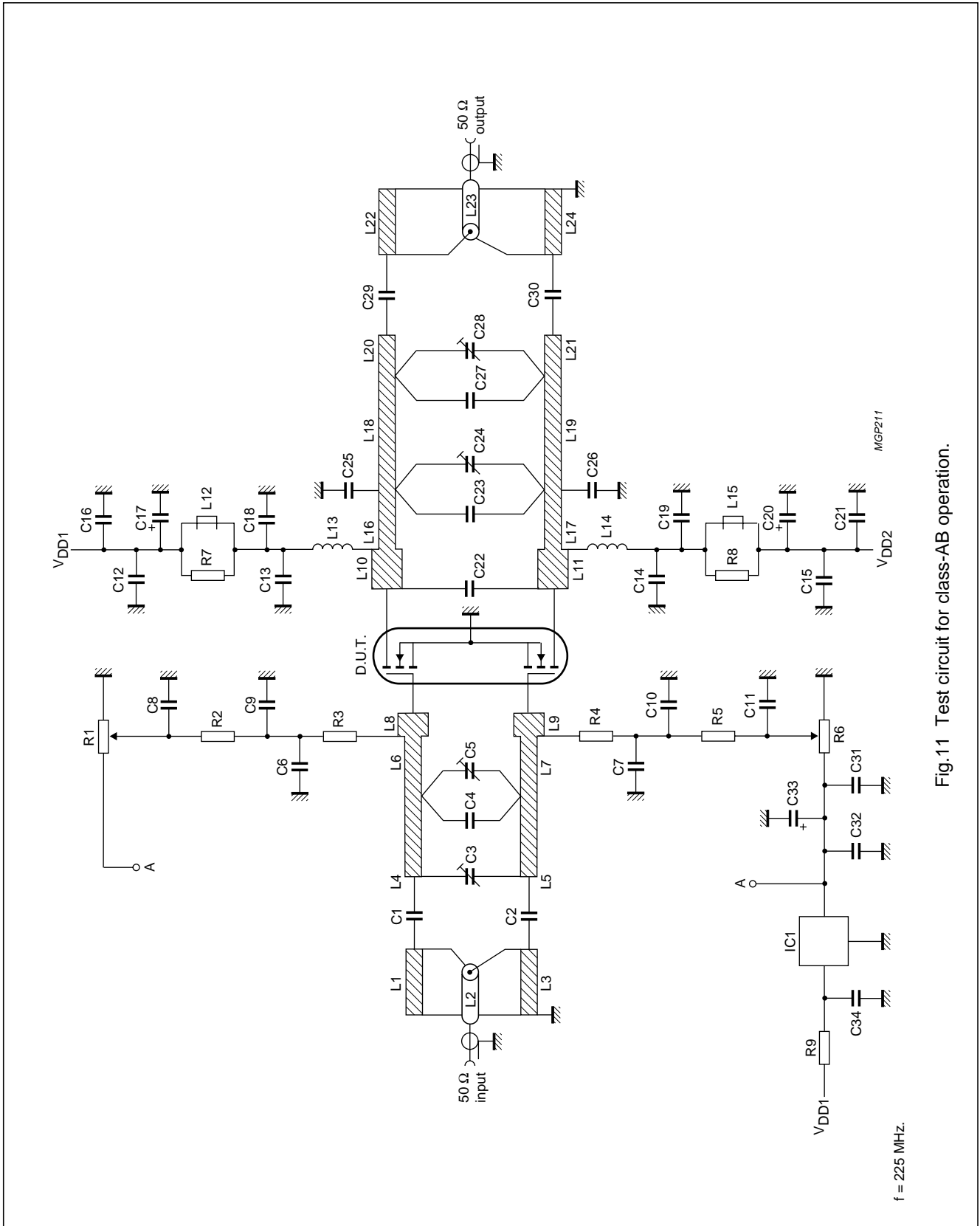


Fig.11 Test circuit for class-AB operation.

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List of components class-AB test circuit; (see Figs 11 and 12)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	2×56 pF + 18 pF in parallel, 500 V		
C3	film dielectric trimmer	2 to 9 pF		2222 809 09005
C4	multilayer ceramic chip capacitor; note 1	47 pF, 500 V		
C5	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6, C7, C9, C10, C12, C15, C31, C34	multilayer ceramic chip capacitor; note 1	1 nF, 500 V		
C8, C11, C16, C21, C32	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C13, C14, C18, C19	multilayer ceramic chip capacitor; note 1	510 pF, 500 V		
C17, C20, C33	electrolytic capacitor	10 μ F, 63 V		
C22	multilayer ceramic chip capacitor; note 1	82 pF, 500 V		
C23	multilayer ceramic chip capacitor; note 1	10 pF + 30 pF in parallel, 500 V		
C24, C28	film dielectric trimmer	2 to 18 pF		2222 809 09006
C25, C26	multilayer ceramic chip capacitor; note 1	39 pF + 47 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor; note 1	18 pF, 500 V		
C29, C30	multilayer ceramic chip capacitor; note 1	3×100 pF in parallel, 500 V		
L1, L3, L22, L24	stripline; note 2	50 Ω	4.8 \times 80 mm	
L2, L23	semi-rigid cable; note 3	50 Ω	ext. dia. 3.6 mm ext. conductor length 80 mm	
L4, L5	stripline; note 2	43 Ω	6 \times 32.5 mm	
L6, L7, L10, L11	stripline; note 2	43 Ω	6 \times 10.5 mm	
L8, L9	stripline; note 2	43 Ω	6 \times 3 mm	
L12, L15	grade 3B Ferroxcube wide-band HF choke	2 in parallel		4312 020 36642
L13, L14	2 turns enamelled 1.6 mm copper wire	25 nH	int. dia. 5 mm leads 2 \times 7 mm space 2.5 mm	
L16, L17	stripline; notes 2 and 4	43 Ω	6 \times 3 mm	
L18, L19	stripline; notes 2 and 4	43 Ω	6 \times 35 mm	
L20, L21	stripline; notes 2 and 4	43 Ω	6 \times 9 mm	
R1, R6	10 turns potentiometer	50 k Ω		
R2, R5	0.4 W metal film resistor	1 k Ω		

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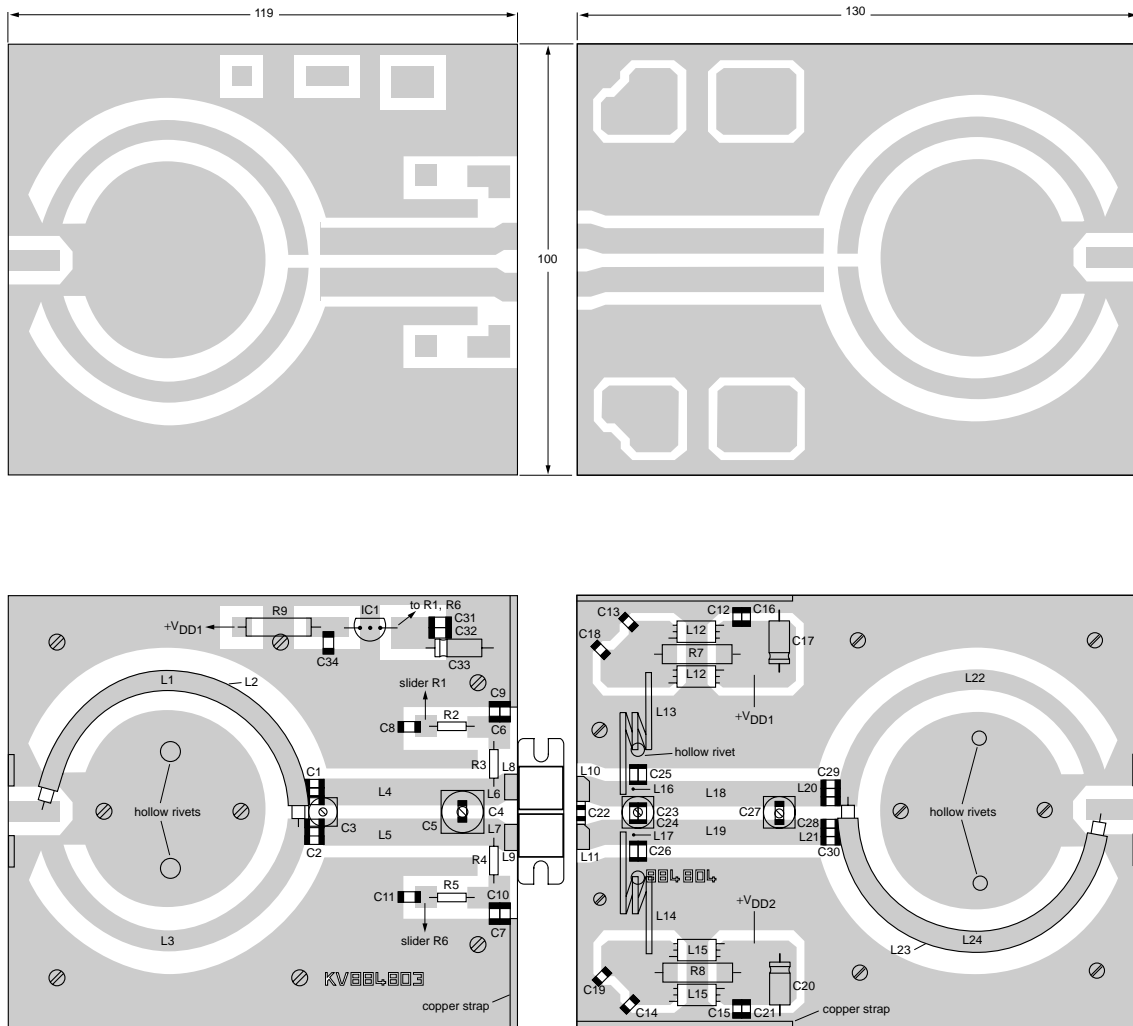
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
R3, R4	0.4 W metal film resistor	536 Ω		
R7, R8	1 W metal film resistor	10 $\Omega \pm 5\%$		
R9	1 W metal film resistor	3.16 k Ω		
IC1	78L05 voltage regulator			

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 to L11, L16 to L22 and L24 are micro-striplines on a double copper-clad printed-circuit board, with glass microfibre PTFE dielectric ($\epsilon_r = 2.2$), thickness $\frac{1}{16}$ inch, thickness of copper sheet $2 \times 35 \mu\text{m}$.
3. L2 and L23 are soldered on striplines L1 and L24 respectively.
4. A copper strap, thickness 0.8 mm, is soldered on striplines L16 to L21.

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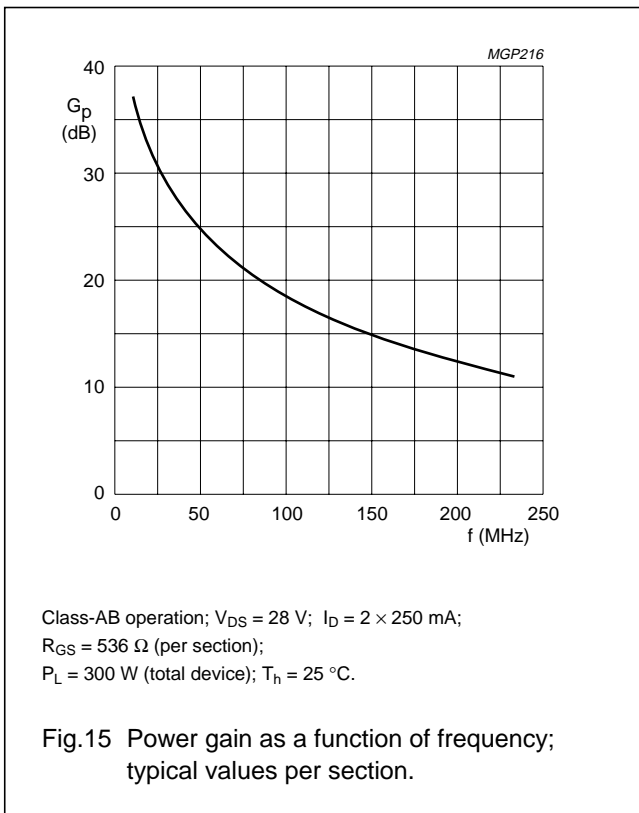
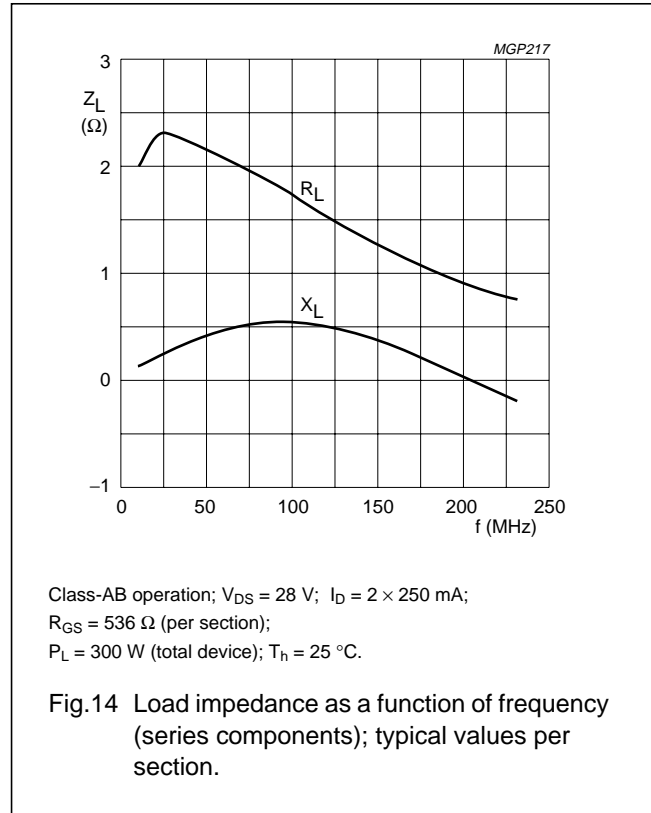
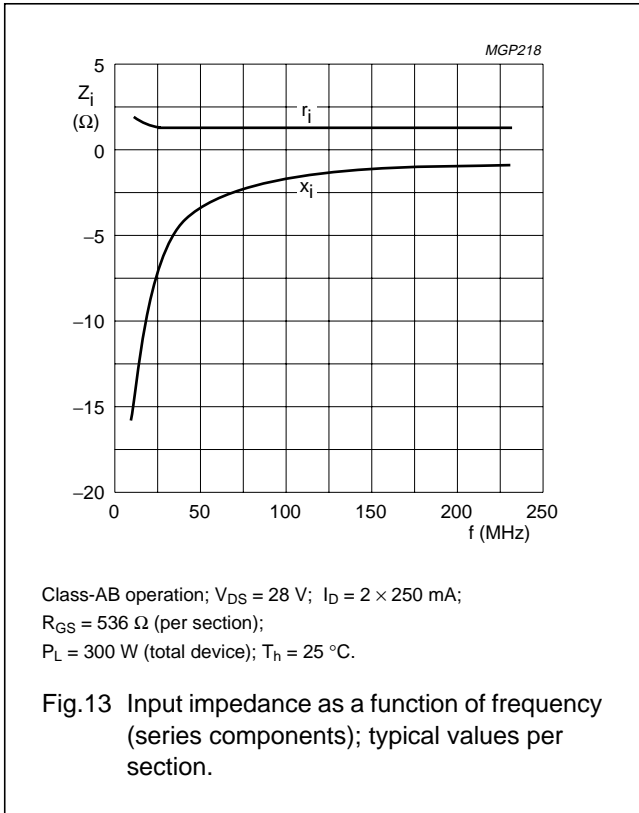
Dimensions in mm.

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.12 Component layout for 225 MHz class-AB test circuit.

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BLF248 scattering parameters $V_{DS} = 28 \text{ V}$; $I_D = 250 \text{ mA}$; note 1

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	s ₁₁	∠ Φ	s ₂₁	∠ Φ	s ₁₂	∠ Φ	s ₂₂	∠ Φ
5	0.85	-158.7	22.19	97.0	0.01	-1.4	0.90	168.9
10	0.85	-168.6	11.27	88.5	0.01	20.7	0.85	174.2
20	0.85	-173.2	5.51	79.0	0.01	18.2	0.83	178.2
30	0.86	-174.1	3.57	72.0	0.02	8.2	0.83	-179.8
40	0.87	-174.3	2.56	65.9	0.02	-0.2	0.83	-178.0
50	0.88	-174.4	1.96	60.6	0.02	-7.2	0.85	-176.6
60	0.89	-174.6	1.55	55.7	0.01	-13.1	0.86	-175.8
70	0.90	-174.8	1.26	51.3	0.01	-17.8	0.87	-175.3
80	0.91	-175.1	1.05	47.5	0.01	-21.6	0.89	-175.0
90	0.92	-175.5	0.88	44.0	0.01	-24.6	0.90	-174.9
100	0.93	-175.8	0.76	40.6	0.01	-27.0	0.91	-175.0
125	0.95	-176.7	0.53	33.6	0.01	-30.2	0.93	-175.6
150	0.96	-177.6	0.38	28.9	0.01	-28.2	0.94	-175.6
175	0.97	-178.4	0.30	25.5	0.00	-21.2	0.96	-176.0
200	0.97	-179.2	0.23	22.3	0.00	-5.3	0.97	-176.7
250	0.98	179.4	0.16	18.6	0.00	47.5	0.98	-177.6
300	0.98	178.2	0.11	17.2	0.01	71.9	0.98	-178.5
350	0.98	177.1	0.08	16.7	0.01	78.0	0.99	-179.1
400	0.99	176.2	0.07	18.9	0.01	84.9	0.99	-179.9
450	0.99	175.2	0.05	21.7	0.01	88.1	0.99	179.6
500	0.99	174.2	0.05	26.7	0.01	88.6	0.99	179.0
600	0.99	172.3	0.04	38.3	0.02	89.4	1.00	177.9
700	0.99	170.4	0.03	50.8	0.02	90.0	1.00	176.9
800	0.99	168.6	0.03	63.7	0.03	91.0	1.00	176.0
900	0.99	166.6	0.04	71.0	0.03	91.6	1.00	175.0
1000	0.99	164.7	0.04	77.6	0.04	92.3	1.00	174.1

Note

- For more extensive s-parameters see internet:
<http://www.semiconductors.philips.com/markets/communications/wirelesscommunication/broadcast>

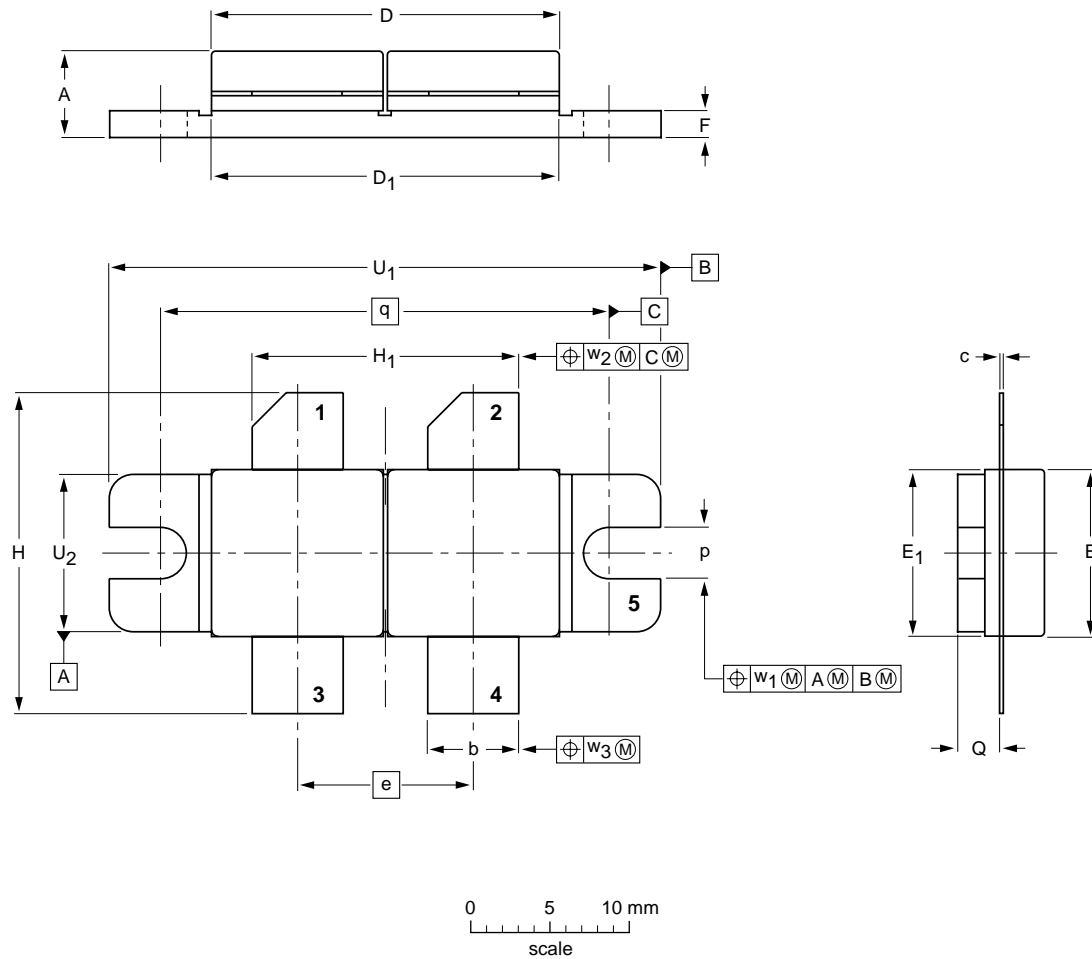
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PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262A1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						99-03-29

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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