74ABT652A

Octal transceiver/register; non-inverting; 3-state

Rev. 02 — 12 March 2010 Product data sheet

1. General description

The 74ABT652A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652A transceiver/register consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin (CPAB or CPBA) goes HIGH. Output Enable (OEAB, $\overline{\text{OEBA}}$) and Select (SAB, SBA) pins are provided for bus management.

2. Features and benefits

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-state outputs
- Live insertion/extraction permitted
- Power-up 3-state
- Power-up reset
- Output capability: +64 mA to –32 mA
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT652AD	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT652ADB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT652APW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Block diagram

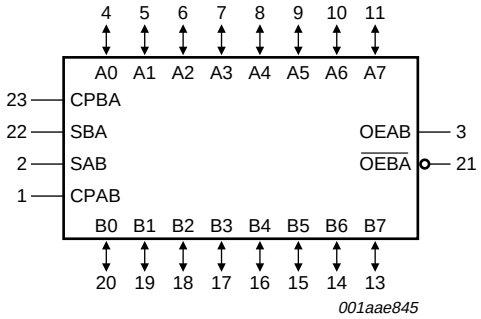


Fig 1. Logic symbol

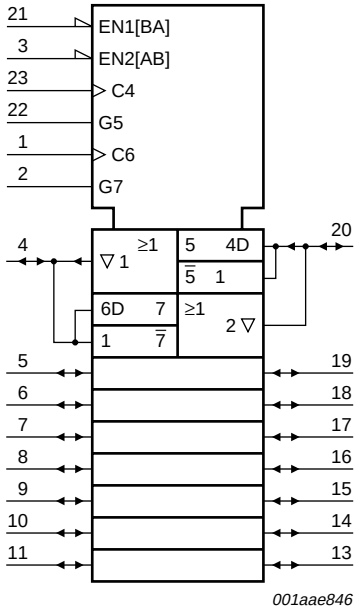


Fig 2. IEC logic symbol

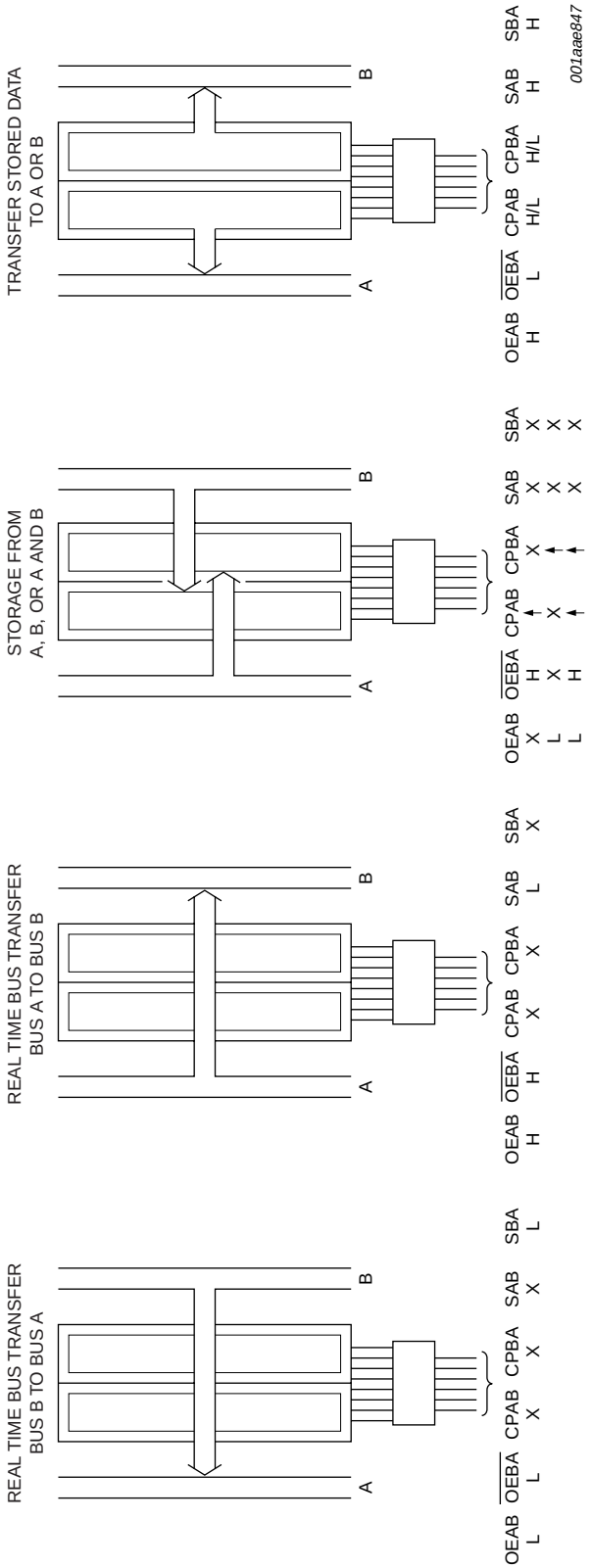


Fig 3. Real time bus transfer and storage

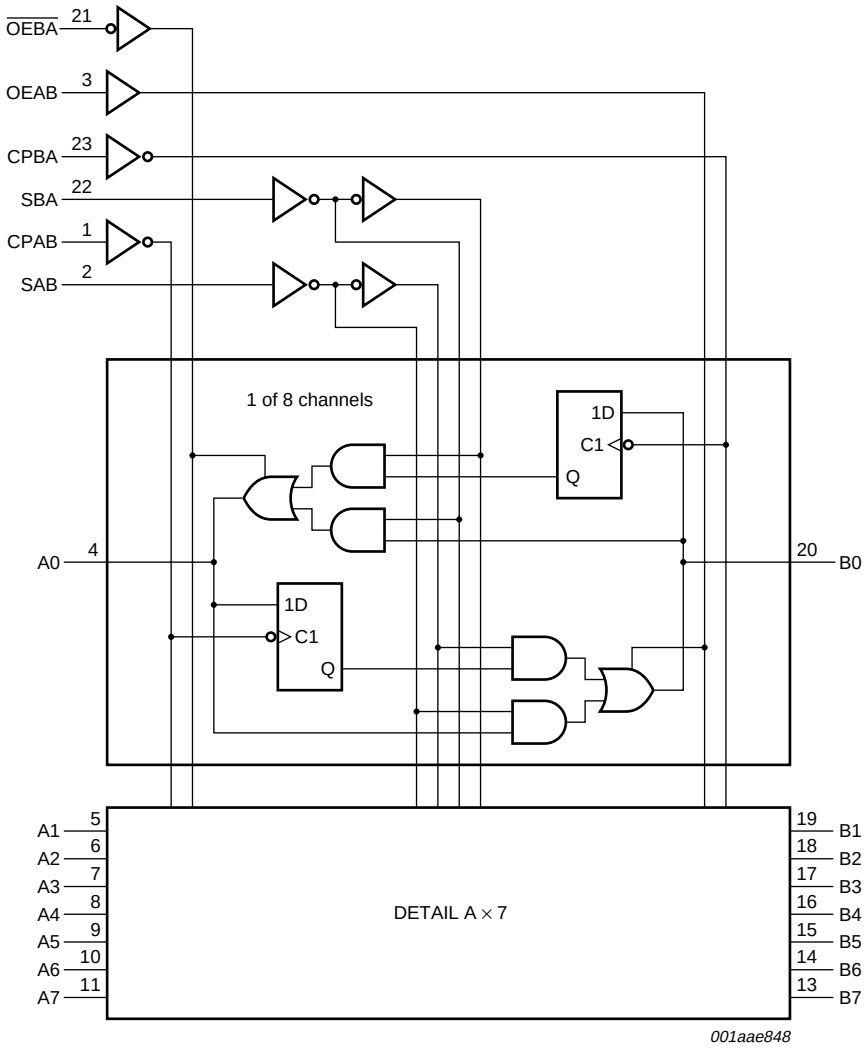


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CPAB	1	A to B clock input
SAB	2	A to B select input
OEAB	3	A to B output enable input
A0, A1, A2, A3, A4, A5, A6, A7	4, 5, 6, 7, 8, 9, 10, 11	data input/output (A side)
GND	12	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	20, 19, 18, 17, 16, 15, 14, 13	data input/output (B side)
$\overline{OEBA}$	21	B to A output enable input (active LOW)
SBA	22	B to A select input
CPBA	23	B to A clock input
V_{CC}	24	positive supply voltage

6. Functional description

6.1 Function table

Table 3. Function table [1]

Inputs						Data I/O		Operating mode
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	An	Bn	
L	H	H or L	H or L	X	X	input	input	isolation
L	H	↑	↑	X	X	input	input	store A and B data
X	H	↑	H or L	X	X	input	unspecified output [2]	store A, hold B
H	H	↑	↑	[3]	X	input	unspecified output [2]	store A in both registers
L	X	H or L	↑	X	X	unspecified output [2]	input	hold A, store B
L	L	↑	↑	X	[3]	unspecified output [2]	input	store B in both registers
L	L	X	X	X	L	output	input	real time B data to A bus
L	L	X	H or L	X	H	output	input	stored B data to A bus
H	H	X	X	L	X	input	output	real time A data to B bus
H	H	H or L	X	H	X	input	output	store A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus; stored B data to A bus

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition.

[2] The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

[3] If both select controls (SAB and SBA) are LOW, then clocks can occur simultaneously. If either select control is HIGH, the clocks must be staggered in order to load both registers.

Figure 3 demonstrates the four fundamental bus-management functions that can be performed with the 74ABT652A.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		–32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		–1.2	–0.9	-	–1.2	-	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = –3 mA		2.5	3.0	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA		3.0	3.5	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	0.3	0.55	-	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V							
		control pins		-	±0.01	±1.0	-	±1.0	µA
		data pins		-	±5	±100	-	±100	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O ≤ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; OEAB, $\overline{OEBA}$ don't care	[2]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
		V_O = 2.7 V		-	5.0	50	-	50	µA
		V_O = 0.5 V		-	–5.0	–50	-	–50	µA
I_{LO}	output leakage current	V_{CC} = 5.5 V; HIGH-state; V_O = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3][5]	–180	–65	–40	–180	–40	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	110	250	-	250	µA
		outputs LOW-state		-	20	30	-	30	mA
		outputs disabled		-	110	250	-	250	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[4]	-	0.3	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	-	-	pF

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 µs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

[5] This data sheet limit may vary among suppliers.

10. Dynamic characteristics

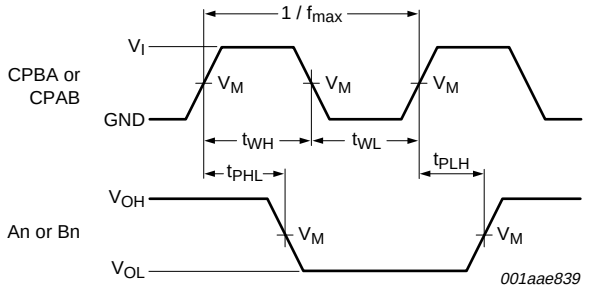
Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 12.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	see Figure 6	125	300	-	125	-	MHz
t_{PLH}	LOW to HIGH propagation delay	CPAB to Bn or CPBA to An; see Figure 6	2.2	3.7	5.1	2.2	5.6	ns
		An to Bn or Bn to An; see Figure 7	1.5	3.0	4.3	1.5	4.8	ns
		SAB to Bn or SBA to An; see Figure 8	1.5	3.5	5.1	1.5	6.5	ns
t_{PHL}	HIGH to LOW propagation delay	CPAB to Bn or CPBA to An; see Figure 6	1.7	4.3	5.1	1.7	5.6	ns
		An to Bn or Bn to An; see Figure 7	1.5	3.6	4.6	1.5	5.4	ns
		SAB to Bn or SBA to An; see Figure 8	1.5	4.2	5.2[1]	1.5	5.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OEBA}$ to An; see Figure 10	2	3.2	4.6	2	5.8	ns
		OEAB to Bn; see Figure 10	2	3.5	6.1	2	6.5	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OEBA}$ to An; see Figure 11	3	4.5	6.8	3	8.5	ns
		OEAB to Bn; see Figure 11	3	4.7	6.5	3	7.4	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OEBA}$ to An; see Figure 10	1.5	3.9	4.7[1]	1.5	5.3[1]	ns
		OEAB to Bn; see Figure 10	1.5	3.8	4.6[1]	1.5	5.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OEBA}$ to An; see Figure 11	1.5	2.9	3.8	1.5	4.1	ns
		OEAB to Bn; see Figure 11	1.5	3.0	4.4	1.5	5.1	ns
$t_{su(H)}$	set-up time HIGH	An to CPAB, Bn to CPBA; see Figure 9	3.0	0.7	-	3.0	-	ns
$t_{su(L)}$	set-up time LOW	An to CPAB, Bn to CPBA; see Figure 9	3.0	0.7	-	3.0	-	ns
$t_{h(H)}$	hold time HIGH	An to CPAB, Bn to CPBA; see Figure 9	0.0	–0.5	-	0.0	-	ns
$t_{h(L)}$	hold time LOW	An to CPAB, Bn to CPBA; see Figure 9	0.0	–0.5	-	0.0	-	ns
t_{WH}	pulse width HIGH	CPAB, CPBA; see Figure 6	4.0	1.0	-	4.0	-	ns
t_{WL}	pulse width LOW	CPAB, CPBA; see Figure 6	4.0	1.0	-	4.0	-	ns

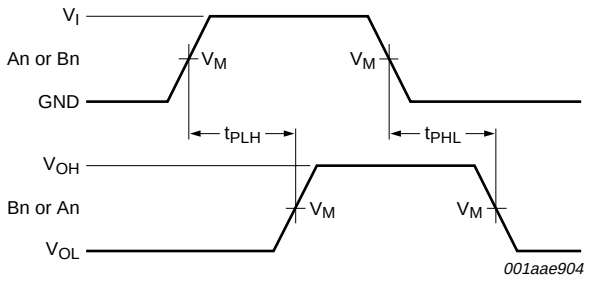
[1] This data sheet limit may vary among suppliers.

11. Waveforms



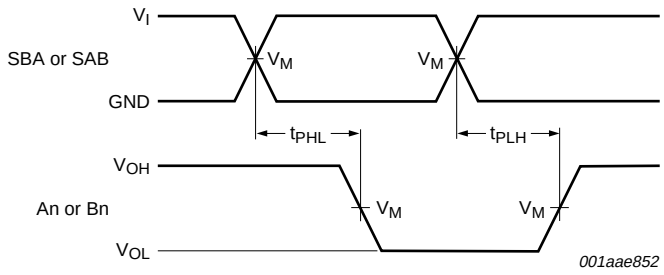
V_M = 1.5 V

Fig 6. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



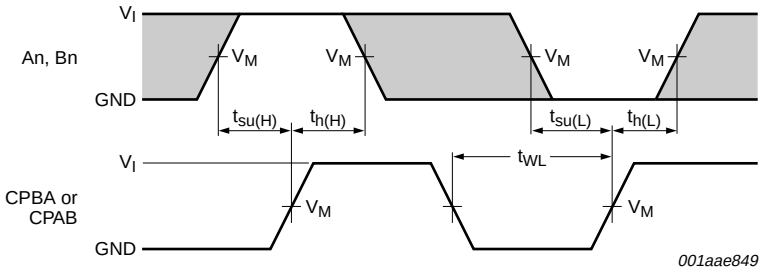
V_M = 1.5 V

Fig 7. Propagation delay, An to Bn or Bn to An



V_M = 1.5 V

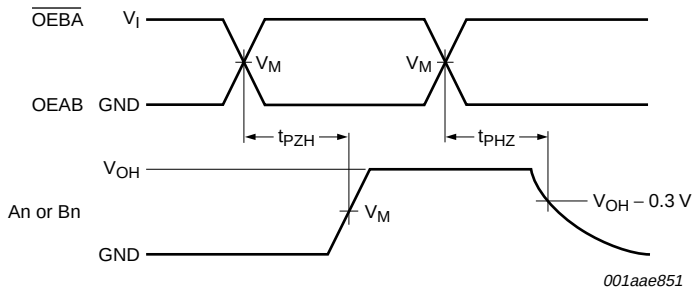
Fig 8. Propagation delay, SBA to An or SAB to Bn



V_M = 1.5 V

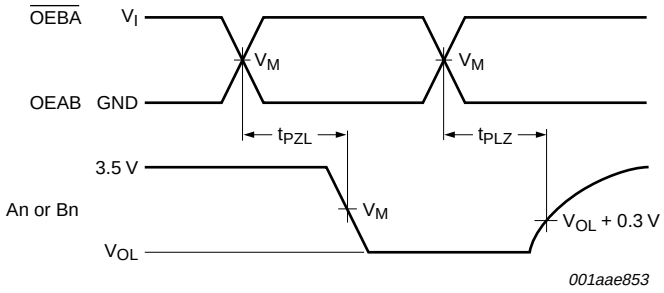
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times



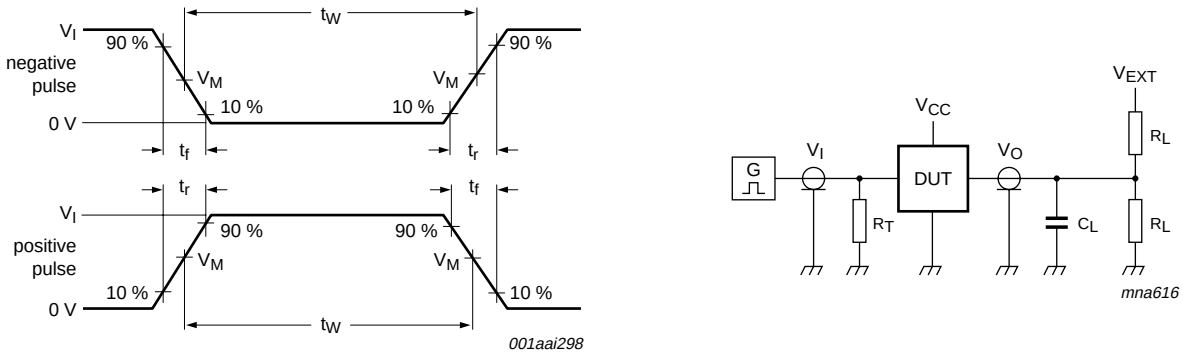
V_M = 1.5 V

Fig 10. 3-state output enable time to HIGH-level and output disable time from HIGH-level



V_M = 1.5 V

Fig 11. 3-state output enable time to LOW-level and output disable time from LOW-level



a. Input pulse definition

b. Test circuit

Test data and V_{EXT} levels are given in Table 8.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

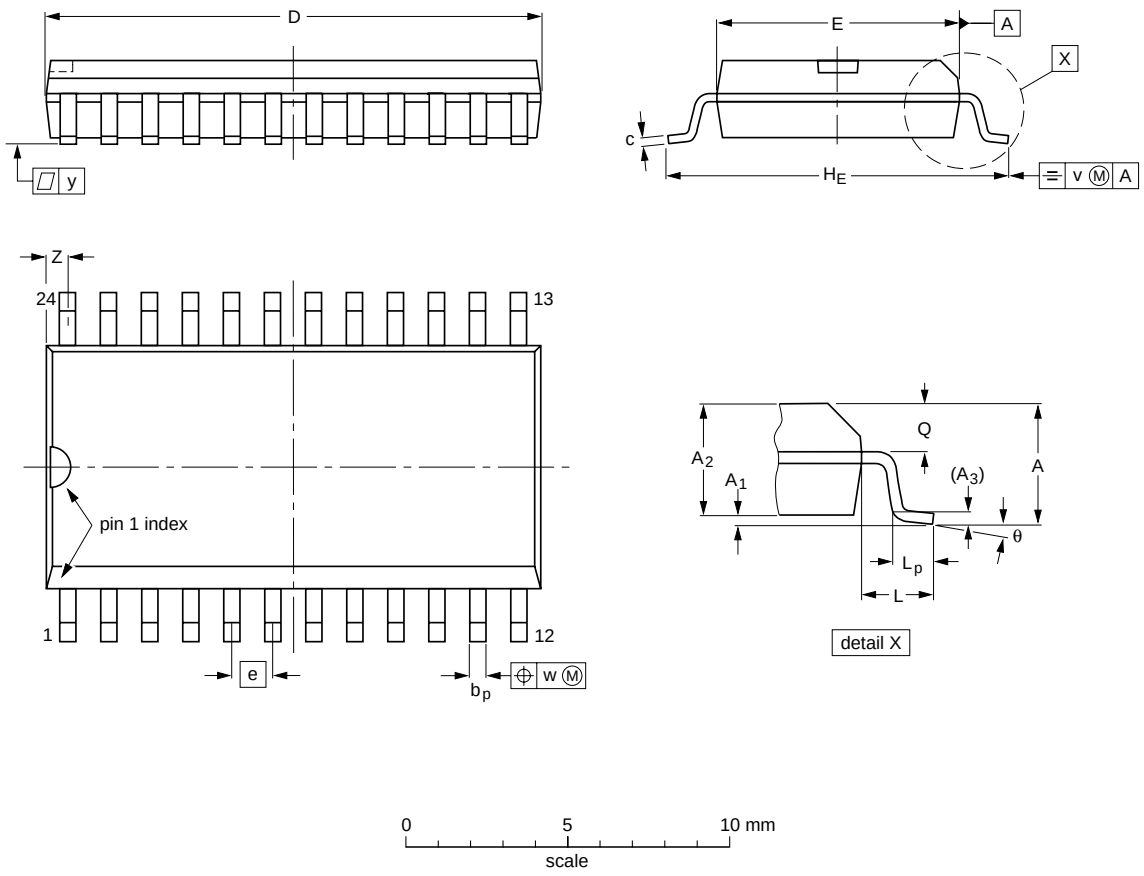
Fig 12. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

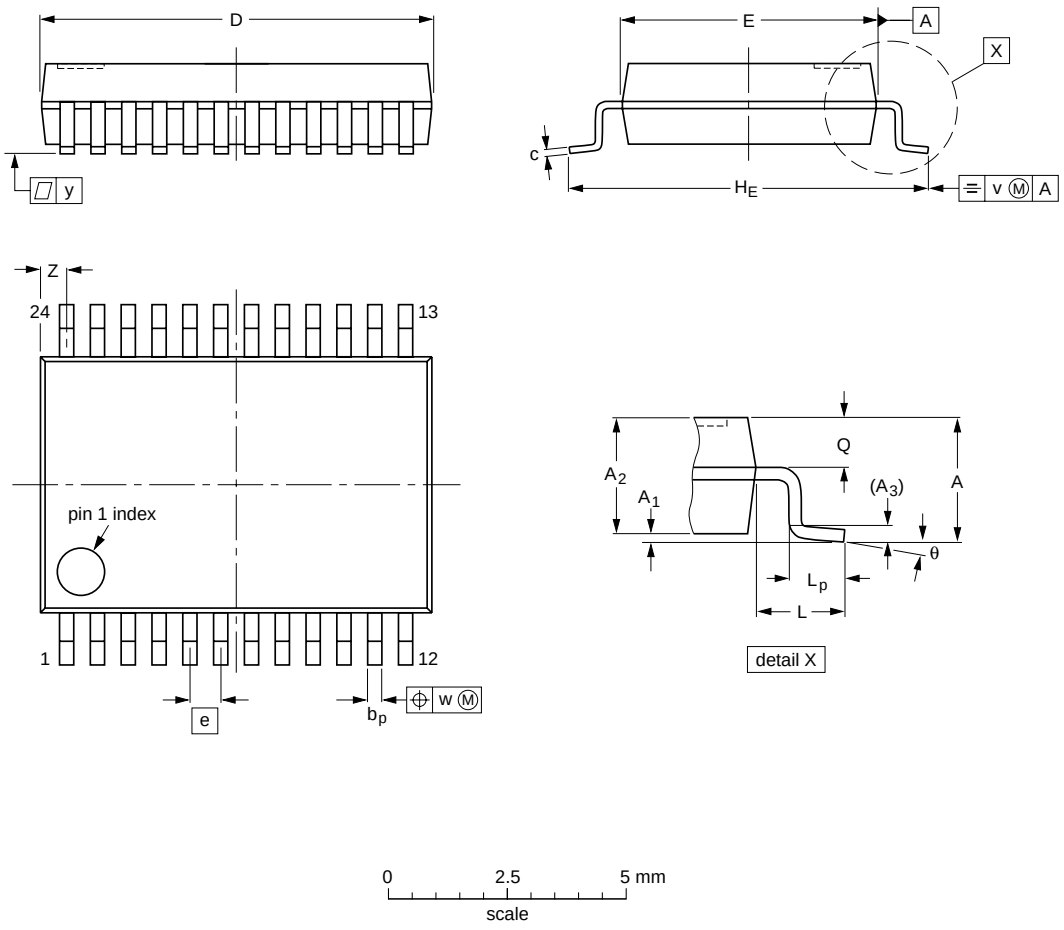
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

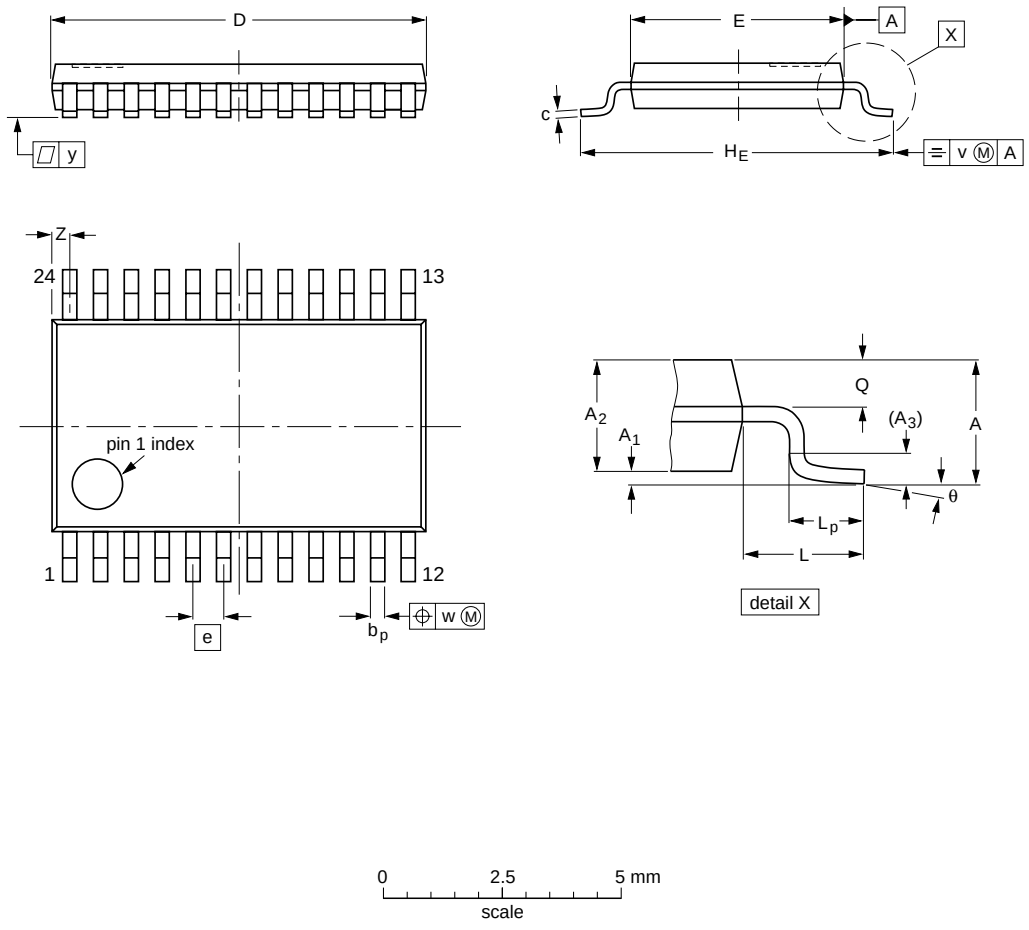
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT355-1 (TSSOP24)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT652A_2	20100312	Product data sheet	-	74ABT652A
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline”.			
74ABT652A	19950419	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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