# BLC8G24LS-240AV

Power LDMOS transistor

Rev. 6 — 2 December 2016

# 1. Product profile

### 1.1 General description

240 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

#### Table 1. Typical performance

Typical RF performance at  $T_{case} = 25 \,^{\circ}$ C in an asymmetrical Doherty production test circuit.  $V_{DS} = 28 \,$ V;  $I_{Dg} = 500 \,$ mA (main);  $V_{GS(amp)peak} = 0.30 \,$ V, unless otherwise specified.

| Test signal      | f            | V <sub>DS</sub> | P <sub>L(AV)</sub> | G <sub>p</sub> | $\eta_D$ | ACPR                 |
|------------------|--------------|-----------------|--------------------|----------------|----------|----------------------|
|                  | (MHz)        | (V)             | (W)                | (dB)           | (%)      | (dBc)                |
| 1-carrier W-CDMA | 2300 to 2400 | 28              | 56                 | 15             | 44       | –29 <mark>[1]</mark> |

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01% probability on CCDF per carrier.

### 1.2 Features and benefits

- Excellent ruggedness
- High-efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Asymmetric design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### **1.3 Applications**

 RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range

**Power LDMOS transistor** 

# 2. Pinning information

| Pin | Description             | Simplified or | utline | Graphic symbol   |
|-----|-------------------------|---------------|--------|------------------|
| 1   | drain2 (peak)           | 2             | 2      |                  |
| 2   | drain1 (main)           | 6<br>[] [= 2  | 9      |                  |
| 3   | gate1 (main)            |               |        | 7⊷∥              |
| 4   | gate2 (peak)            | <br>∏∎ 3      |        | 3                |
| 5   | source                  |               |        | 4 - <b>1</b> - 5 |
| 6   | video decoupling (main) |               |        | 8-               |
| 7   | n.c.                    |               |        | 9                |
| 8   | n.c.                    |               |        | 1                |
| 9   | video decoupling (peak) |               |        | aaa-009150       |

[1] Connected to flange.

# 3. Ordering information

#### Table 3.Ordering information

| Type number     | Packag | Package   |           |  |  |
|-----------------|--------|---|-----------|--|--|
|                 | Name   | Description   | Version   |  |  |
| BLC8G24LS-240AV | -      | air cavity plastic earless flanged package; 8 leads | SOT1252-1 |  |  |

# 4. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                   | Parameter                          | Conditions | Min  | Max  | Unit |
|--------------------------|------------------------------------|------------|------|------|------|
| V <sub>DS</sub>          | drain-source voltage               |            | -    | 65   | V    |
| V <sub>GS(amp)main</sub> | main amplifier gate-source voltage |            | -0.5 | +13  | V    |
| V <sub>GS(amp)peak</sub> | peak amplifier gate-source voltage |            | -0.5 | +13  | V    |
| T <sub>stg</sub>         | storage temperature                |            | -65  | +150 | °C   |
| Tj                       | junction temperature               | <u>[1]</u> | -    | 225  | °C   |

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

# 5. Thermal characteristics

#### Table 5.Thermal characteristics

| Symbol               | Parameter | Conditions   | Тур  | Unit |
|----------------------|-----------|--|------|------|
| R <sub>th(j-c)</sub> |           | V <sub>DS</sub> = 28 V; I <sub>Dq</sub> = 500 mA (main);<br>V <sub>GS(amp)peak</sub> = 0.30 V; T <sub>case</sub> = 80 °C;<br>P <sub>L</sub> = 56 W | 0.26 | K/W  |

# 6. Characteristics

| Table 6. | DC characteristics |  |
|----------|--------------------|--|
|          |                    |  |

 $T_j = 25 \ ^{\circ}C$  unless otherwise specified.

| Symbol               | Parameter                        | Conditions  | Min | Тур   | Max | Unit |
|----------------------|----------------------------------|---|-----|-------|-----|------|
| Main dev             | rice                             |   |     |       |     |      |
| V <sub>(BR)DSS</sub> | drain-source breakdown voltage   | V <sub>GS</sub> = 0 V; I <sub>D</sub> = 1.44 mA                           | 65  | -     | -   | V    |
| V <sub>GS(th)</sub>  | gate-source threshold voltage    | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 144 mA                           | 1.5 | 1.9   | 2.3 | V    |
| I <sub>DSS</sub>     | drain leakage current            | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V                             | -   | -     | 2.8 | μA   |
| I <sub>DSX</sub>     | drain cut-off current            | $V_{GS} = V_{GS(th)} + 3.75 \text{ V};$<br>$V_{DS} = 10 \text{ V}$        | -   | 27    | -   | A    |
| I <sub>GSS</sub>     | gate leakage current             | V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V                             | -   | -     | 280 | nA   |
| 9 <sub>fs</sub>      | forward transconductance         | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 5.04 A                           | -   | 10.10 | -   | S    |
| R <sub>DS(on)</sub>  | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 3.75 V;$<br>I <sub>D</sub> = 5.04 A                | -   | 100   | 166 | mΩ   |
| Peak dev             | vice                             | 1   | 1   |       | 1   |      |
| V <sub>(BR)DSS</sub> | drain-source breakdown voltage   | V <sub>GS</sub> = 0 V; I <sub>D</sub> = 2.2 mA                            | 65  | -     | -   | V    |
| V <sub>GS(th)</sub>  | gate-source threshold voltage    | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 220 mA                           | 1.5 | 1.9   | 2.3 | V    |
| I <sub>DSS</sub>     | drain leakage current            | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V                             | -   | -     | 2.8 | μA   |
| I <sub>DSX</sub>     | drain cut-off current            | $V_{GS} = V_{GS(th)} + 3.75 \text{ V};$<br>$V_{DS} = 10 \text{ V}$        | -   | 41    | -   | A    |
| I <sub>GSS</sub>     | gate leakage current             | V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V                             | -   | -     | 280 | nA   |
| 9 <sub>fs</sub>      | forward transconductance         | V <sub>DS</sub> = 10 V; I <sub>D</sub> = 7.70 A                           | -   | 15.63 | -   | S    |
| R <sub>DS(on)</sub>  | drain-source on-state resistance | V <sub>GS</sub> = V <sub>GS(th)</sub> + 3.75 V;<br>I <sub>D</sub> = 7.7 A | -   | 69    | 112 | mΩ   |

#### Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH;  $f_1$  = 2300 MHz;  $f_2$  = 2400 MHz; RF performance at  $V_{DS}$  = 28 V;  $I_{Dq}$  = 500 mA (main);  $V_{GS(amp)peak}$  = 0.30 V;  $T_{case}$  = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit in 2300 MHz to 2400 MHz.

| Symbol           | Parameter                    | Conditions                | Min  | Тур  | Max | Unit |
|------------------|------------------------------|---------------------------|------|------|-----|------|
| G <sub>p</sub>   | power gain                   | P <sub>L(AV)</sub> = 56 W | 13.3 | 14.5 | -   | dB   |
| RL <sub>in</sub> | input return loss            | P <sub>L(AV)</sub> = 56 W | -    | -10  | -6  | dB   |
| η <sub>D</sub>   | drain efficiency             | P <sub>L(AV)</sub> = 56 W | 38   | 44   | -   | %    |
| ACPR             | adjacent channel power ratio | P <sub>L(AV)</sub> = 56 W | -    | -29  | -25 | dBc  |

# 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLC8G24LS-240AV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 28 V;  $I_{Dq}$  = 500 mA (main);  $V_{GS(amp)peak}$  = 0.30 V;  $P_L$  = 240 W (CW); f = 2300 MHz.

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### 7.2 Impedance information

#### Table 8. Typical impedance of main device

Measured load-pull data of main device;  $I_{Dq}$  = 1000 mA;  $V_{DS}$  = 28 V. Typical values unless otherwise specified.

| f       | Z <sub>S</sub> [1]  | Z <sub>L</sub> [1] | PL <sup>[2]</sup> | η <mark>ρ<sup>[2]</sup></mark> | G <sub>p</sub> [2] |
|---------|---------------------|--------------------|-------------------|--------------------------------|--------------------|
| (MHz)   | (Ω)                 | (Ω)                | (W)               | (%)                            | (dB)               |
| Maximum | power load          |                    |                   |                                |                    |
| 2300    | 1.1 – j3.5          | 1.6 – j4.4         | 171               | 56.20                          | 15.2               |
| 2350    | 1.6 – j3.6          | 1.7 – j4.5         | 178               | 57.60                          | 15.3               |
| 2400    | 1.9 – j4.5          | 1.5 – j4.6         | 175               | 55.10                          | 16.0               |
| Maximum | drain efficiency lo | ad                 |                   |                                |                    |
| 2300    | 1.1 – j3.5          | 3.1 – j3.5         | 127               | 65.50                          | 17.1               |
| 2350    | 1.6 – j3.6          | 2.7 – j3.3         | 130               | 65.30                          | 17.4               |
| 2400    | 1.9 – j4.5          | 2.4 – j3.5         | 131               | 64.70                          | 18.1               |

[1]  $Z_{S}$  and  $Z_{L}$  defined in Figure 1.

[2] at 3 dB gain compression.

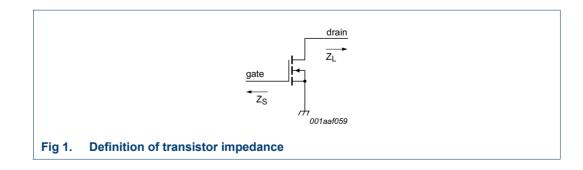
#### Table 9. Typical impedance of peak device

Measured load-pull data of peak device;  $I_{Dq} = 1230 \text{ mA}$ ;  $V_{DS} = 28 \text{ V}$ . Typical values unless otherwise specified.

| f         | Z <sub>S</sub> [1]  | ZL <sup>[1]</sup> | PL <sup>[2]</sup> | ηρ <mark>[2]</mark> | G <sub>p</sub> [2] |
|-----------|---------------------|-------------------|-------------------|---------------------|--------------------|
| (MHz)     | (Ω)                 | (Ω)               | (W)               | (%)                 | (dB)               |
| Maximum p | ower load           |                   | I                 | I.                  | I                  |
| 2300      | 1.0 – j5.3          | 4.0 – j4.5        | 252               | 55.30               | 16.5               |
| 2350      | 1.9 – j5.4          | 3.9 – j4.5        | 248               | 55.00               | 16.1               |
| 2400      | 2.1 – j6.5          | 4.6 – j4.5        | 245               | 53.80               | 16.8               |
| Maximum d | Irain efficiency lo | ad                |                   |                     | I                  |
| 2300      | 1.0 – j5.3          | 2.7 – j2.4        | 190               | 63.90               | 18.3               |
| 2350      | 1.9 – j5.4          | 2.2 – j2.5        | 175               | 63.70               | 18.1               |
| 2400      | 2.1 – j6.5          | 2.3 – j2.7        | 176               | 63.00               | 18.8               |

[1]  $Z_S$  and  $Z_L$  defined in Figure 1.

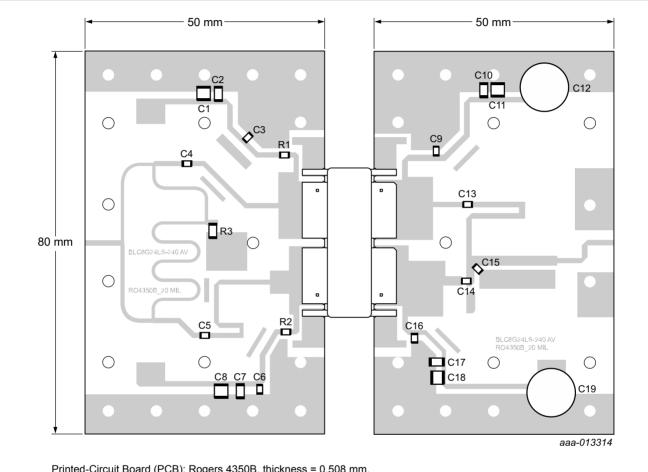
[2] at 3 dB gain compression.



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### 7.3 VBW in Doherty operation

The BLC8G24LS-240AV shows 80 MHz (typical) video bandwidth in Doherty test circuit in 2.35 GHz at  $V_{DS}$  = 28 V;  $I_{Dq}$  = 500 mA and  $V_{GS(amp)peak}$  = 0.30 V.



## 7.4 Test circuit

Printed-Circuit Board (PCB): Rogers 4350B, thickness = 0.508 mm. See <u>Table 10</u> for a list of components.

### Fig 2. Component layout

# Table 10.List of componentsFor test circuit see Figure 2.

| i loc on our oro <u>rigaro 2</u> .   |                                   |               |                       |  |  |
|--------------------------------------|-----------------------------------|---------------|-----------------------|--|--|
| Component                            | Description                       | Value         | Remarks               |  |  |
| C1, C8, C11, C18                     | multilayer ceramic chip capacitor | 10 μF         | Murata                |  |  |
| C2, C7, C10, C17                     | multilayer ceramic chip capacitor | 1 μF          | Murata                |  |  |
| C3, C4, C5, C6,<br>C9, C13, C14, C16 | multilayer ceramic chip capacitor | 12 pF         | ATC 800B              |  |  |
| C12, C19                             | electrolytic capacitor            | 2200 μF, 50 V |                       |  |  |
| C15                                  | multilayer ceramic chip capacitor | 0.8 pF        | ATC 600F              |  |  |
| R1, R2                               | resistor                          | 9.1 Ω         | Vishay Dale: SMD 0805 |  |  |
| R3                                   | resistor                          | 50 Ω          | Vishay Dale: SMD 0805 |  |  |

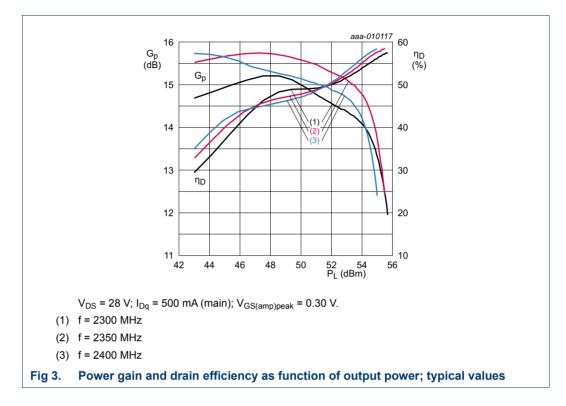
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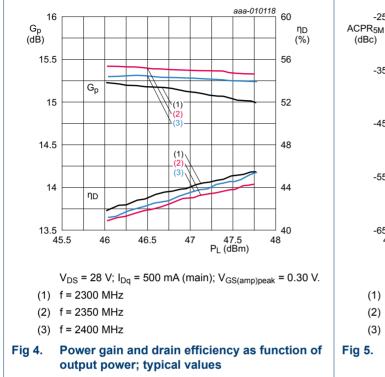
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# 7.5 Graphical data

### 7.5.1 Pulsed CW

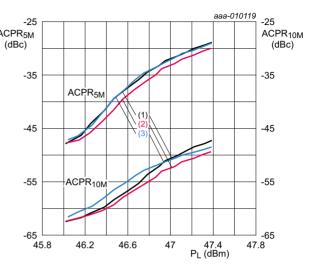


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### 7.5.2 1-Carrier W-CDMA

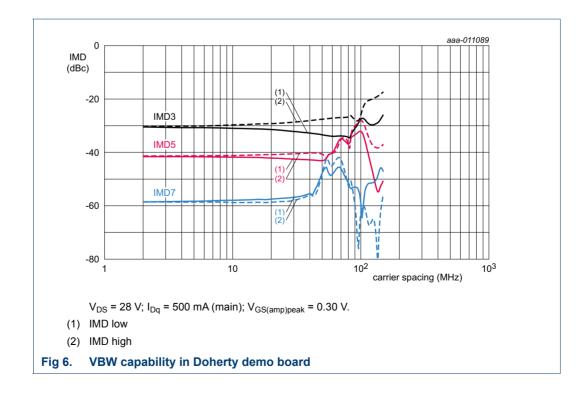




 $V_{DS}$  = 28 V;  $I_{Dq}$  = 500 mA (main);  $V_{GS(amp)peak}$  = 0.30 V.

- (1) f = 2300 MHz
- (2) f = 2350 MHz
- (3) f = 2400 MHz





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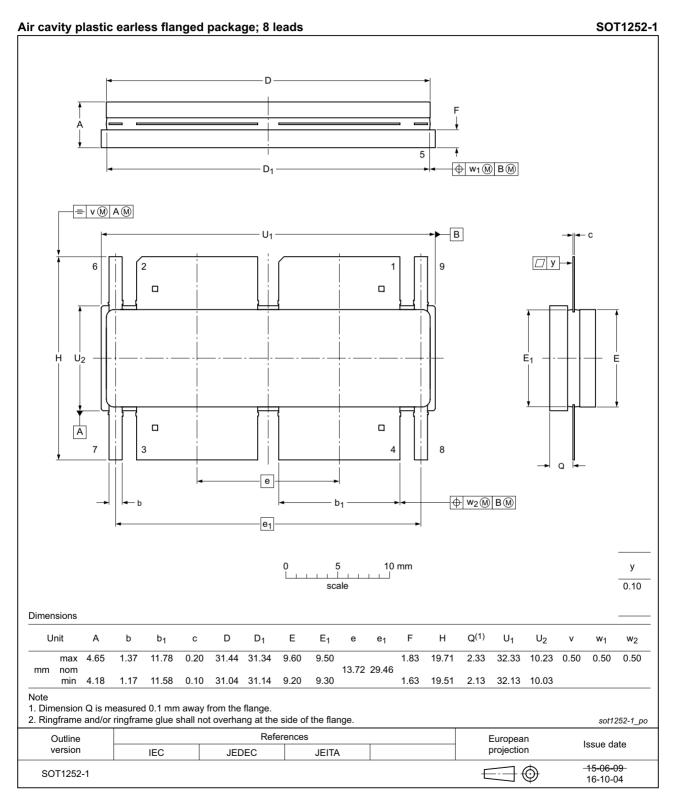
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# AMPLEON

BLC8G24LS-240AV

**Power LDMOS transistor** 

# 8. Package outline



#### Fig 7. Package outline SOT1252-1

BLC8G24LS-240AV
Product data sheet

# 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

#### Table 11.ESD sensitivity

| ESD model                                |                                   | Class   |
|--|-----------------------------------|---------|
| Charged Device Model (CDM); According to | o ANSI/ESDA/JEDEC standard JS-002 | C2A [1] |
| Human Body Model (HBM); According to Al  | NSI/ESDA/JEDEC standard JS-001    | 2 [2]   |

 CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

# **10. Abbreviations**

#### Table 12. Abbreviations

| Acronym | Description                                    |
|---------|--|
| 3GPP    | 3rd Generation Partnership Project             |
| CCDF    | Complementary Cumulative Distribution Function |
| CW      | Continuous Wave                                |
| DPCH    | Dedicated Physical CHannel                     |
| ESD     | ElectroStatic Discharge                        |
| LDMOS   | Laterally Diffused Metal-Oxide Semiconductor   |
| MTF     | Median Time to Failure                         |
| PAR     | Peak-to-Average Ratio                          |
| SMD     | Surface Mounted Device                         |
| VBW     | Video Bandwidth                                |
| VSWR    | Voltage Standing Wave Ratio                    |
| W-CDMA  | Wideband Code Division Multiple Access         |

# 11. Revision history

### Table 13. Revision history

| Document ID         | Release date  | Data sheet status             | Change notice | Supersedes          |  |
|---------------------|---|-------------------------------|---------------|---------------------|--|
| BLC8G24LS-240AV v.6 | 20161202  | Product data sheet            | -             | BLC8G24LS-240AV v.5 |  |
| Modifications:      | <u>Figure 7 on page 8</u> : updated package outline drawing SOT1252-1 |                               |               |                     |  |
|                     | Section 9 on  | page 9: updated Handling info | ormation      |                     |  |
| BLC8G24LS-240AV v.5 | 20160106  | Product data sheet            | -             | BLC8G24LS-240AV v.4 |  |
| BLC8G24LS-240AV v.4 | 20150901  | Product data sheet            | -             | BLC8G24LS-240AV v.3 |  |
| BLC8G24LS-240AV v.3 | 20150728  | Product data sheet            | -             | BLC8G24LS-240AV v.2 |  |
| BLC8G24LS-240AV v.2 | 20141218  | Product data sheet            | -             | BLC8G24LS-240AV v.1 |  |
| BLC8G24LS-240AV v.1 | 20130926  | Objective data sheet          | -             | -                   |  |

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### 12.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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