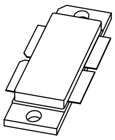

BLF872

UHF power LDMOS transistor

Rev. 01 — 20 February 2006 **Product data sheet**

1. Product profile

1.1 General description

A 300 W LDMOS RF power transistor for broadcast transmitter applications and industrial applications. The transistor can deliver 250 W broadband over the full UHF band from 470 MHz to 860 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital transmitter applications.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical 2-tone performance at 860 MHz, a drain-source voltage V_{DS} of 32 V and a quiescent drain current I_{Dq} = 2 × 0.9 A:
  - Peak envelope power load power $P_{L(PEP)}$ = 300 W
  - Gain G_p = 15 dB
  - Drain efficiency η_D = 43 %
  - Third order intermodulation distortion IMD3 = –28 dBc
- Typical DVB performance at 858 MHz, a drain-source voltage V_{DS} of 32 V and a quiescent drain current I_{Dq} = 2 × 0.9 A:
  - Average output power $P_{L(AV)}$ = 70 W
  - Gain G_p = 15 dB
  - Drain efficiency η_D = 30 %
  - Third order intermodulation distortion IMD3 = –28 dBc (4.3 MHz from center frequency)
- Advanced flange material for optimum thermal behavior and reliability
- Excellent ruggedness
- High power gain
- Designed for broadband operation (UHF band)
- Excellent reliability
- Internal input and output matching for high gain and optimum broadband operation
- Source on underside eliminates DC isolators, reducing common-mode inductance
- Easy power control

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1.3 Applications

- Communication transmitter applications in the UHF band
- Industrial applications in the UHF band

1.4 Quick reference data

Table 1: Quick reference data

Typical RF performance at V_{DS} = 32 V and T_h = 25 °C in a common-source narrowband 860 MHz test circuit. [1]

Mode of operation	f (MHz)	P_L (W)	$P_{L(PEP)}$ (W)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)
CW, class AB	860	300	-	-	14	55	-
2-tone, class AB	f_1 = 860; f_2 = 860.1	-	300	-	15	42	–28
PAL BG	860 (ch69)	300 (peak sync.) [2]	-	-	15	42	-
DVB-T (8K OFDM)	858	-	-	70	15	30	–28 [3]

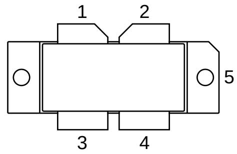
[1] T_h is the heatsink temperature.

[2] Black video signal, sync expansion: input sync = 33 %; output sync ≥ 27 %.

[3] Measured dBc at 4.3 MHz from center frequency.

2. Pinning information

Table 2: Pinning

Description	Pin		Simplified outline
drain 1	1		
drain 2	2		
gate 1	3		
gate 2	4		
source	5	[1]	

[1] Connected to flange.

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
BLF872	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT800-1

4. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-	±13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_h = 25 °C	[1]	0.32	K/W
$R_{th(j-h)}$	thermal resistance from junction to heatsink	T_h = 25 °C	[1] [2]	0.4	K/W

[1] T_h is the heatsink temperature.

[2] $R_{th(j-h)}$ is dependent on the applied thermal compound and clamping/mounting of the device.

6. Characteristics

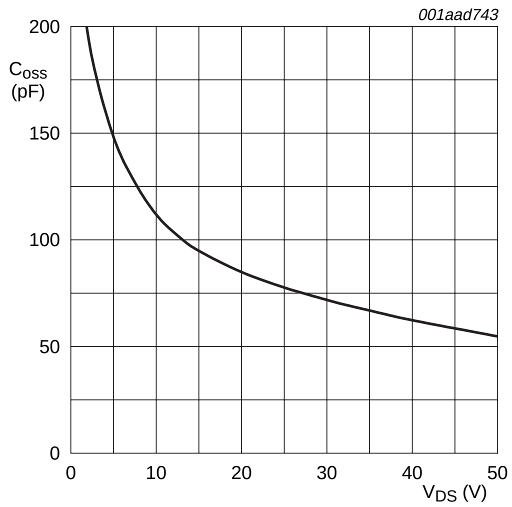
Table 6: Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions [1]		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 5 mA		65	-	-	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 20 V; I_D = 250 mA		5.2	-	6.2	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V		-	-	2.2	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 6 V; V_{DS} = 10 V		-	41	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V		-	-	40	nA
g_{fs}	forward transconductance	V_{GS} = 20 V; I_D = 16 A		-	10	-	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 6 V; I_D = 9 A		-	80	-	mΩ
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	[2]	-	200	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	[2]	-	70	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	[2]	-	2.5	-	pF

[1] I_D is the drain current.

[2] Capacitance values without internal matching.



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance C_{oss} as a function of drain-source voltage V_{DS}; typical values per section; capacitance value without internal matching

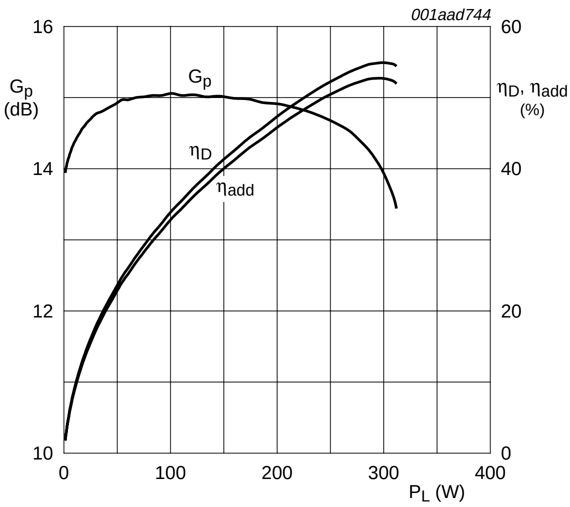
7. Application information

Table 7: RF performance in a common-source 860 MHz narrowband test circuit

T_h = 25 °C unless otherwise specified. [1]

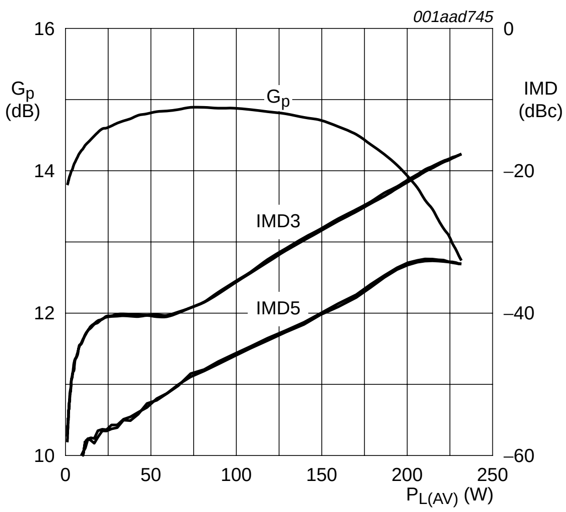
Mode of operation	f (MHz)	V_{DS} (V)	I_{Dq} (A)	$P_{L(PEP)}$ (W)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	ΔG_p (dB)
2-tone, class AB	f_1 = 860; f_2 = 860.1	32	2 × 0.9	300	-	> 14	> 40	≤ –25	≤ 1
DVB-T (8K OFDM)	858	32	2 × 0.9	-	70	> 14	> 26	≤ –25	-

[1] Sync. compression: input sync. ≥ 33 %, output sync. 27 %.



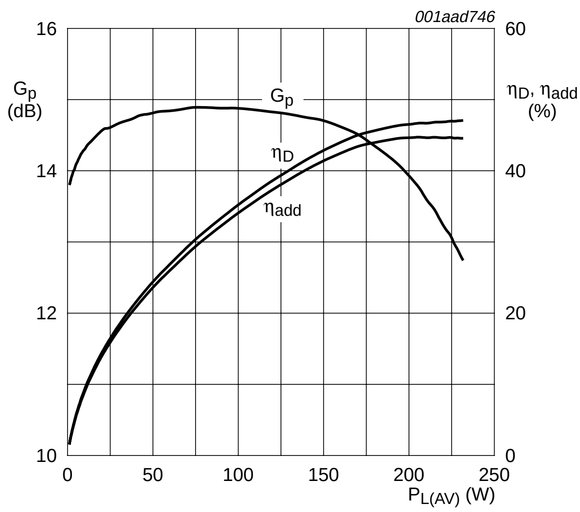
V_{DS} = 32 V; f = 860 MHz; I_{Dq} = 2 × 0.9 A; T_h = 25 °C.

Fig 2. CW power gain G_p, drain efficiency η_D and power added efficiency η_{add} as a function of output power P_L; typical values



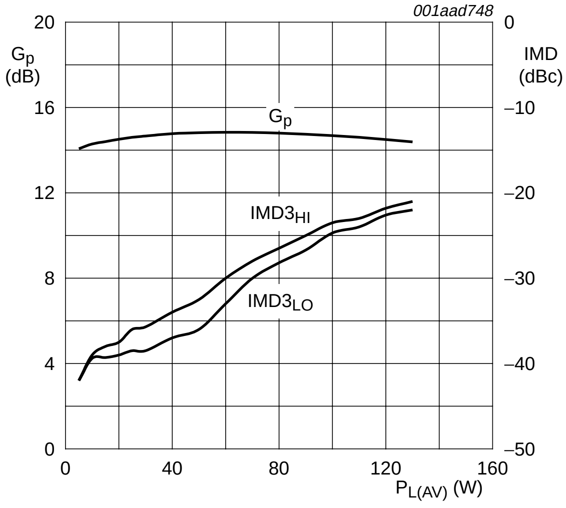
V_{DS} = 32 V; f_1 = 860 MHz; f_2 = 860.1 MHz;
I_{Dq} = 2 × 0.9 A; T_h = 25 °C.

Fig 3. 2-tone power gain G_p and intermodulation distortion IMD as a function of average output power $P_{L(AV)}$; typical values



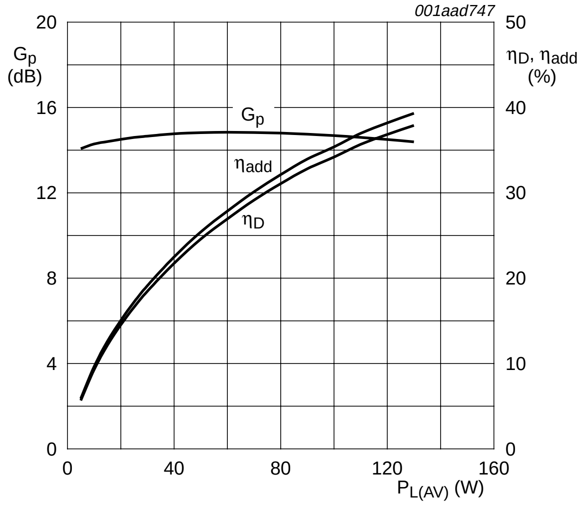
V_{DS} = 32 V; f_1 = 860 MHz; f_2 = 860.1 MHz;
I_{Dq} = 2 × 0.9 A; T_h = 25 °C.

Fig 4. 2-tone power gain G_p, drain efficiency η_D and power added efficiency η_{add} as a function of average output power $P_{L(AV)}$; typical values



IMD at ±4.3 MHz from frequency center.

Fig 5. DVB-T (8K OFDM) power gain G_p and third order intermodulation distortion (high-frequency component $IMD3_{HI}$ and low-frequency component $IMD3_{LO}$) as a function of average output power $P_{L(AV)}$; typical values

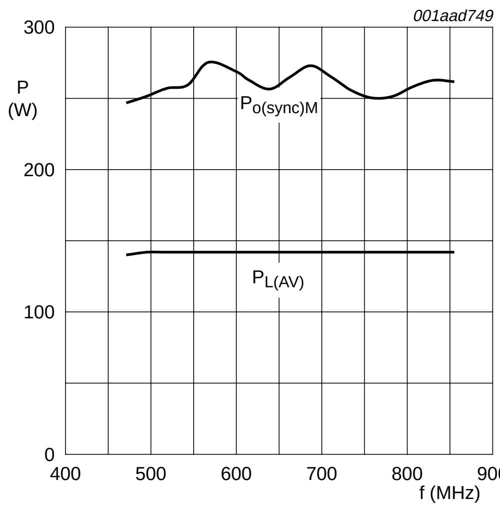


V_{DS} = 32 V; f = 858 MHz; I_{Dq} = 2 × 0.9 A; T_h = 25 °C.

Fig 6. DVB-T (8K OFDM) power gain G_p, drain efficiency η_D and power added efficiency η_{add} as a function of average output power $P_{L(AV)}$; typical values

7.1 Broadband operation data

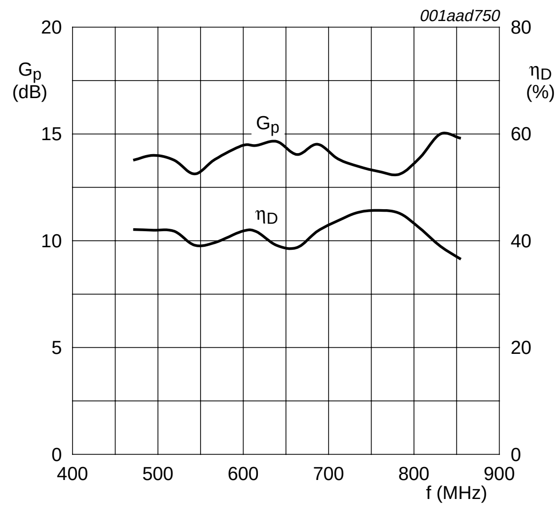
Measured in a common-source broadband (470 MHz to 860 MHz) test circuit.



V_{DS} = 32 V; I_{Dq} = 2 × 0.9 A; T_h = 25 °C.

Black video signal, sync expansion:
input sync = 33 %; output sync ≥ 27 %.

Fig 7. Analog TV (black video signal) peak sync output power $P_{o(sync)M}$ and average output power $P_{L(AV)}$ as a function of frequency f



V_{DS} = 32 V; I_{Dq} = 2 × 0.9 A; T_h = 25 °C.

Black video signal, sync expansion:
input sync = 33 %; output sync ≥ 27 %.

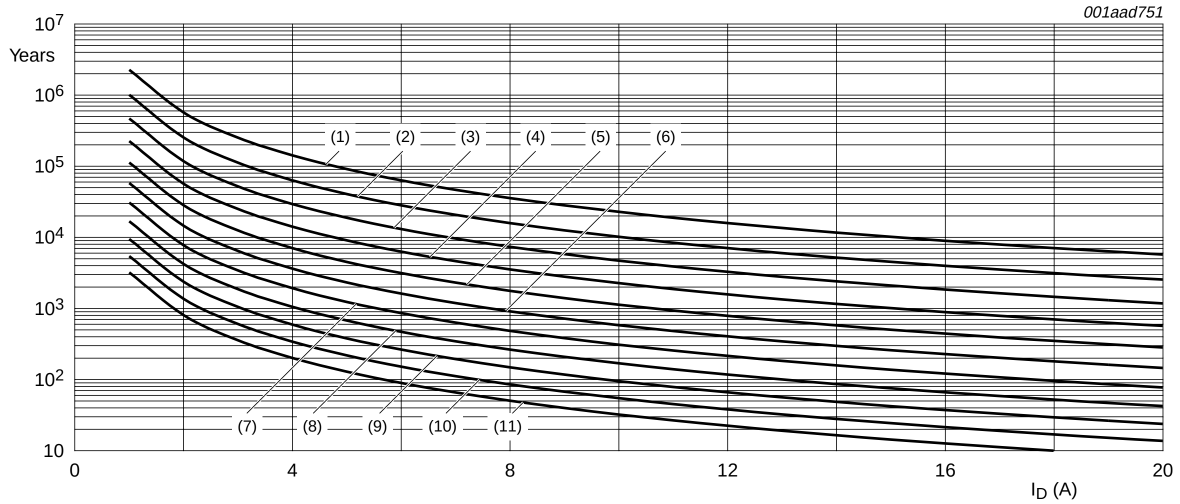
Fig 8. Analog TV (black video signal) power gain G_p and drain efficiency η_D as a function of frequency f

7.2 Ruggedness in class-AB operation

The BLF872 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 860 MHz at rated power.

Measured in a common-source broadband (470 MHz to 860 MHz) test circuit.

7.3 Reliability



TTF; 0.1 % failure fraction; best estimate values.

(1) T_j = 100 °C

(2) T_j = 110 °C

(3) T_j = 120 °C

(4) T_j = 130 °C

(5) T_j = 140 °C

(6) T_j = 150 °C

(7) T_j = 160 °C

(8) T_j = 170 °C

(9) T_j = 180 °C

(10) T_j = 190 °C

(11) T_j = 200 °C

Fig 9. BLF872 electromigration (I_D, total device)

8. Test information

Table 8: List of components

For test circuit, see Figure 10, 11 and 12.

Component	Description	Value		Remarks
B1, B2 balun	semi rigid coax	25 Ω		EZ90-25-TP
C1	multilayer ceramic chip capacitor	12 pF	[1]	
C2	multilayer ceramic chip capacitor	10 pF	[1]	
C3, C5	multilayer ceramic chip capacitor	5.6 pF	[1]	
C4	multilayer ceramic chip capacitor	6.8 pF	[1]	
C6, C7	multilayer ceramic chip capacitor	2.0 pF	[2]	
C8	multilayer ceramic chip capacitor	18 pF	[1]	
C9, C10	multilayer ceramic chip capacitor	0.5 pF	[2]	
C11, C12	multilayer ceramic chip capacitor	100 pF	[1]	
C13, C14	multilayer ceramic chip capacitor	100 pF	[2]	

Table 8: List of components *...continued*

For test circuit, see Figure 10, 11 and 12.

Component	Description	Value		Remarks
C15, C16	ceramic capacitor	15 nF		
C17, C18	electrolytic capacitor	470 μF		
C20	multilayer ceramic chip capacitor	13 pF	[3]	
C21	tekelec trimmer	0.6 pF to 4.5 pF		
C22	multilayer ceramic chip capacitor	3.9 pF	[3]	
C23	multilayer ceramic chip capacitor	10 pF	[3]	
C24, C32	multilayer ceramic chip capacitor	3.0 pF	[3]	
C25	multilayer ceramic chip capacitor	30 pF	[3]	
C26, C27	multilayer ceramic chip capacitor	100 pF	[3]	
C28, C29	ceramic capacitor	15 nF		
C30, C31	electrolytic capacitor	10 μF		
L1	stripline		[4]	(W × L) 24 mm × 13.1 mm
L2	stripline		[4]	(W × L) 10 mm × 17.7 mm
L3	stripline		[4]	(W × L) 5 mm × 16.5 mm
L4	stripline		[4]	(W × L) 2.4 mm × 15 mm
L5	stripline		[4]	(W × L) 3.5 mm × 43 mm
L6	stripline		[4]	(W × L) 2 mm × 43.3 mm
L10	stripline		[4]	(W × L) 24 mm × 10 mm
L11	stripline		[4]	(W × L) 10 mm × 15 mm
L12	stripline		[4]	(W × L) 3 mm × 31.5 mm
L13	stripline		[4]	(W × L) 2 mm × 43.3 mm
R1	resistor	5.6 Ω		
R2	resistor	5.6 Ω		
R3	resistor	100 Ω		
R4	resistor	100 Ω		
R5	potentiometer	2 kΩ		
R6	potentiometer	2 kΩ		

[1] American technical ceramics type 180R or capacitor of same quality.

[2] American technical ceramics type 100B or capacitor of same quality.

[3] American technical ceramics type 100A or capacitor of same quality.

[4] PCB: Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.

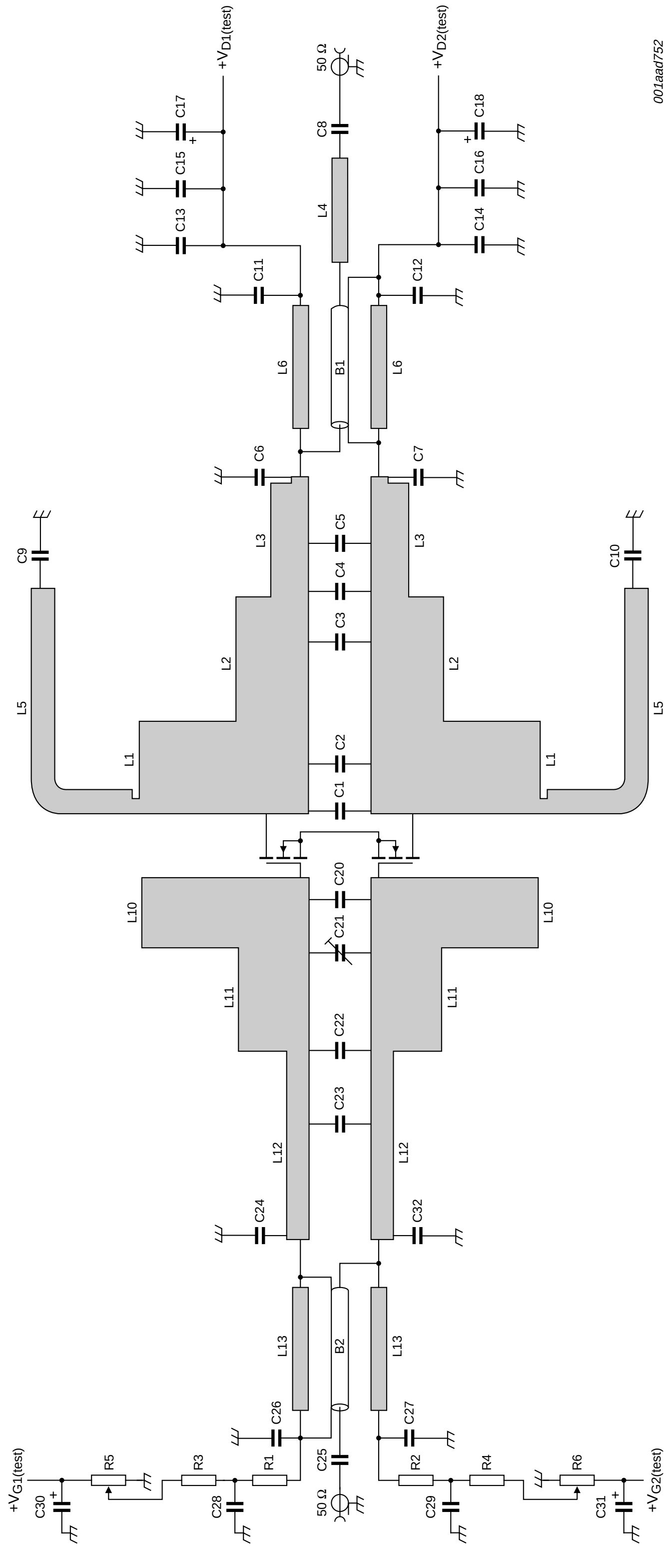


Fig 10. Class-AB common-source broadband test circuit; $V_{D1(test)}$, $V_{D2(test)}$, $V_{G1(test)}$ and $V_{G2(test)}$ are drain and gate test voltages

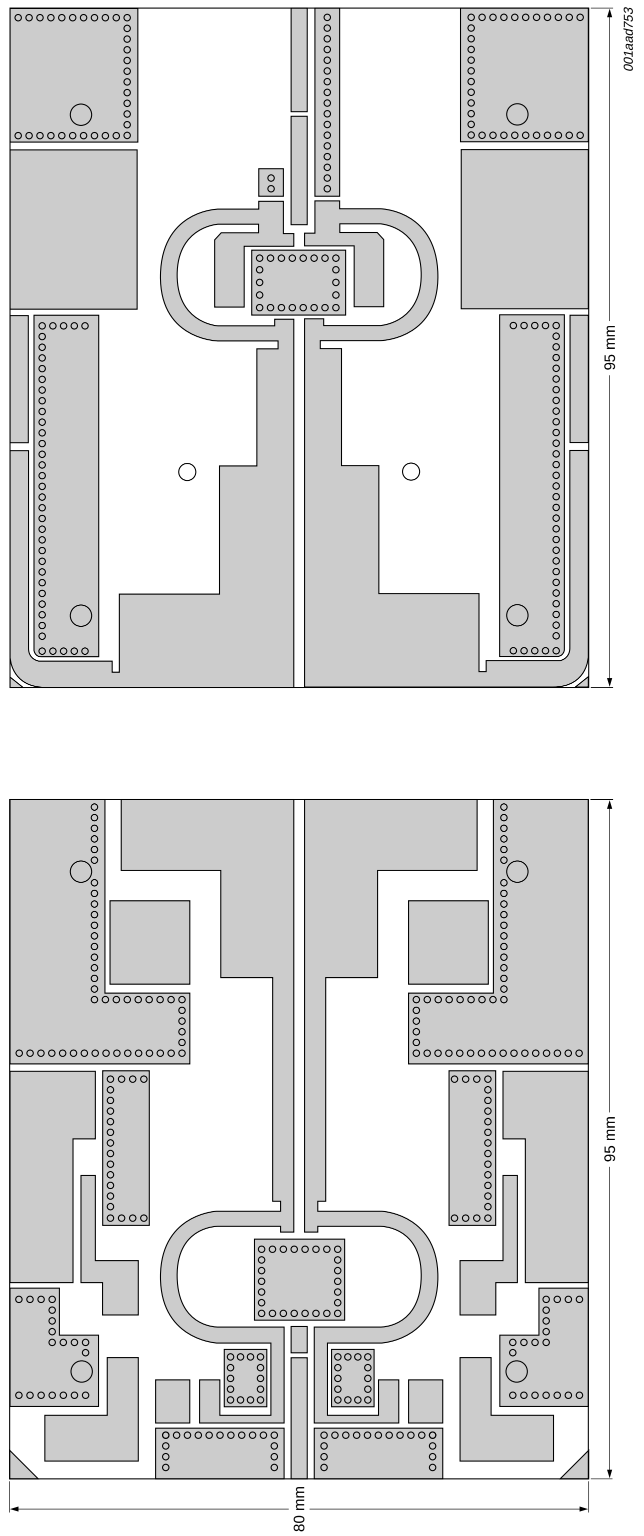


Fig 11. Printed-circuit board for class-AB broadband test circuit

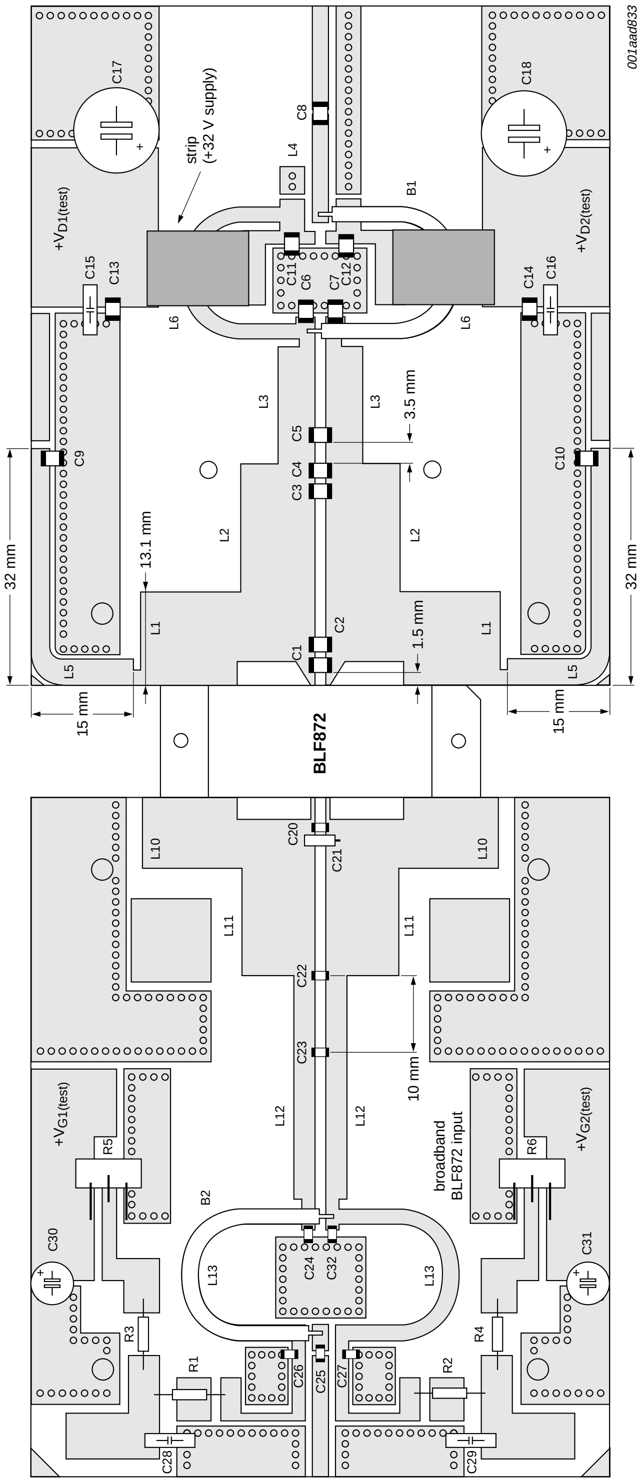
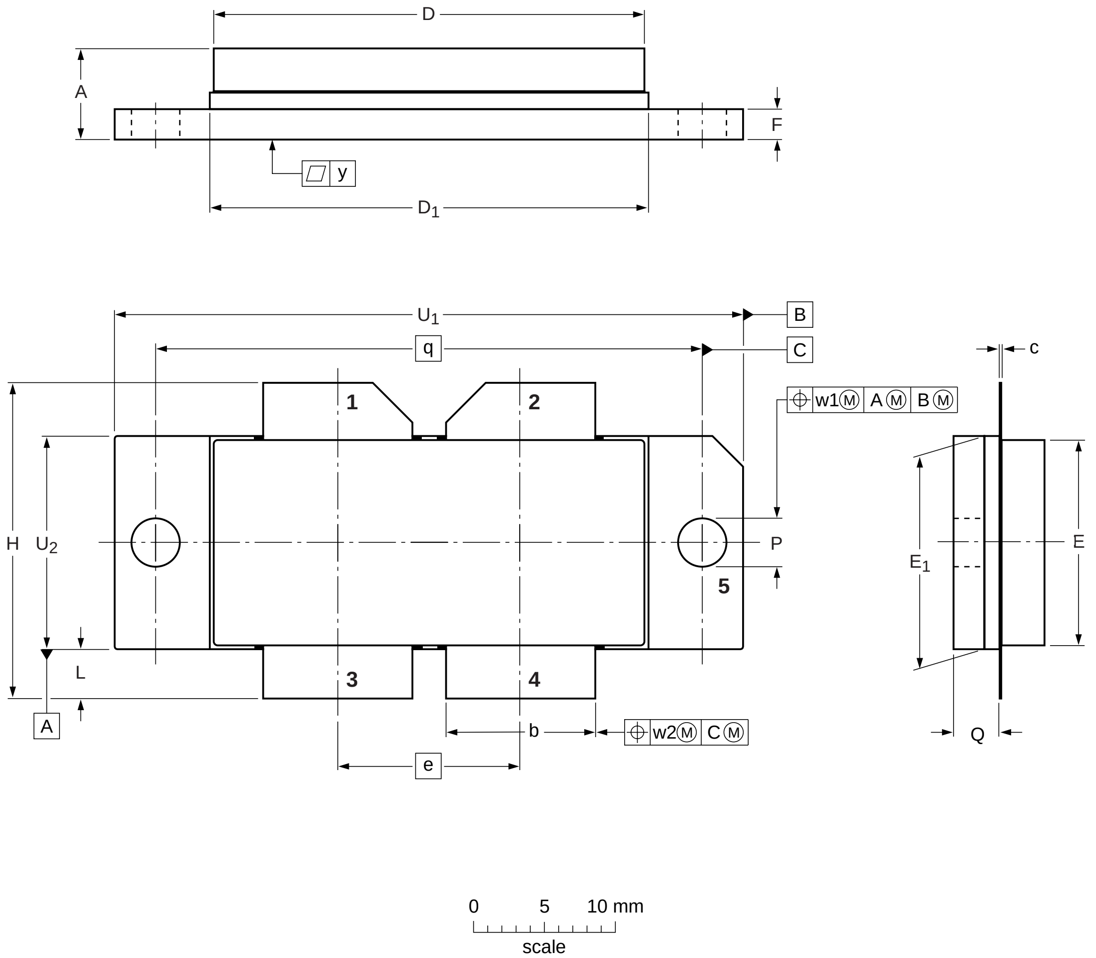


Fig 12. Component layout for class-AB broadband test circuit

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT800-1**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	e	F	H	L	p	Q	q	U_1	U_2	w_1	w_2	y
mm	6.6 6.2	10.55 10.45	0.15 0.10	30.5 29.9	31.1 30.9	14.6 14.4	15.3 15.1	12.7	2.26 2.00	22.8 21.8	3.7 3.3	3.56 3.49	3.4 3.1	38.5	44.5 44.2	15.4 15.0	0.25	0.25	0.05
inches	0.260 0.244	0.415 0.411	0.006 0.004	1.201 1.177	1.224 1.216	0.575 0.567	0.602 0.594	0.5	0.089 0.079	0.898 0.858	0.146 0.130	0.140 0.137	0.134 0.122	1.516	1.752 1.740	0.606 0.591	0.01	0.01	0.002

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT800-1						~~05-06-02~~ 05-06-07

Fig 13. Package outline SOT800-1

10. Abbreviations

Table 9: Abbreviations

Acronym	Description
CDMA	Code Division Multiple Access
CW	Continuous Wave
DVB	Digital Video Broadcast
EDGE	Enhanced Data rates for GSM Evolution
ESR	Equivalent Series Resistance
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
OFDM	Orthogonal Frequency Division Multiplexing
PCB	Printed-Circuit Board
PEP	Peak Envelope Power
RF	Radio Frequency
SMD	Surface Mount Device
TTF	Time To Failure
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BLF872_1	20060220	Product data sheet	-	-	-

12. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

13. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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17. Contents

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