

# BLF546

UHF push-pull power MOS transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

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Ampleon

## UHF push-pull power MOS transistor

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## FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

## DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268A balanced flange package, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

## PINNING - SOT268A

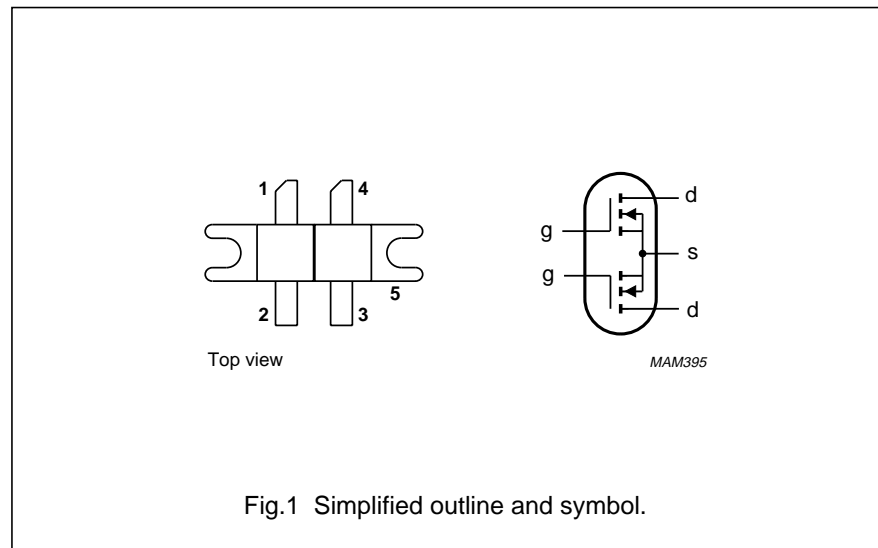
PIN	DESCRIPTION
1	drain 1
2	gate 1
3	gate 2
4	drain 2
5	source

## QUICK REFERENCE DATA

RF performance at  $T_h = 25\text{ }^\circ\text{C}$  in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)
CW, class-B	500	28	80	>11	>50

## PIN CONFIGURATION



## CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

## WARNING

## Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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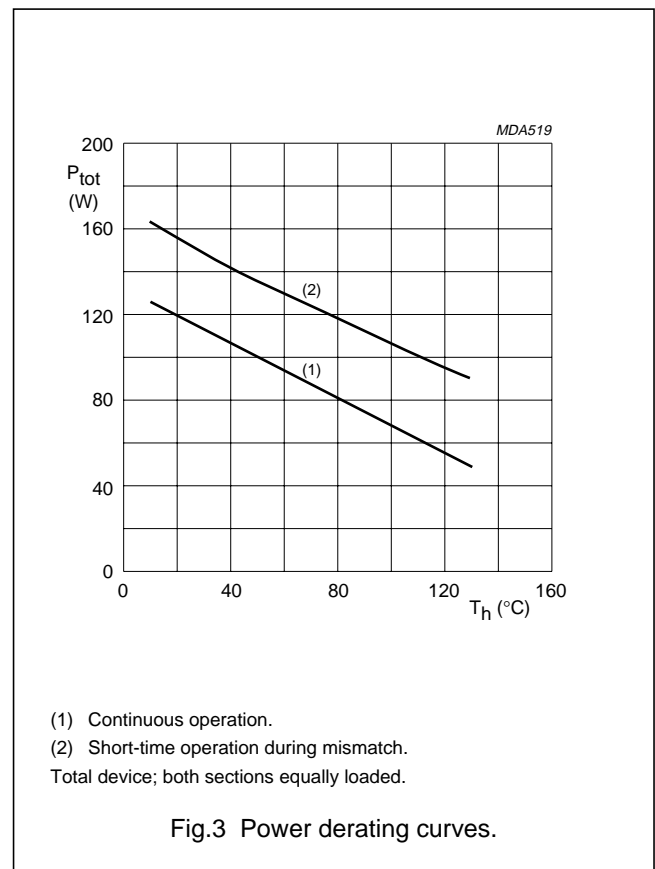
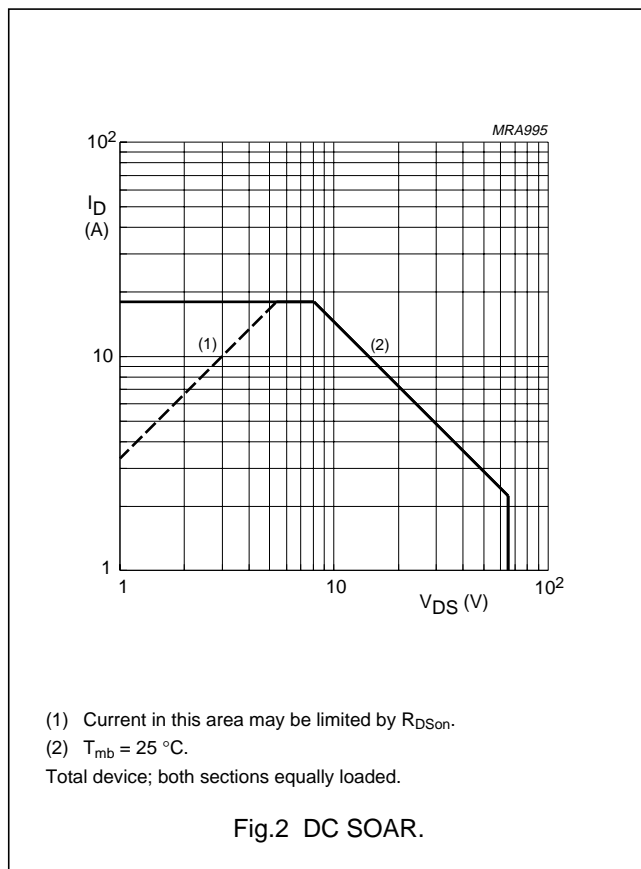
## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor section (unless otherwise specified)</b>					
$V_{DS}$	drain-source voltage		–	65	V
$V_{GS}$	gate-source voltage		–	$\pm 20$	V
$I_D$	drain current (DC)		–	9	A
$P_{tot}$	total power dissipation	$T_{mb} \leq 25\text{ }^\circ\text{C}$ ; total device; both sections equally loaded	–	145	W
$T_{stg}$	storage temperature		–65	150	$^\circ\text{C}$
$T_j$	junction temperature		–	200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.2	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25	K/W



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## CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

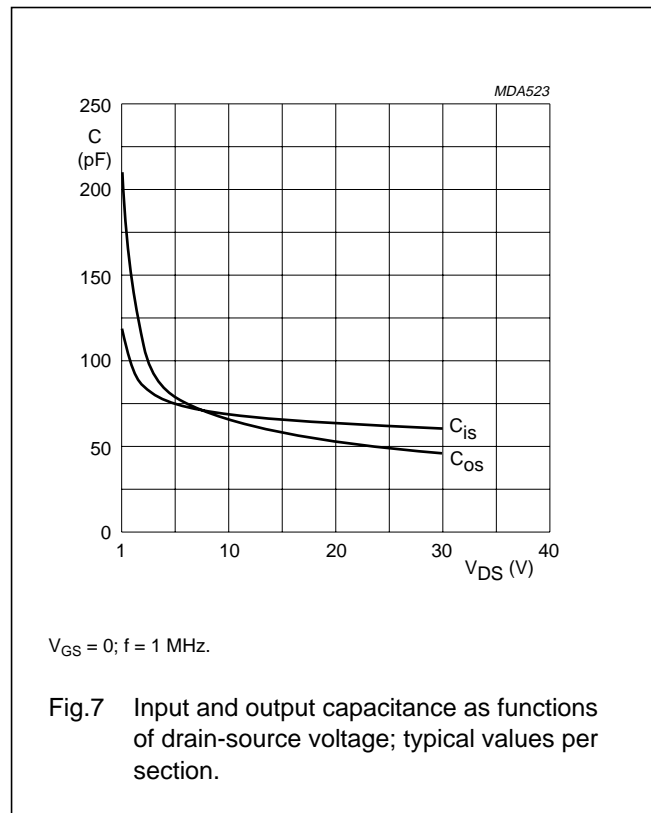
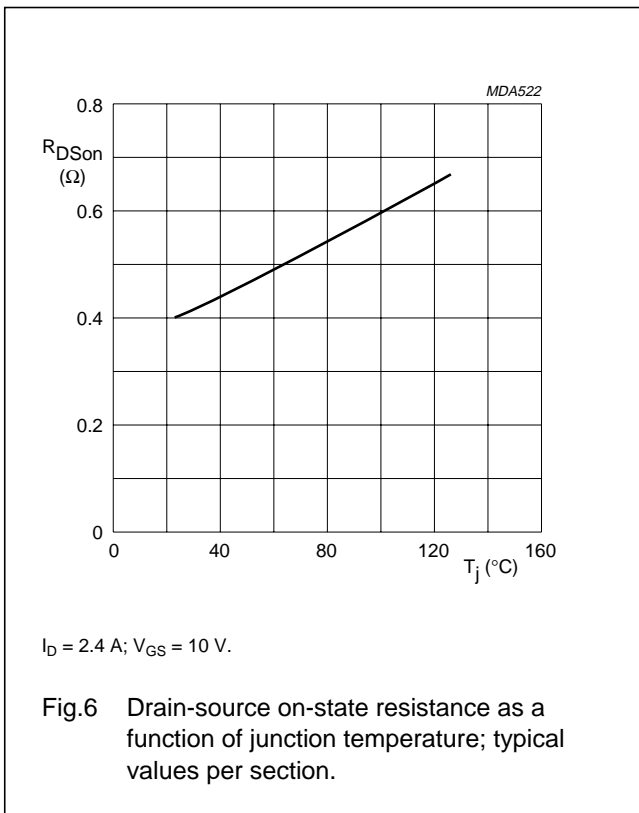
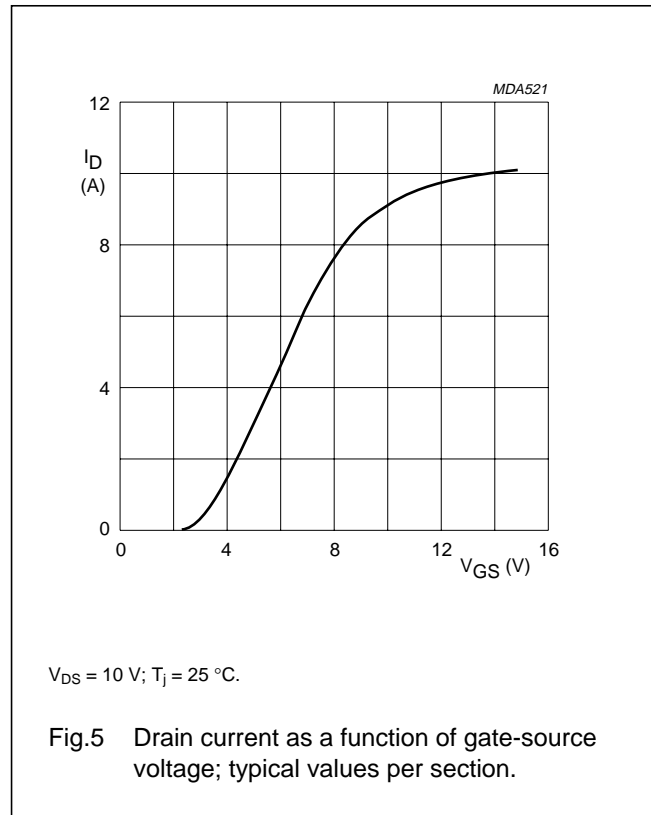
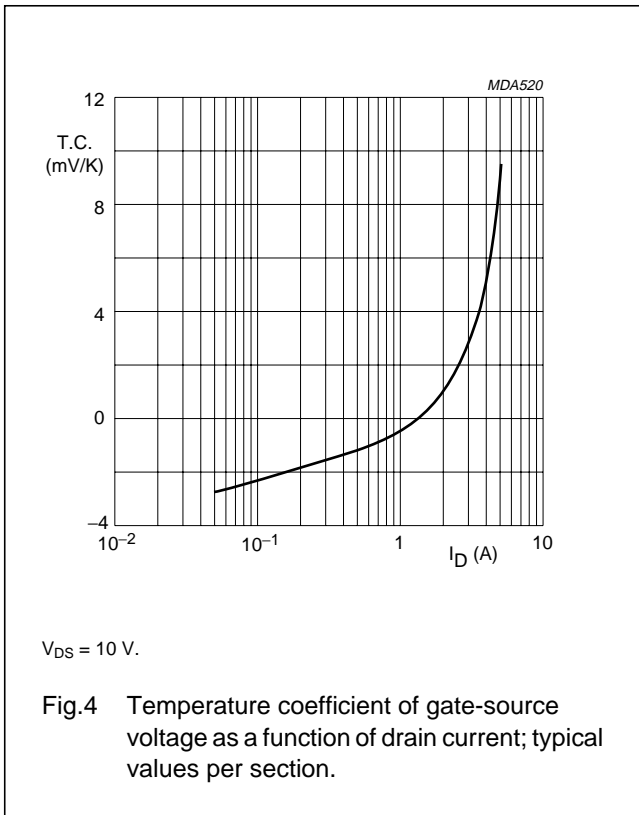
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per section</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 20\text{ mA}$	65	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	2	mA
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$	–	–	1	$\mu\text{A}$
$V_{GSth}$	gate-source threshold voltage	$I_D = 80\text{ mA}; V_{DS} = 10\text{ V}$	1	–	4	V
$g_{fs}$	forward transconductance	$I_D = 2.4\text{ A}; V_{DS} = 10\text{ V}$	1.2	1.7	–	S
$R_{DSon}$	drain-source on-state resistance	$I_D = 2.4\text{ A}; V_{GS} = 10\text{ V}$	–	0.4	0.6	$\Omega$
$I_{DSX}$	on-state drain current	$V_{GS} = 15\text{ V}; V_{DS} = 10\text{ V}$	–	10	–	A
$C_{is}$	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	60	–	pF
$C_{os}$	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	46	–	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	15	–	pF

 $V_{GS}$  group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

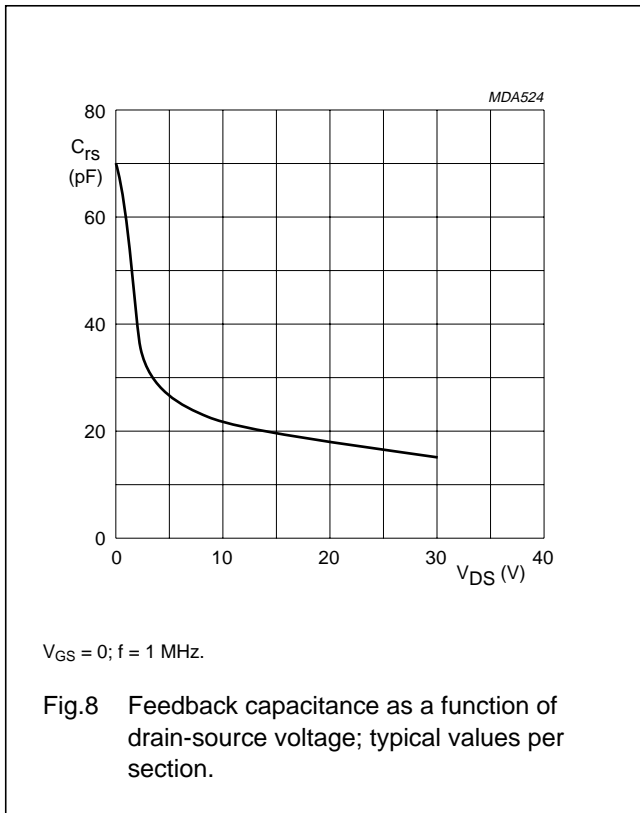
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**APPLICATION INFORMATION FOR CLASS-B OPERATION**

$T_h = 25$  °C;  $R_{th\ mb-h} = 0.25$  K/W, unless otherwise specified.

RF performance in a common source, class-B, push-pull circuit.

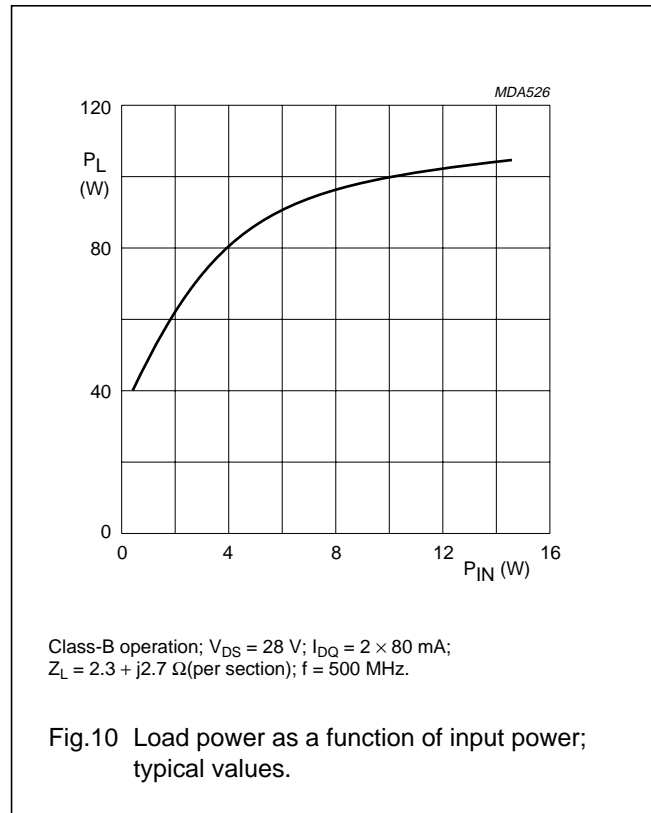
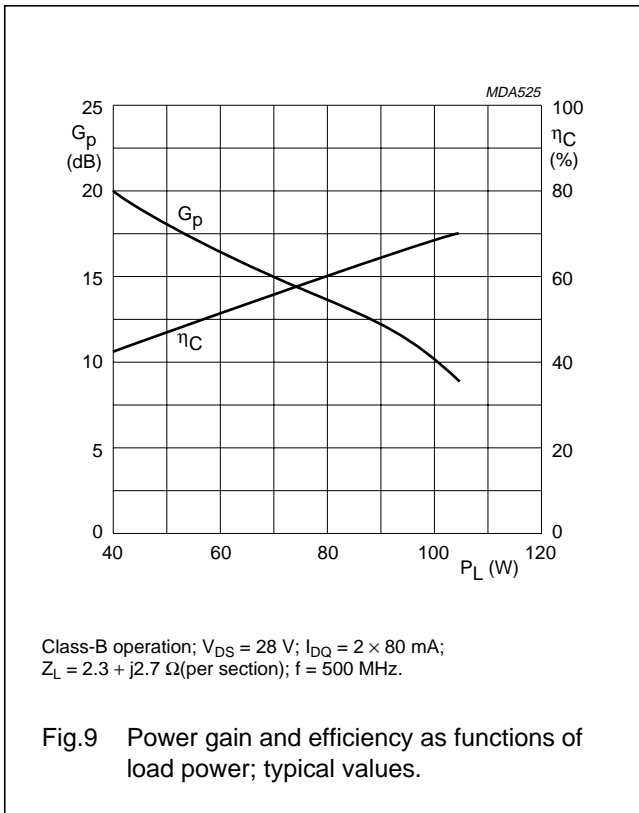
MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$I_{DQ}$ (mA)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)
CW, class-B	500	28	$2 \times 80$	80	>11 typ. 13	>50 typ. 60

**Ruggedness in class-B operation**

The BLF546 is capable of withstanding a full load mismatch corresponding to  $V_{SWR} = 10$  through all phases under the following conditions:  $V_{DS} = 28$  V;  $f = 500$  MHz at rated output power.

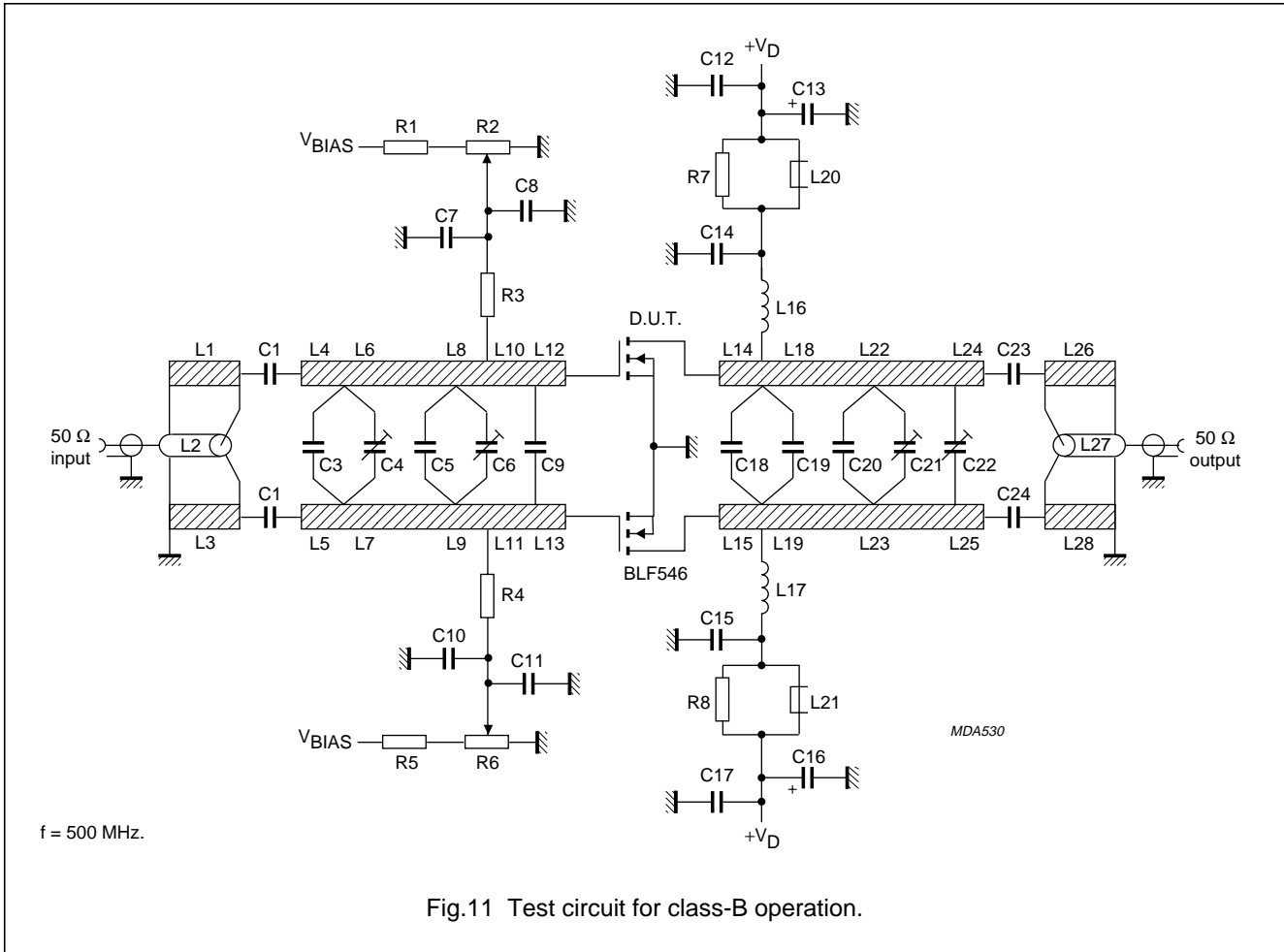
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List of components (see Fig.11)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	33 pF, 500 V		
C3	multilayer ceramic chip capacitor; note 1	11 pF, 500 V		
C4, C6, C21, C22	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor; note 2	12 pF, 500 V		
C7, C10, C14, C15	multilayer ceramic chip capacitor; note 1	390 pF, 500 V		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C9	multilayer ceramic chip capacitor; note 2	39 pF, 500 V		
C13, C16	electrolytic capacitor	4.7 μF, 63 V		2222 030 38478



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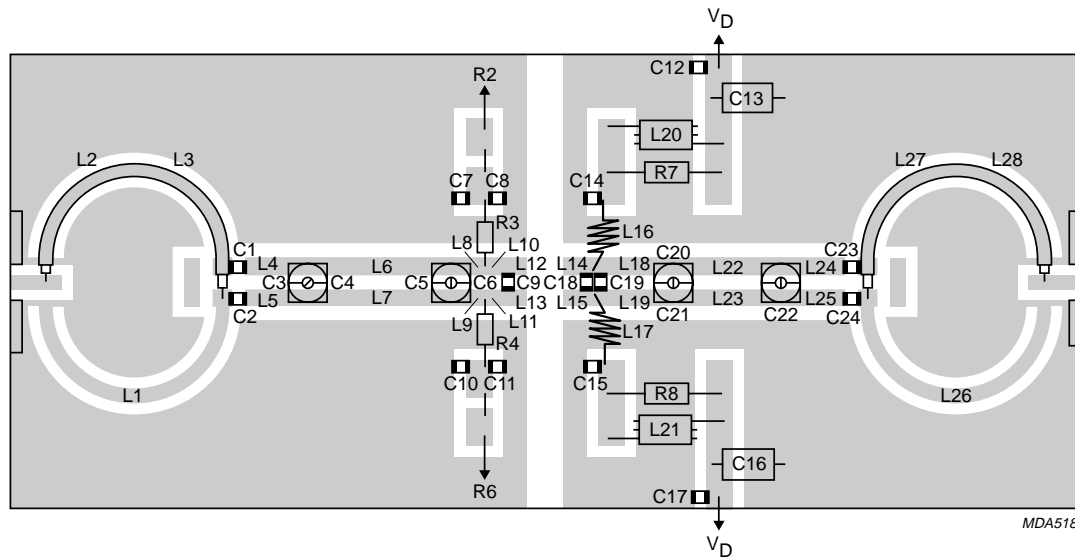
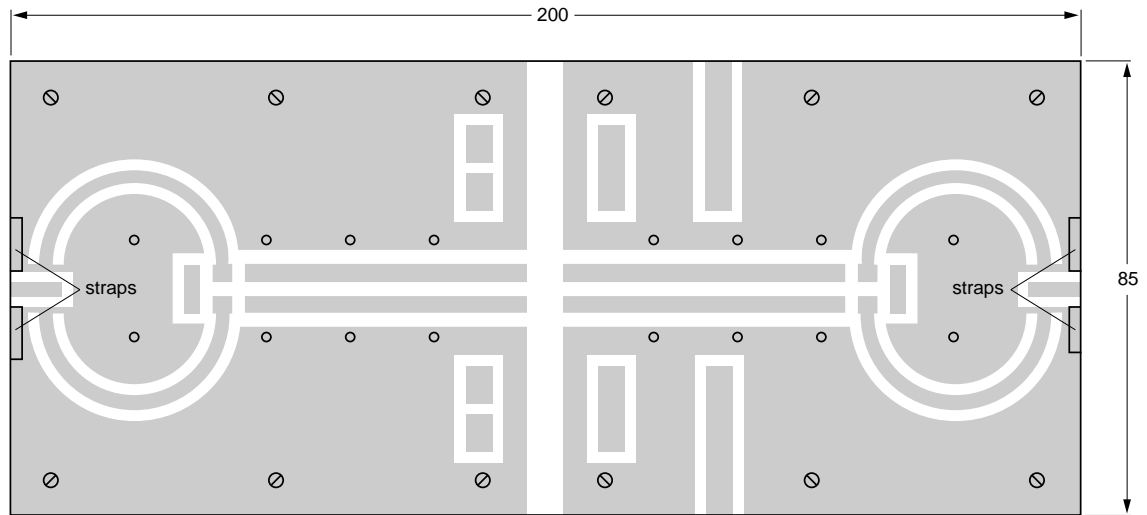
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C18, C19	multilayer ceramic chip capacitor; note 2	18 pF, 500 V		
C20	multilayer ceramic chip capacitor; note 2	15 pF, 500 V		
C23, C24	multilayer ceramic chip capacitor; note 1	15 pF, 500 V		
L1, L3, L26, L28	stripline; note 3	50 $\Omega$	55.6 $\times$ 2.4 mm	
L2	semi-rigid cable; note 4	50 $\Omega$	ext. dia. 2 mm ext. conductor length 55.6 mm	
L4, L5	stripline; note 3	42 $\Omega$	12 $\times$ 3 mm	
L6, L7	stripline; note 3	42 $\Omega$	26.5 $\times$ 3 mm	
L8, L9	stripline; note 3	42 $\Omega$	5.5 $\times$ 3 mm	
L10, L11	stripline; note 3	42 $\Omega$	6 $\times$ 3 mm	
L12, L13	stripline; note 3	42 $\Omega$	3 $\times$ 3 mm	
L14, L15	stripline; note 3	42 $\Omega$	7 $\times$ 3 mm	
L16, L17	3 turns enamelled 1 mm copper wire	15.6 nH	length 8.5 mm int. dia. 5.4 mm leads 2 $\times$ 5 mm	
L18, L19	stripline; note 3	42 $\Omega$	12 $\times$ 3 mm	
L20, L21	grade 3B Ferroxcube RF choke			4312 020 36642
L22, L23	stripline; note 3	42 $\Omega$	20 $\times$ 3 mm	
L24, L25	stripline; note 3	42 $\Omega$	14 $\times$ 3 mm	
L27	semi-rigid cable; note 5	50 $\Omega$	ext. dia. 2 mm ext. conductor length 55.6 mm	
R1, R5	0.4 W metal film resistor	11.5 k $\Omega$		2322 151 71153
R2, R6	10 turns cermet potentiometer	50 k $\Omega$		
R3, R4	0.4 W metal film resistor	10 k $\Omega$		2322 151 71003
R7, R8	1 W metal film resistor	10 $\Omega$		2322 153 51009

**Notes**

- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
- The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ( $\epsilon_r = 2.2$ ); thickness  $\frac{1}{32}$  inch.
- Semi-rigid cable L2 is soldered on to stripline L3.
- Semi-rigid cable L27 is soldered on to stripline L28.

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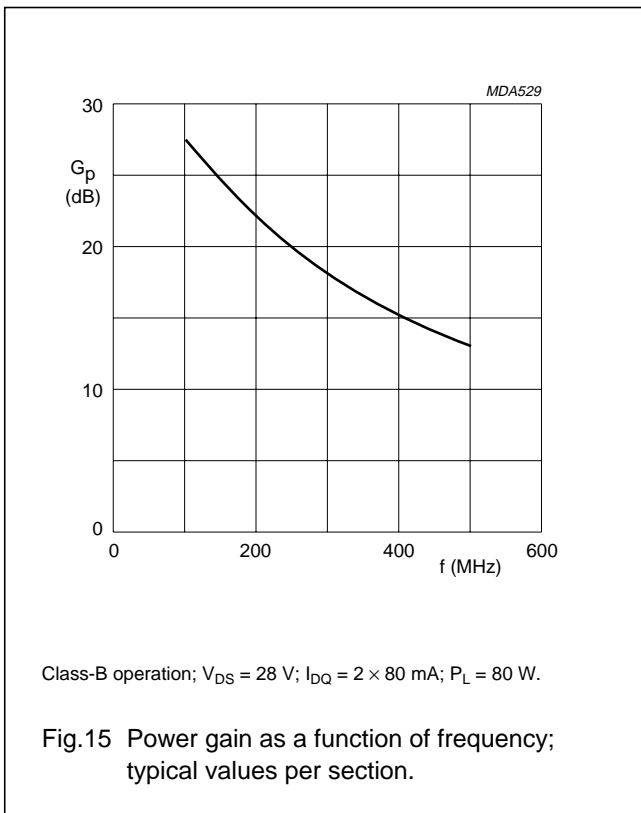
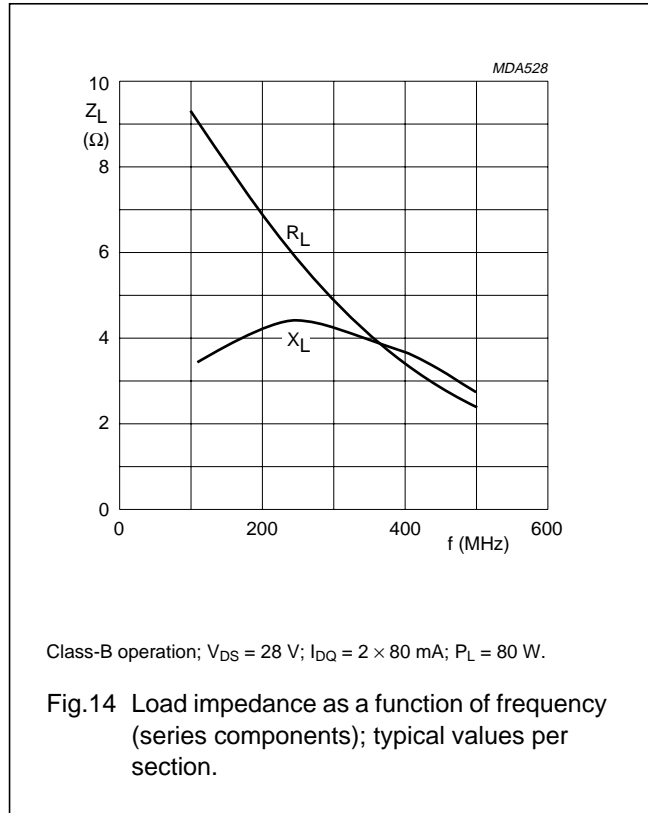
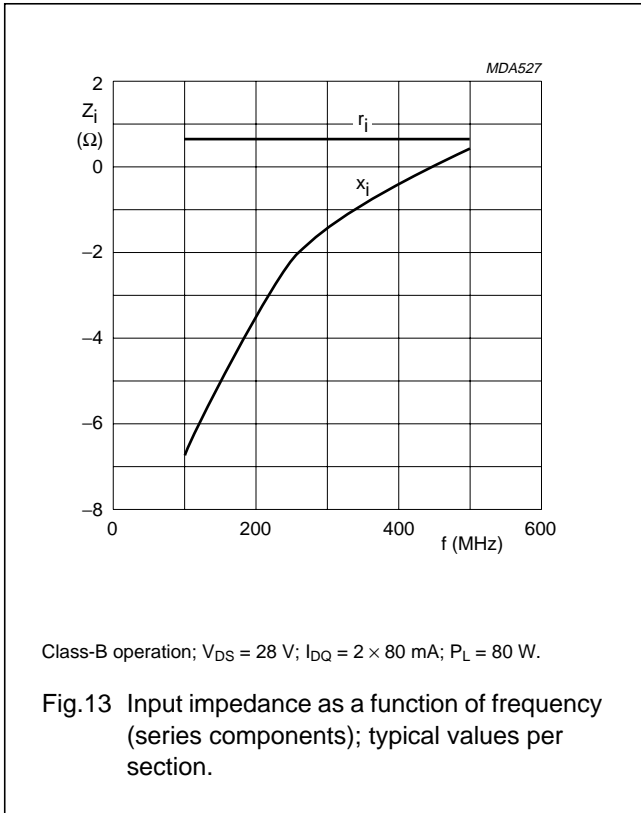
Dimensions in mm.

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.

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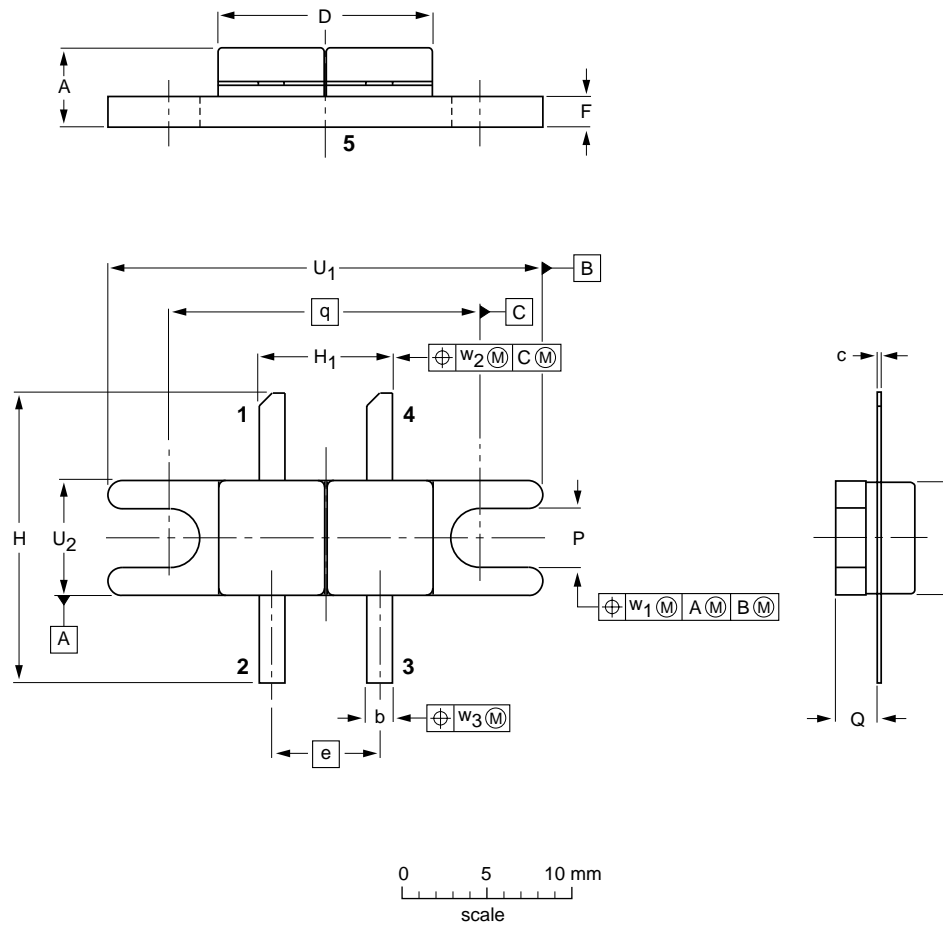
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## PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT268A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	4.91 4.19	1.66 1.39	0.13 0.07	12.96 12.44	6.48 6.22	6.45	2.04 1.77	17.02 16.00	8.23 7.72	3.43 3.17	2.67 2.41	18.42	24.90 24.63	6.61 6.35	0.25	0.51	0.25
inches	0.193 0.165	0.065 0.055	0.005 0.003	0.510 0.490	0.255 0.245	0.254	0.080 0.070	0.670 0.630	0.324 0.304	0.135 0.125	0.105 0.095	0.725	0.980 0.970	0.260 0.250	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT268A						99-03-29

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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