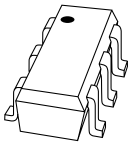


BF1214

Dual N-channel dual gate MOSFET

Rev. 01 — 30 October 2007 Product data sheet

1. Product profile

1.1 General description

The BF1214 is a combination of two dual gate MOSFET amplifiers with shared source and gate2 leads.

The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT363 micro-miniature plastic package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Two low noise gain controlled amplifiers in a single package; both with a partly integrated bias
- Superior cross modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio
- Both amplifiers optimized for VHF applications, yet suitable for VHF and UHF applications

1.3 Applications

- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage
  - digital and analog television tuners
  - professional communication equipment

1.4 Quick reference data

Table 1. Quick reference data for amplifier A and B

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	DC		-	-	6	V
I_D	drain current	DC		-	-	30	mA
P_{tot}	total power dissipation	$T_{sp} \leq 107$ °C	[1]	-	-	180	mW
$\|y_{fs}\|$	forward transfer admittance	f = 100 MHz; T_j = 25 °C; I_D = 18 mA		27	32	37	mS
$C_{iss(G1)}$	input capacitance at gate1	f = 100 MHz	[2]	-	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	f = 100 MHz	[2]	-	20	-	fF
NF	noise figure	f = 400 MHz; $Y_S = Y_{S(opt)}$		-	0.9	1.5	dB
		f = 800 MHz; $Y_S = Y_{S(opt)}$		-	1.2	1.8	dB
Xmod	cross modulation	input level for k = 1 % at 40 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz	[3]	102	105	-	dBμV
T_j	junction temperature			-	-	150	°C

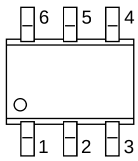
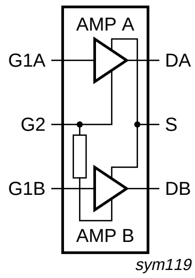
[1] T_{sp} is the temperature at the soldering point of the source lead.

[2] Calculated from S-parameters.

[3] Measured in Figure 24 test circuit.

2. Pinning information

Table 2. Discrete pinning

Pin	Description	Simplified outline	Symbol
1	drain (AMP A)		
2	source		
3	drain (AMP B)		
4	gate1 (AMP B)		
5	gate2		
6	gate1 (AMP A)		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BF1214	-	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking

Type number	Marking	Description
BF1214	SB*	* = p : made in Hong Kong
		* = t : made in Malaysia
		* = w : made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per MOSFET						
V_{DS}	drain-source voltage	DC		-	6	V
I_D	drain current	DC		-	30	mA
I_{G1}	gate1 current			-	±10	mA
I_{G2}	gate2 current			-	±10	mA
P_{tot}	total power dissipation	$T_{sp} \leq 107$ °C	[1]	-	180	mW
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C

[1] T_{sp} is the temperature at the soldering point of the source lead.

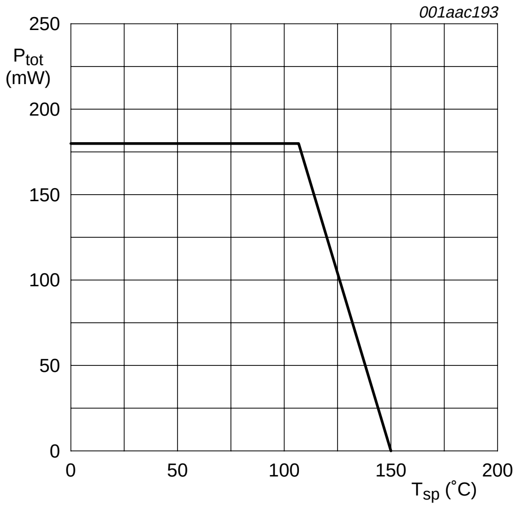


Fig 1. Power derating curve

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		240	K/W

7. Static characteristics

Table 7. Static characteristics

$T_j = 25\,°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per MOSFET; unless otherwise specified						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$ V; $I_D = 10$ µA				
		amplifier A	6	-	-	V
		amplifier B	6	-	-	V
$V_{(BR)G1-SS}$	gate1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ V; $I_{G1-S} = 10$ mA	6	-	10	V
$V_{(BR)G2-SS}$	gate2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ V; $I_{G2-S} = 10$ mA	6	-	10	V
$V_{F(S-G1)}$	forward source-gate1 voltage	$V_{G2-S} = V_{DS} = 0$ V; $I_{S-G1} = 10$ mA	0.5	-	1.5	V
$V_{F(S-G2)}$	forward source-gate2 voltage	$V_{G1-S} = V_{DS} = 0$ V; $I_{S-G2} = 10$ mA	0.5	-	1.5	V
$V_{G1-S(th)}$	gate1-source threshold voltage	$V_{DS} = 5$ V; $V_{G2-S} = 4$ V; $I_D = 100$ µA	0.3	-	1.0	V
$V_{G2-S(th)}$	gate2-source threshold voltage	$V_{DS} = 5$ V; $V_{G1-S} = 5$ V; $I_D = 100$ µA	0.4	-	1.0	V
I_{DS}	drain-source current	$V_{G2-S} = 4$ V [1]				
		amplifier A; $V_{DS(A)} = 5$ V; $R_{G1(A)} = 68$ kΩ	13	-	23	mA
		amplifier B; $V_{DS(B)} = 5$ V; $R_{G1(B)} = 68$ kΩ	13	-	23	mA
I_{G1-S}	gate1 cut-off current	$V_{G2-S} = 0$ V; $V_{DS(A)} = V_{DS(B)} = 0$ V				
		amplifier A; $V_{G1-S(A)} = 5$ V	-	-	50	nA
		amplifier B; $V_{G1-S(B)} = 5$ V	-	-	50	nA
I_{G2-S}	gate2 cut-off current	$V_{G2-S} = 4$ V; $V_{DS(A)} = V_{DS(B)} = 0$ V; $V_{G1-S(A)} = V_{G1-S(B)} = 0$ V	-	-	20	nA

[1] R_{G1} connects gate1 to $V_{GG} = 5$ V.

8. Dynamic characteristics

Table 8. Dynamic characteristics for amplifier A and B

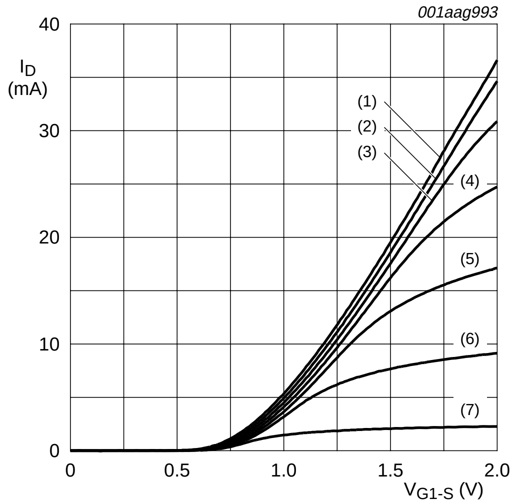
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 18 mA.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\|y_{fs}\|$	forward transfer admittance	f = 100 MHz; T_j = 25 °C		27	32	37	mS
$C_{iss(G1)}$	input capacitance at gate1	f = 100 MHz	[1]	-	2.2	2.7	pF
$C_{iss(G2)}$	input capacitance at gate2	f = 100 MHz	[1]	-	3.5	-	pF
C_{oss}	output capacitance	f = 100 MHz	[1]	-	0.8	-	pF
C_{rss}	reverse transfer capacitance	f = 100 MHz	[1]	-	20	-	fF
G_{tr}	transducer power gain	amplifier A; B_S = $B_{S(opt)}$; B_L = $B_{L(opt)}$	[1]				
		f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS		31	35	39	dB
		f = 400 MHz; G_S = 2 mS; G_L = 1 mS		27	31	35	dB
		f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS		22	26	30	dB
		amplifier B; B_S = $B_{S(opt)}$; B_L = $B_{L(opt)}$	[1]				
		f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS		31	35	39	dB
		f = 400 MHz; G_S = 2 mS; G_L = 1 mS		29	33	37	dB
		f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS		25	29	33	dB
NF	noise figure	f = 11 MHz; G_S = 20 mS; B_S = 0 S		-	3.0	-	dB
		f = 400 MHz; Y_S = $Y_{S(opt)}$		-	0.9	1.5	dB
		f = 800 MHz; Y_S = $Y_{S(opt)}$		-	1.2	1.8	dB
Xmod	cross modulation	input level for k = 1 %; f_w = 50 MHz; f_{unw} = 60 MHz	[2]				
		at 0 dB AGC		90	-	-	dBµV
		at 10 dB AGC		-	94	-	dBµV
		at 20 dB AGC		-	99	-	dBµV
		at 40 dB AGC		102	105	-	dBµV

[1] Calculated from S-parameters.

[2] Measured in Figure 24 test circuit.

8.1 Graphs for amplifier A and B



(1) V_{G2-S} = 4.0 V.

(2) V_{G2-S} = 3.5 V.

(3) V_{G2-S} = 3.0 V.

(4) V_{G2-S} = 2.5 V.

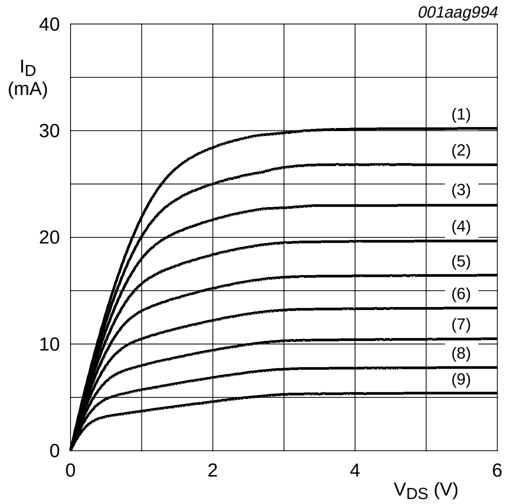
(5) V_{G2-S} = 2.0 V.

(6) V_{G2-S} = 1.5 V.

(7) V_{G2-S} = 1.0 V.

V_{DS} = 5 V; T_j = 25 °C.

Fig 2. Transfer characteristics; typical values



(1) V_{G1-S} = 1.8 V.

(2) V_{G1-S} = 1.7 V.

(3) V_{G1-S} = 1.6 V.

(4) V_{G1-S} = 1.5 V.

(5) V_{G1-S} = 1.4 V.

(6) V_{G1-S} = 1.3 V.

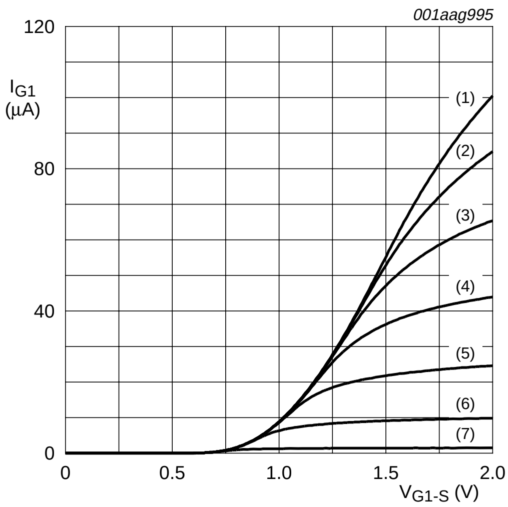
(7) V_{G1-S} = 1.2 V.

(8) V_{G1-S} = 1.1 V.

(9) V_{G1-S} = 1.0 V.

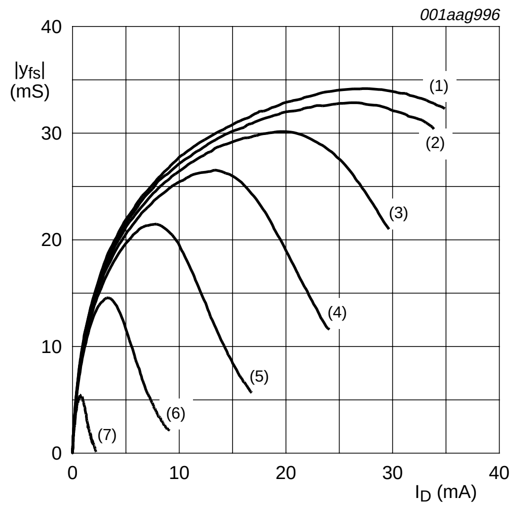
V_{G2-S} = 4 V; T_j = 25 °C.

Fig 3. Output characteristics; typical values



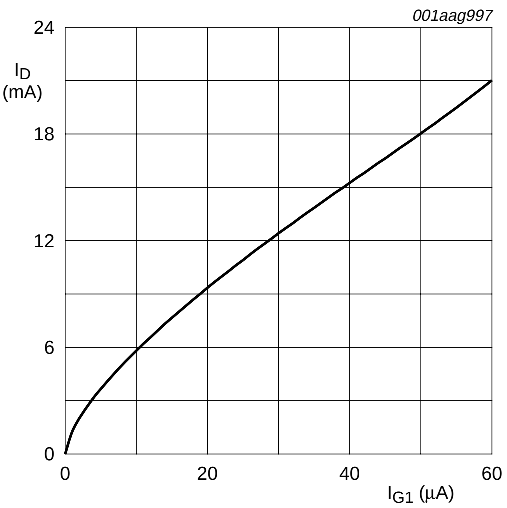
(1) V_{G2-S} = 4.0 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3.0 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2.0 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1.0 V.
V_{DS} = 5 V; T_j = 25 °C.

Fig 4. Gate1 current as a function of gate1 voltage; typical values



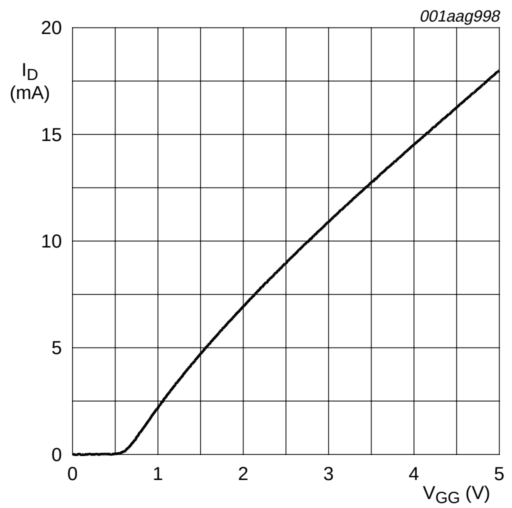
(1) V_{G2-S} = 4.0 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3.0 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2.0 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1.0 V.
V_{DS} = 5 V; T_j = 25 °C.

Fig 5. Forward transfer admittance as a function of drain current; typical values



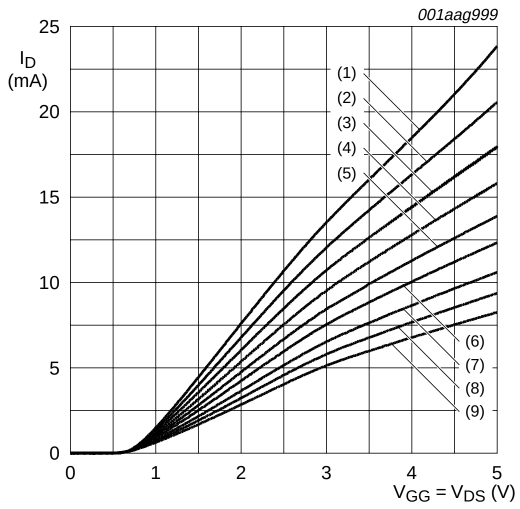
V_{DS} = 5 V; V_{G2-S} = 4 V; T_j = 25 °C.

Fig 6. Drain current as a function of gate1 current; typical values



V_{DS} = 5 V; V_{G2-S} = 4 V; R_{G1} = 68 kΩ; T_j = 25 °C.

Fig 7. Drain current as a function of gate1 supply voltage (V_{GG}); typical values



(1) R_{G1} = 47 kΩ.

(2) R_{G1} = 56 kΩ.

(3) R_{G1} = 68 kΩ.

(4) R_{G1} = 82 kΩ.

(5) R_{G1} = 100 kΩ.

(6) R_{G1} = 120 kΩ.

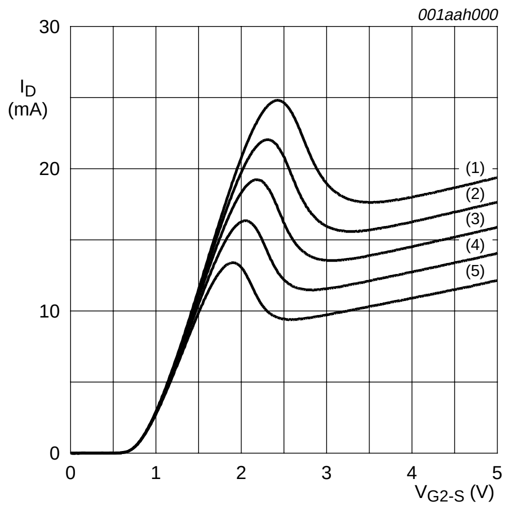
(7) R_{G1} = 150 kΩ.

(8) R_{G1} = 180 kΩ.

(9) R_{G1} = 220 kΩ.

V_{G2-S} = 4 V; T_j = 25 °C.

Fig 8. Drain current as a function of V_{DS} and V_{GG}; typical values



(1) V_{GG} = 5.0 V.

(2) V_{GG} = 4.5 V.

(3) V_{GG} = 4.0 V.

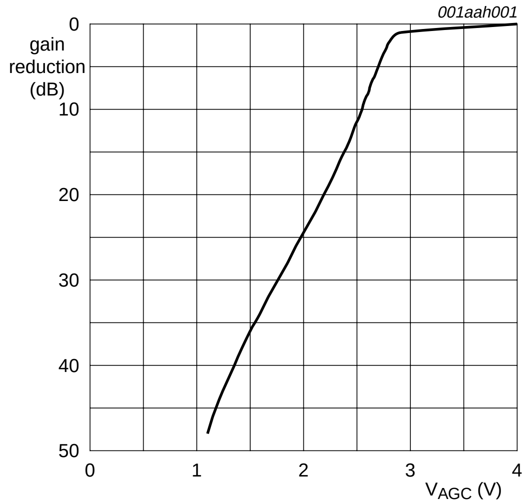
(4) V_{GG} = 3.5 V.

(5) V_{GG} = 3.0 V.

T_j = 25 °C; R_{G1} = 68 kΩ (connected to V_{GG}).

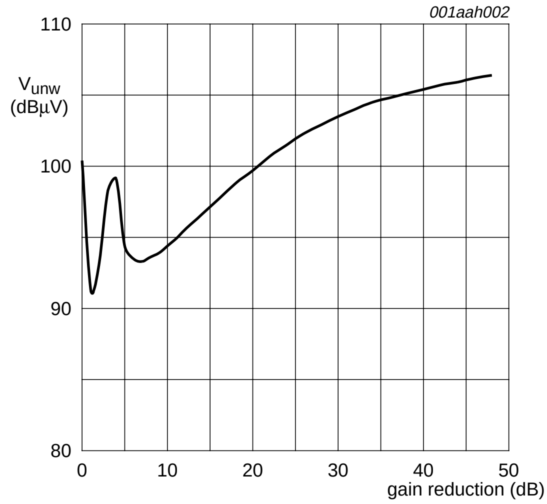
Fig 9. Drain current as a function of gate2 voltage; typical values

8.2 Graphs for amplifier A



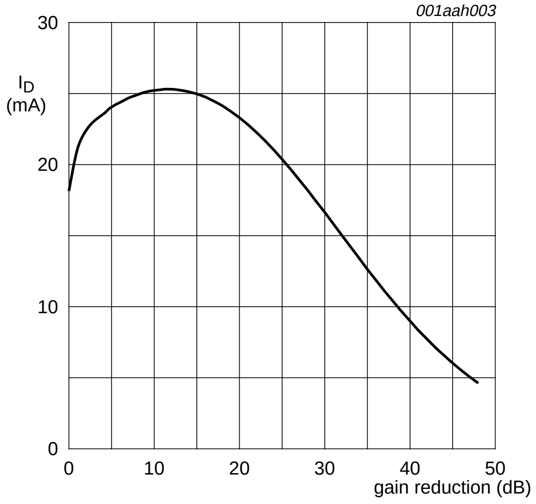
$V_{DS(A)}$ = 5 V; V_{GG} = 5 V; $I_{D(nom)(A)}$ = 18 mA; $R_{G1(A)}$ = 68 kΩ; f_w = 50 MHz; T_{amb} = 25 °C; see Figure 24.

Fig 10. Amplifier A: typical gain reduction as a function of the AGC voltage; typical values



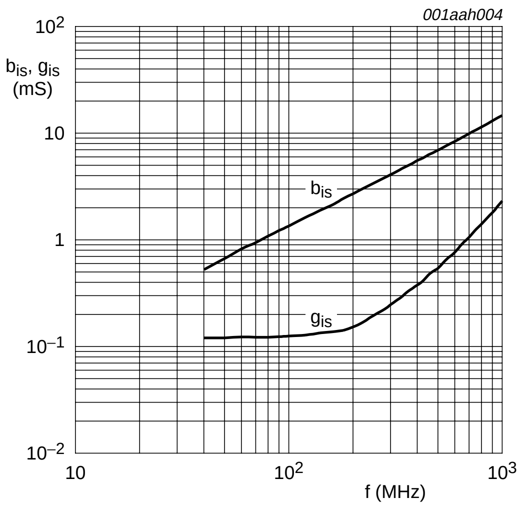
$V_{DS(A)}$ = 5 V; V_{GG} = 5 V; $V_{G2-S(nom)}$ = 4 V; $R_{G1(A)}$ = 68 kΩ; f_w = 50 MHz; f_{unw} = 60 MHz; $I_{D(nom)(A)}$ = 18 mA; T_{amb} = 25 °C; see Figure 24.

Fig 11. Amplifier A: unwanted voltage for 1 % cross modulation as a function of gain reduction; typical values



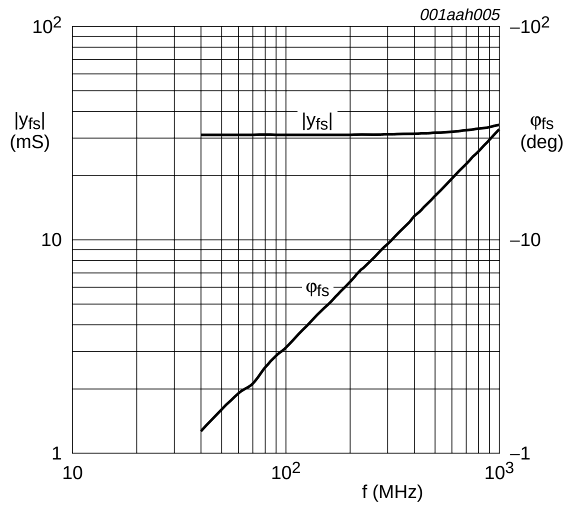
$V_{DS(A)}$ = 5 V; V_{GG} = 5 V; $V_{G2-S(nom)}$ = 4 V; $R_{G1(A)}$ = 68 kΩ; f_w = 50 MHz; $I_{D(nom)(A)}$ = 18 mA; T_{amb} = 25 °C; see Figure 24.

Fig 12. Amplifier A: typical drain current as a function of gain reduction; typical values



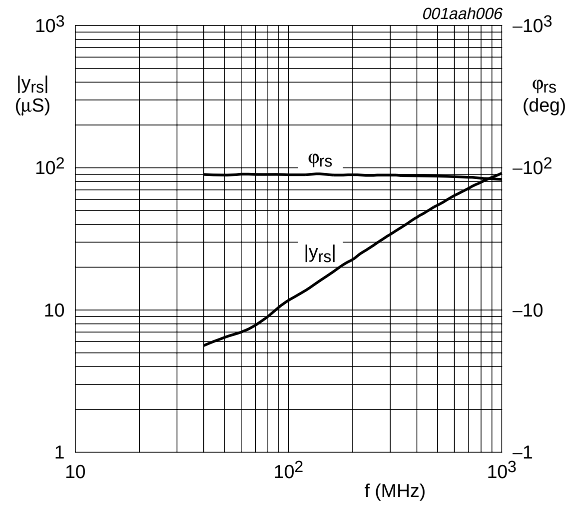
$V_{DS(A)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(B)}$ = 0 V;
$I_{D(A)}$ = 18 mA.

Fig 13. Amplifier A: input admittance as a function of frequency; typical values



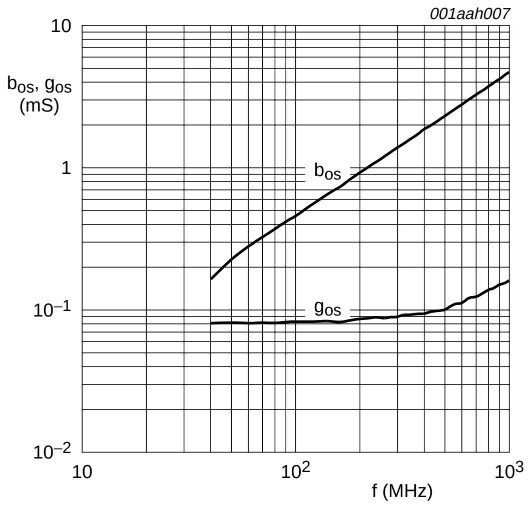
$V_{DS(A)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(B)}$ = 0 V;
$I_{D(A)}$ = 18 mA.

Fig 14. Amplifier A: forward transfer admittance and phase as a function of frequency; typical values



$V_{DS(A)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(B)}$ = 0 V;
$I_{D(A)}$ = 18 mA.

Fig 15. Amplifier A: reverse transfer admittance and phase as a function of frequency; typical values



$V_{DS(A)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(B)}$ = 0 V;
$I_{D(A)}$ = 18 mA.

Fig 16. Amplifier A: output admittance as a function of frequency; typical values

8.2.1 Scattering parameters for amplifier A

Table 9. Scattering parameters for amplifier A

$V_{DS(A)}$ = 5 V; V_{G2-S} = 4 V; $I_{D(A)}$ = 18 mA; $V_{DS(B)}$ = 0 V; $V_{G1-S(B)}$ = 0 V; T_{amb} = 25 °C; typical values.

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)
40	0.9877	–3.07	3.07	176.73	0.0006	88.01	0.9902	–1.00
100	0.9888	–7.81	3.07	171.67	0.0012	85.54	0.9918	–2.74
200	0.9852	–15.61	3.04	163.23	0.0022	80.05	0.9910	–5.50
300	0.9766	–23.41	3.00	154.91	0.0033	75.66	0.9896	–8.22
400	0.9643	–31.14	2.95	146.63	0.0042	71.57	0.9881	–10.93
500	0.9504	–38.62	2.89	138.57	0.0050	67.10	0.9859	–13.61
600	0.9339	–45.96	2.82	130.61	0.0056	63.38	0.9836	–16.28
700	0.9151	–53.13	2.74	122.79	0.0061	59.74	0.9813	–18.96
800	0.8960	–60.18	2.66	115.17	0.0064	56.44	0.9790	–21.60
900	0.8766	–67.00	2.57	107.66	0.0065	53.53	0.9769	–24.20
1000	0.8564	–73.58	2.49	100.35	0.0066	50.29	0.9753	–26.88

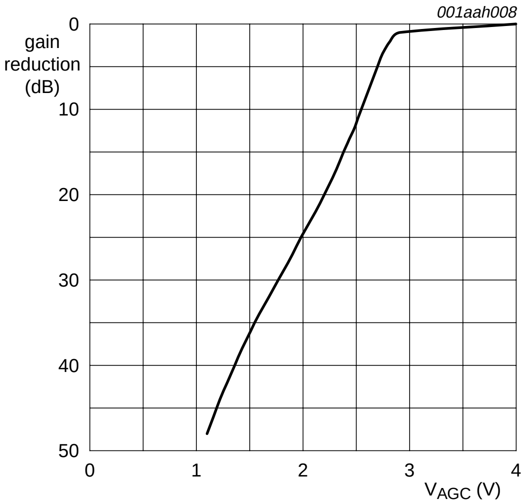
8.2.2 Noise data for amplifier A

Table 10. Noise data for amplifier A

$V_{DS(A)}$ = 5 V; V_{G2-S} = 4 V; $I_{D(A)}$ = 18 mA; T_{amb} = 25 °C; typical values.

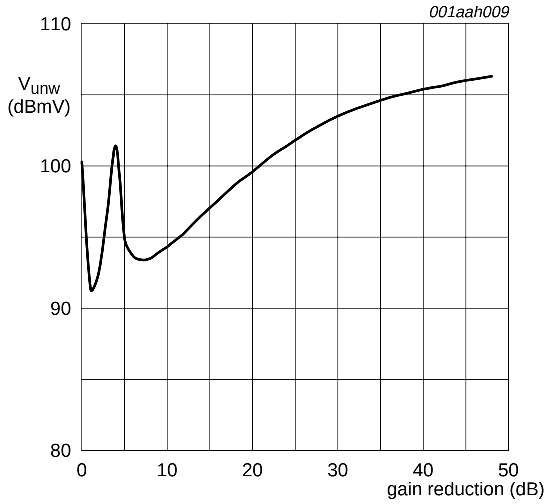
f (MHz)	NF_{min} (dB)	Γ_{opt}		r_n (ratio)
		(ratio)	(deg)	
400	0.91	0.76	23.60	0.677
800	1.23	0.71	48.91	0.620

8.3 Graphs for amplifier B



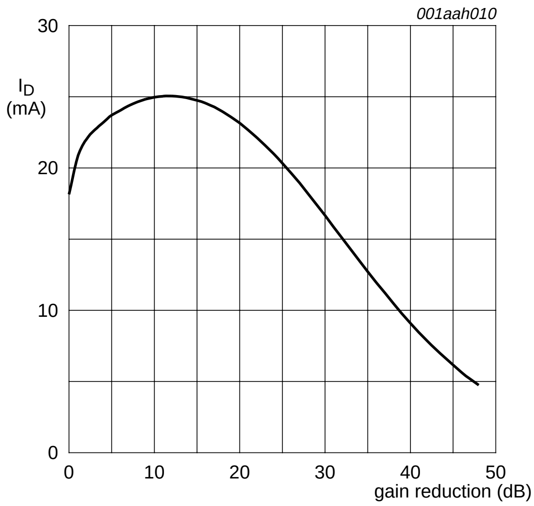
$V_{DS(B)}$ = 5 V; V_{GG} = 5 V; $I_{D(nom)(B)}$ = 18 mA; $R_{G1(B)}$ = 68 kΩ; f_w = 50 MHz; T_{amb} = 25 °C; see Figure 24.

Fig 17. Amplifier B: typical gain reduction as a function of the AGC voltage; typical values



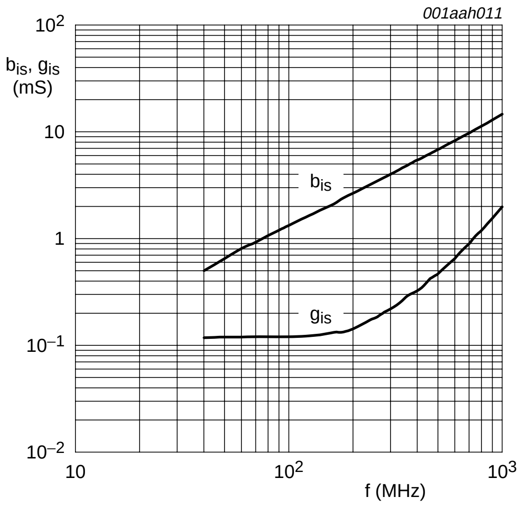
$V_{DS(B)}$ = 5 V; V_{GG} = 5 V; $V_{G2\text{-}S(nom)}$ = 4 V; $R_{G1(B)}$ = 68 kΩ; f_w = 50 MHz; f_{unw} = 60 MHz; $I_{D(nom)(B)}$ = 18 mA; T_{amb} = 25 °C; see Figure 24.

Fig 18. Amplifier B: unwanted voltage for 1 % cross modulation as a function of gain reduction; typical values



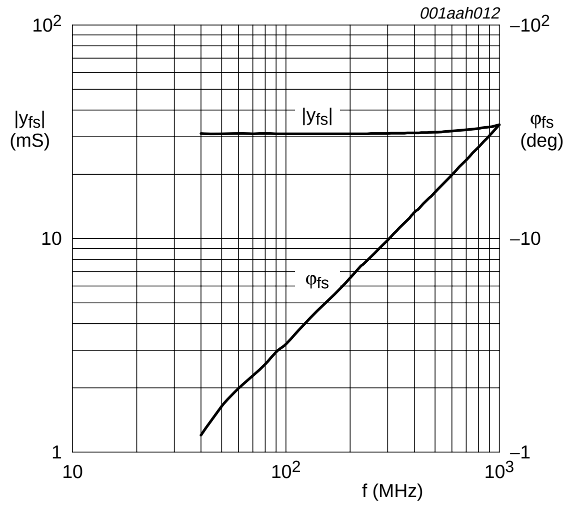
$V_{DS(B)}$ = 5 V; V_{GG} = 5 V; $V_{G2\text{-}S(nom)}$ = 4 V; $R_{G1(B)}$ = 68 kΩ; $I_{D(nom)(B)}$ = 18 mA; f_w = 50 MHz; T_{amb} = 25 °C; see Figure 24.

Fig 19. Amplifier B: typical drain current as a function of gain reduction; typical values



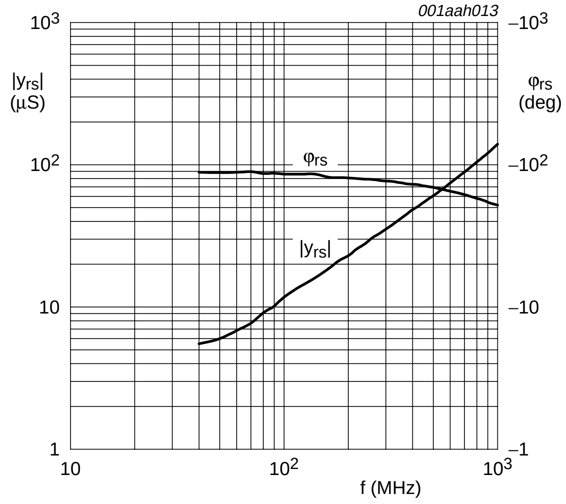
$V_{DS(B)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $V_{DS(A)}$ = 0 V;
$I_{D(B)}$ = 18 mA.

Fig 20. Amplifier B: input admittance as a function of frequency; typical values



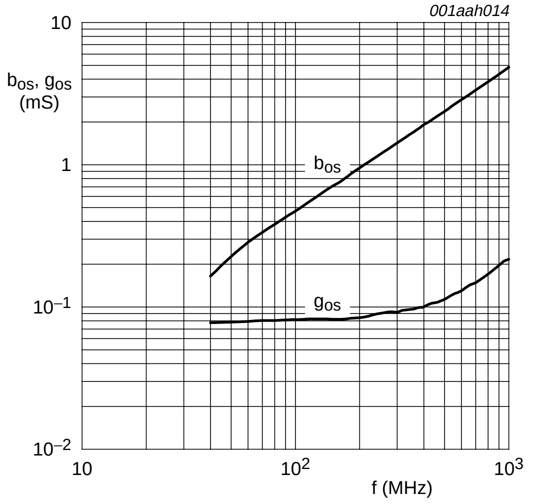
$V_{DS(B)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $V_{DS(A)}$ = 0 V;
$I_{D(B)}$ = 18 mA.

Fig 21. Amplifier B: forward transfer admittance and phase as a function of frequency; typical values



$V_{DS(B)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $V_{DS(A)}$ = 0 V;
$I_{D(B)}$ = 18 mA.

Fig 22. Amplifier B: reverse transfer admittance and phase as a function of frequency; typical values



$V_{DS(B)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $V_{DS(A)}$ = 0 V;
$I_{D(B)}$ = 18 mA.

Fig 23. Amplifier B: output admittance as a function of frequency; typical values

8.3.1 Scattering parameters for amplifier B

Table 11. Scattering parameters for amplifier B

$V_{DS(B)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $I_{D(B)}$ = 18 mA; $V_{DS(A)}$ = 0 V; $V_{G1\text{-}S(A)}$ = 0 V; T_{amb} = 25 °C; typical values.

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)
40	0.9836	–2.92	3.06	176.89	0.0005	89.71	0.9897	–0.98
100	0.9890	–7.68	3.06	171.63	0.0012	92.19	0.9920	–2.79
200	0.9869	–15.32	3.03	163.14	0.0023	88.94	0.9914	–5.62
300	0.9801	–23.00	2.99	154.74	0.0034	87.64	0.9902	–8.42
400	0.9704	–30.69	2.94	146.34	0.0045	86.52	0.9889	–11.21
500	0.9595	–38.13	2.88	138.13	0.0056	85.29	0.9869	–14.01
600	0.9458	–45.45	2.81	129.99	0.0066	84.60	0.9845	–16.81
700	0.9300	–52.67	2.73	121.93	0.0075	83.78	0.9818	–19.64
800	0.9132	–59.82	2.65	114.01	0.0085	82.86	0.9786	–22.44
900	0.8959	–66.74	2.56	106.18	0.0093	81.97	0.9750	–25.22
1000	0.8775	–73.43	2.47	98.51	0.0101	80.62	0.9717	–28.10

8.3.2 Noise data for amplifier B

Table 12. Noise data for amplifier B

$V_{DS(B)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $I_{D(B)}$ = 18 mA; T_{amb} = 25 °C; typical values.

f (MHz)	NF_{min} (dB)	Γ_{opt}		r_n (ratio)
		(ratio)	(deg)	
400	0.91	0.76	22.58	0.690
800	1.24	0.71	47.34	0.620

9. Test information

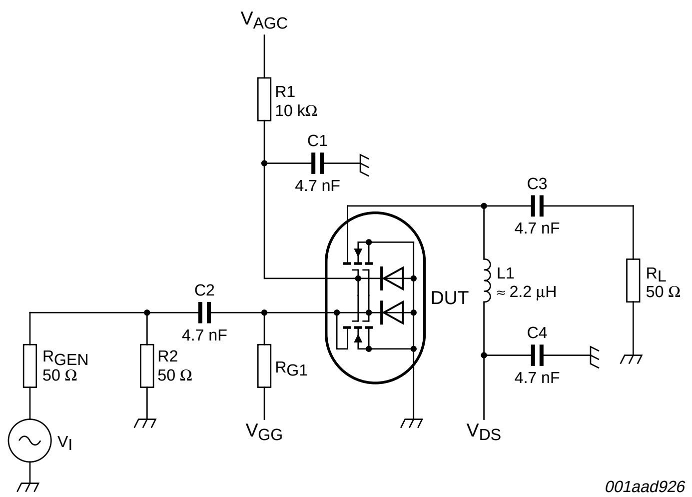
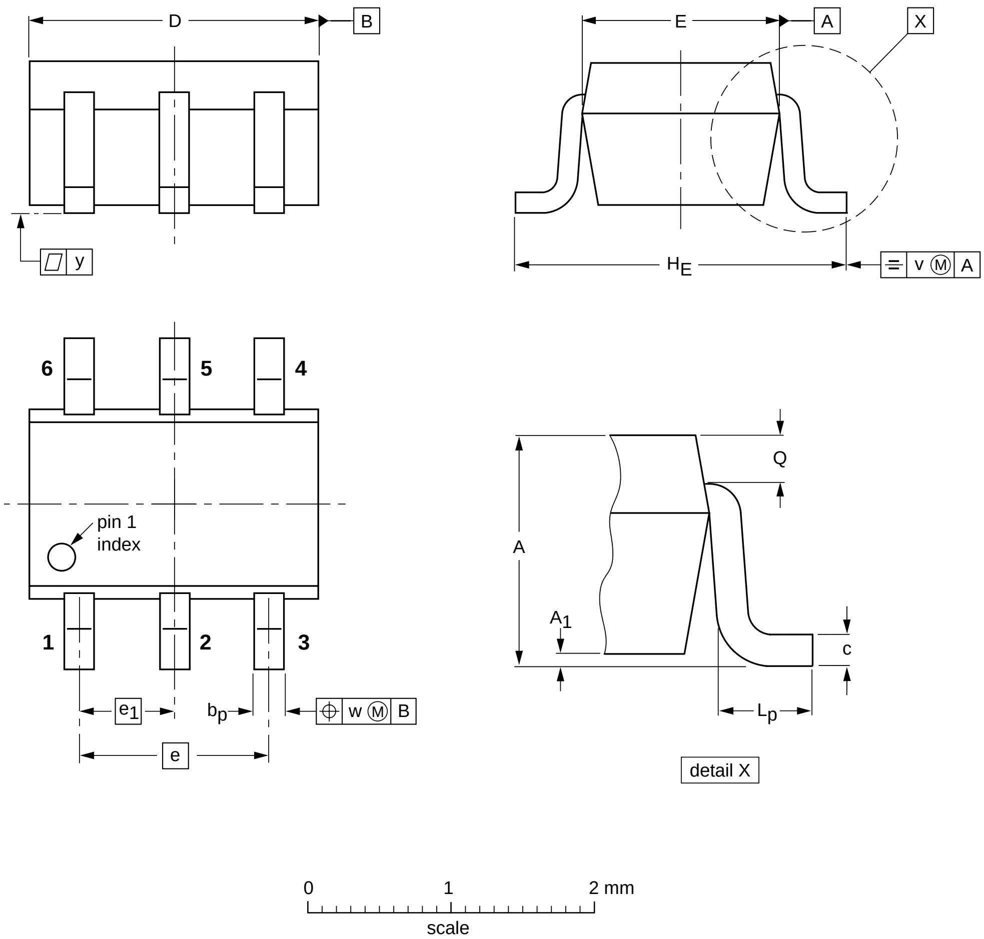


Fig 24. Cross modulation test setup (for one MOSFET)

10. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig 25. Package outline SOT363

11. Abbreviations

Table 13. Abbreviations

Acronym	Description
AGC	Automatic Gain Control
DC	Direct Current
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
UHF	Ultra High Frequency
VHF	Very High Frequency

12. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF1214_1	20071030	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

13.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 30 October 2007

Document identifier: BF1214_1