BLF346

VHF power MOS transistor

Rev. 6 — 1 September 2015

AMPLEON

Product data sheet

IMPORTANT NOTICE

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Ampleon

VHF power MOS transistor BLF346

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

APPLICATIONS

- Linear amplifier applications in television transmitters and transposers.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor encapsulated in a 6-lead, SOT119A flange package, with a ceramic cap. All leads are isolated from the flange. A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the General Section of the associated Data Handbook for further information.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT119A

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

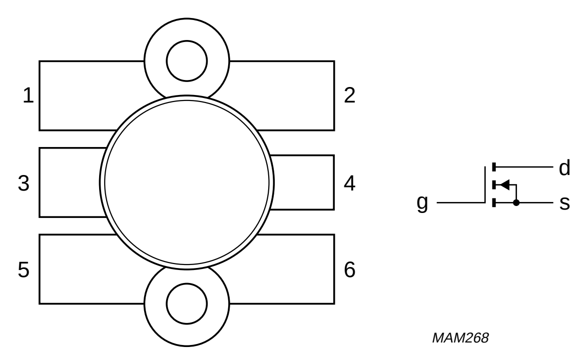

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance in a linear amplifier.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	P_L (W)	G_p (dB)	d_{im} (dB) (1)
Class-A	224.25	28	3	70	>24	>14	–52
				25	typ. 30	typ. 16.5	–52

Note

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak synchronization level.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

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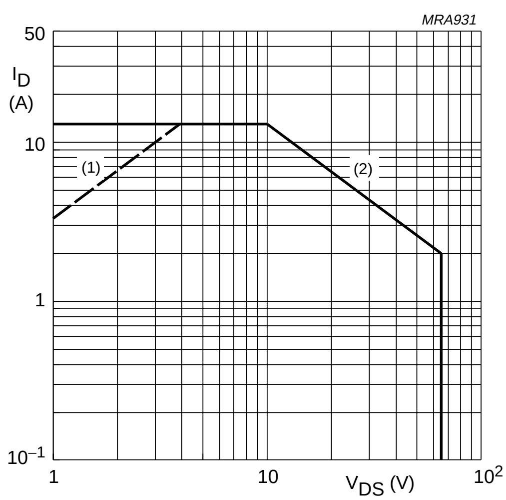
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	13	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	130	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

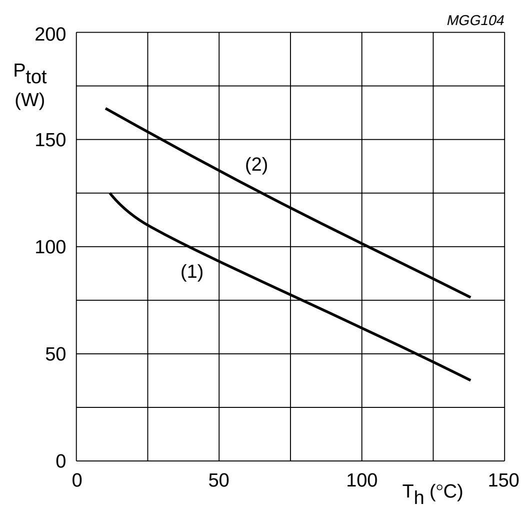
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 130 W	1.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 130 W	0.2	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

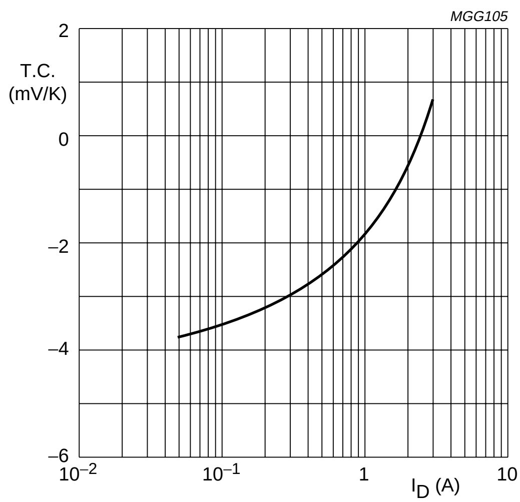
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 50 mA	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	V_{DS} = 10 V; I_D = 50 mA	–	–	100	mV
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	3	4.2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	22	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	225	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	180	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF

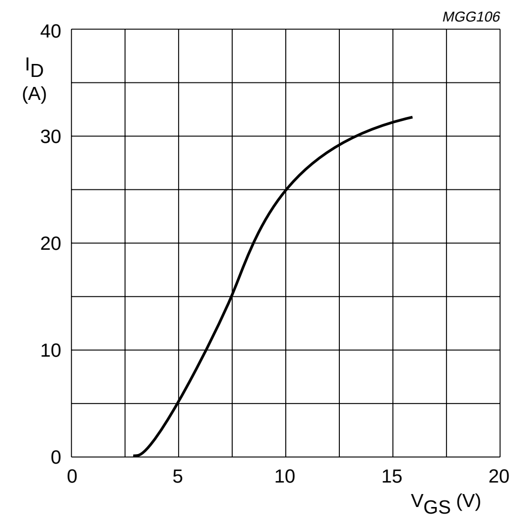
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



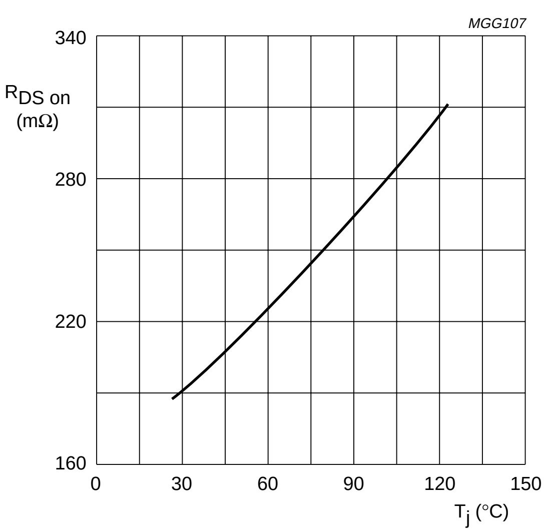
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



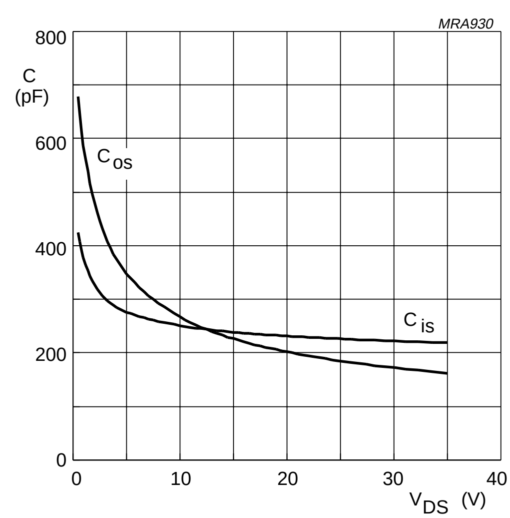
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.



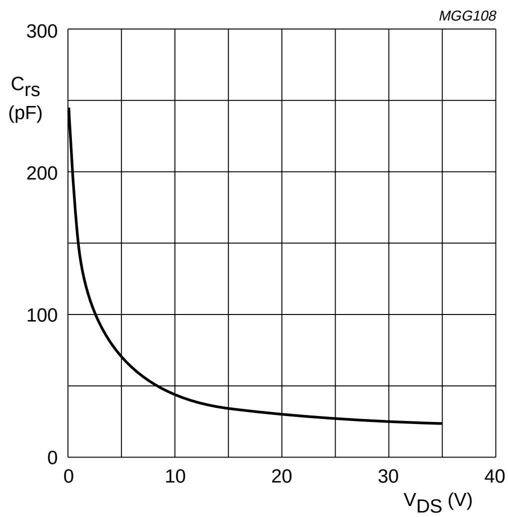
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

APPLICATION INFORMATION

RF performance in a linear amplifier (common source class-A circuit).
$R_{th\ mb\text{-}h}$ = 0.2 K/W; Z_L = 1.1 + j0.2 Ω unless otherwise specified.

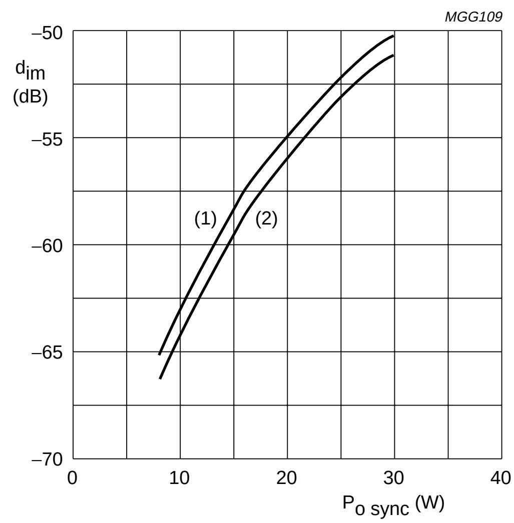
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB) (1)
Class-A	224.25	28	3	70	>24	>14	–52
				25	typ. 30	typ. 16.5	–52
				70	typ. 20	typ. 14.5	–55
				25	typ. 22	typ. 15	–55

Note

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak synchronization level.

Ruggedness in class-A operation

The BLF346 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 225 MHz at rated output power.



(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.9 Intermodulation distortion as a function of peak synchronized output power.

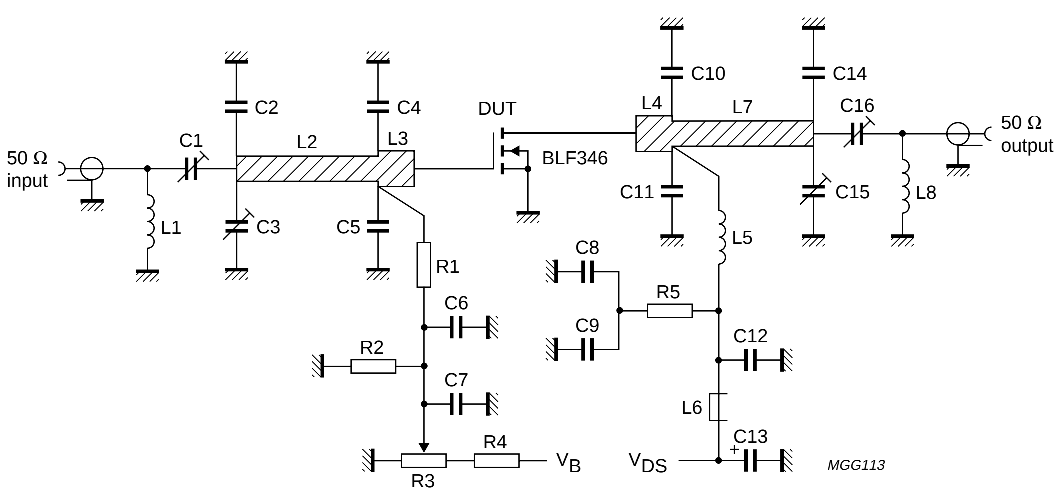


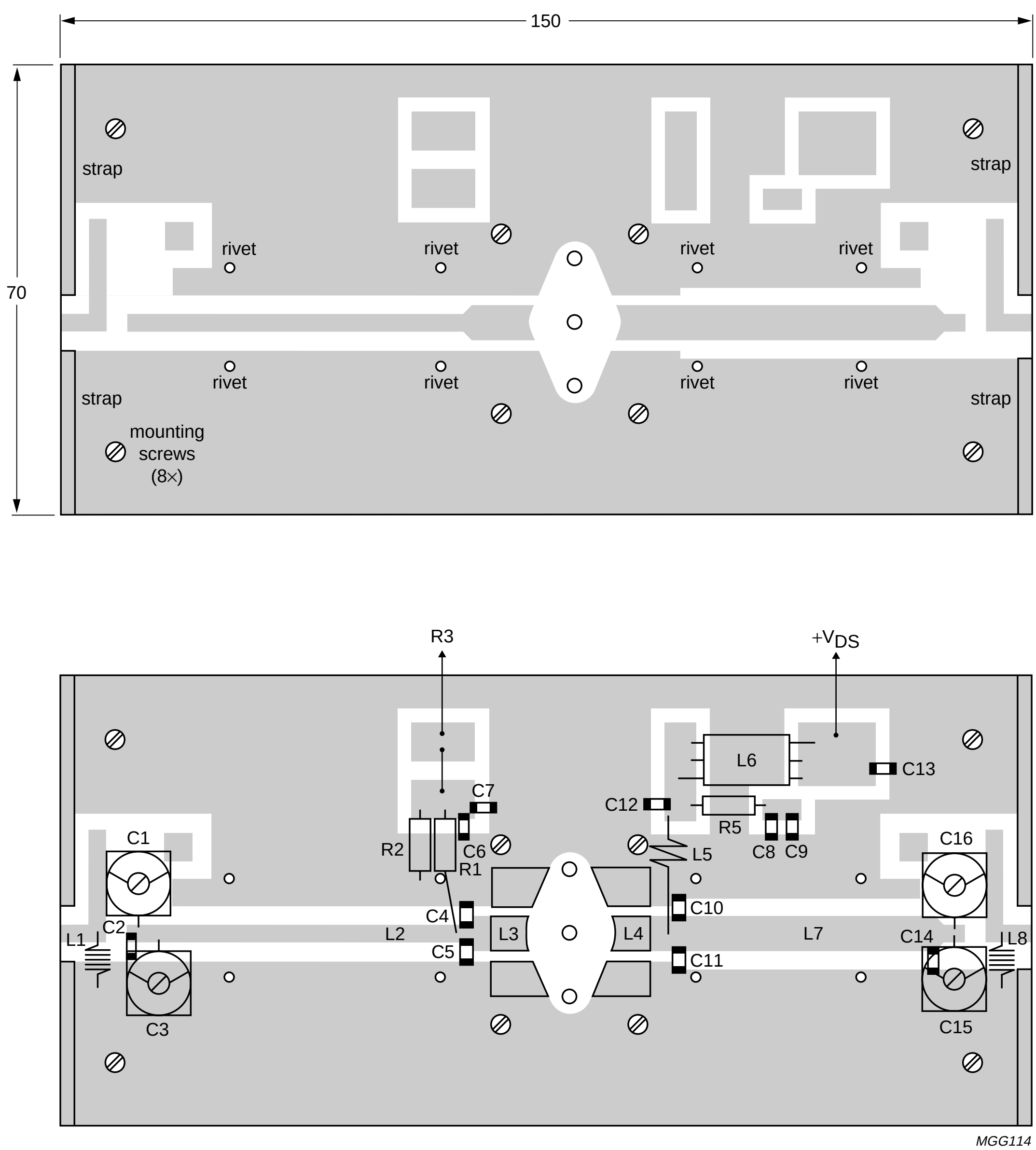
Fig.10 Test circuit for class-A operation at f = 225 MHz.

List of components (see Figs 10 and 11).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	2 to 18 pF		2222 809 09003
C2	multilayer ceramic chip capacitor; note 1	10 pF, 500 V		
C3, C15, C16	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4, C5	multilayer ceramic chip capacitor; note 1	56 pF, 500 V		
C6, C12	multilayer ceramic chip capacitor; note 1	680 pF, 500 V		
C7, C8, C9	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C10, C11	multilayer ceramic chip capacitor; note 1	43 pF, 500 V		
C13	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C14	multilayer ceramic chip capacitor; note 1	27 pF, 500 V		
L1	4 turns enamelled 0.7 mm copper wire	42.4 nH	length 4 mm; int. dia. 3 mm; leads 2 × 5 mm	
L2	stripline; note 2	50 Ω	length 49 mm; width 2.8 mm	
L3, L4	stripline; note 2	31 Ω	length 11.5 mm; width 6 mm	
L5	2 turns enamelled 1.5 mm copper wire	18.7 nH	length 8 mm; int. dia. 4 mm; leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
L7	stripline; note 2	31 Ω	length 40 mm; width 6 mm	
L8	3 turns enamelled 1.5 mm copper wire	28.8 nH	length 8 mm; int. dia. 4 mm; leads 2 × 5 mm	
R1	metal film resistor	1 kΩ, 0.4 W		2322 151 71002
R2	metal film resistor	100 kΩ, 0.4 W		2322 151 71004
R3	10 turns cermet potentiometer	100 Ω		
R4	metal film resistor	316 kΩ, 0.4 W		2322 153 53161
R5	metal film resistor	10 Ω, 0.4 W		2322 153 51009

Notes

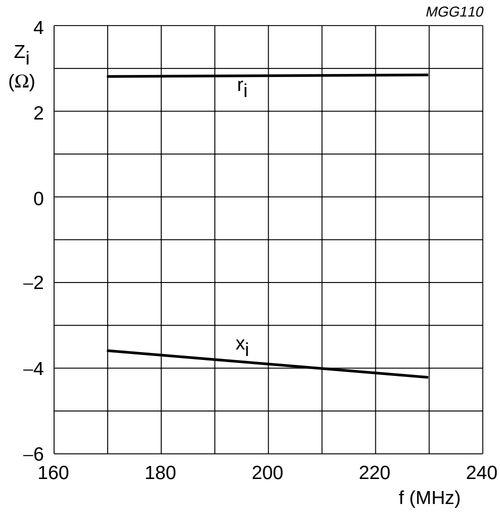
1. American Technical Ceramics capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed-circuit board with epoxy fibre-glass dielectric (ε_r = 4.5); thickness $^1/_{16}$ inch.



Dimensions in mm.

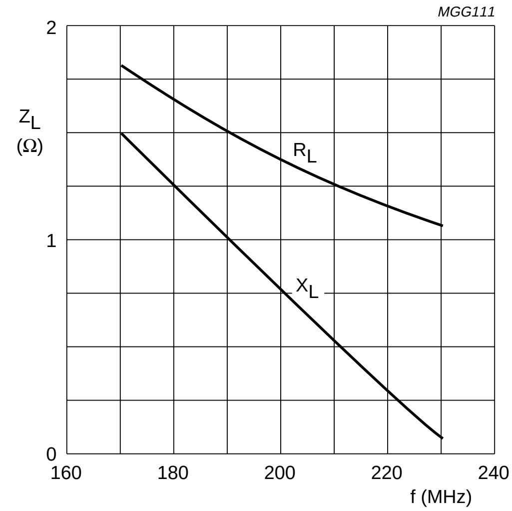
The circuit and components are situated on one side of the printed-circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.11 Component layout for 225 MHz class-A test circuit.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.12 Input impedance as a function of frequency (series components); typical values.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.13 Load impedance as a function of frequency (series components); typical values.

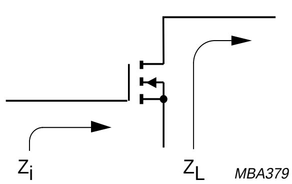
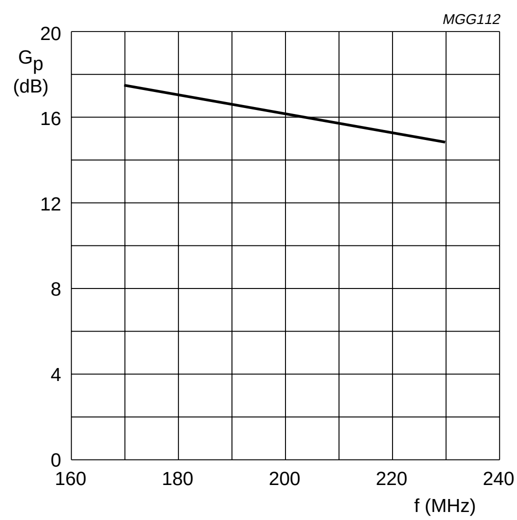


Fig.14 Definition of MOS impedance.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.15 Power gain as a function of frequency; typical values.

BLF346 scattering parameters

V_{DS} = 28 V; I_D = 3000 mA; note 1.

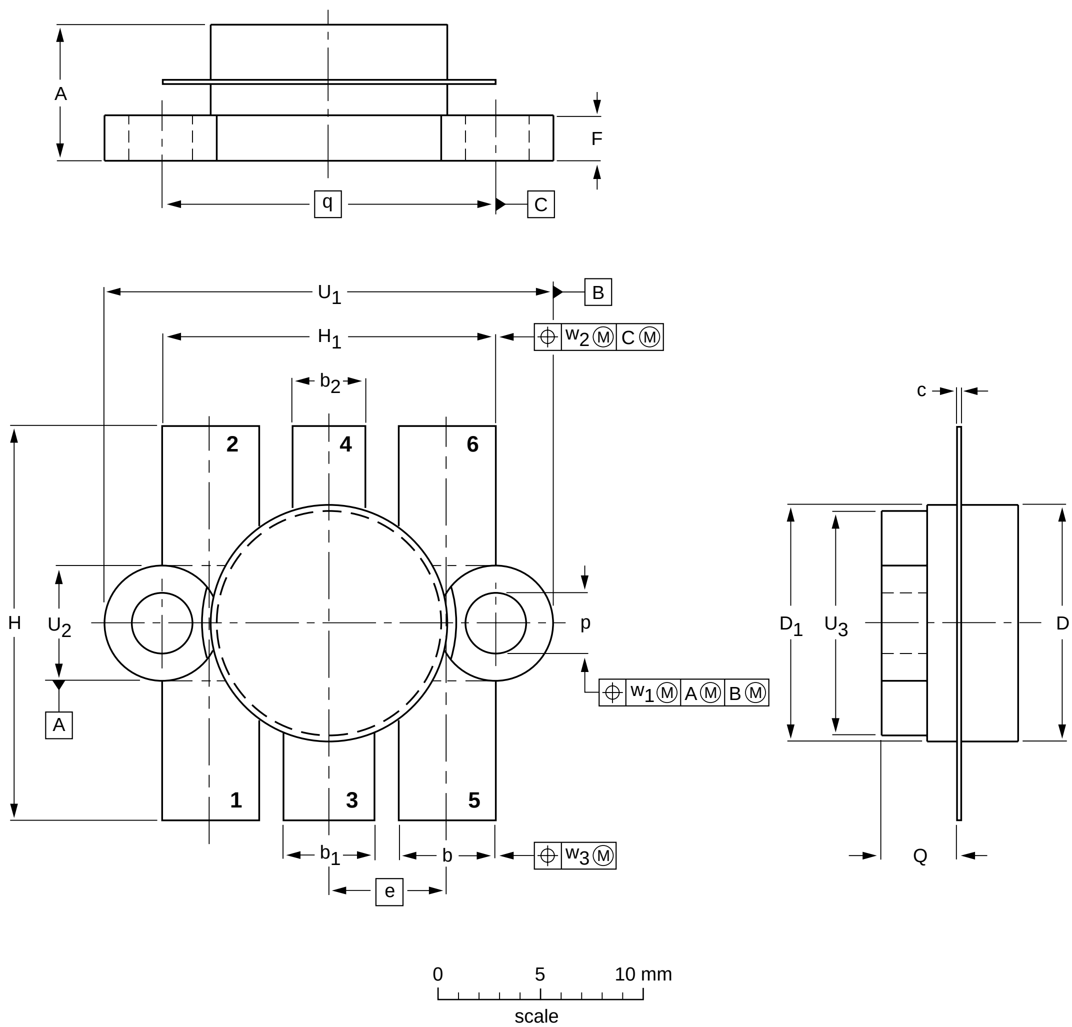
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	$\|s_{11}\|$	∠ Φ	$\|s_{21}\|$	∠ Φ	$\|s_{12}\|$	∠ Φ	$\|s_{22}\|$	∠ Φ
100	0.91	–178.9	2.12	67.7	0.01	–0.6	0.88	–177.3
105	0.91	–179.0	2.01	66.6	0.01	–0.4	0.88	–177.4
110	0.92	–179.1	1.91	65.5	0.01	–0.1	0.88	–177.4
115	0.92	–179.2	1.81	64.5	0.01	0.2	0.88	–177.4
120	0.92	–179.3	1.72	63.5	0.01	0.5	0.89	–177.4
130	0.92	–179.5	1.56	61.5	0.01	1.3	0.89	–177.5
140	0.92	–179.7	1.43	59.6	0.01	2.5	0.89	–177.5
150	0.93	–179.9	1.31	58.0	0.01	4.1	0.90	–177.6
160	0.93	180.0	1.21	56.3	0.01	6.0	0.90	–177.7
170	0.93	179.8	1.12	54.7	0.01	8.2	0.90	–177.8
180	0.93	179.5	1.04	53.0	0.01	10.5	0.91	–177.9
190	0.93	179.3	0.97	51.2	0.01	13.0	0.91	–178.0
200	0.94	179.1	0.91	49.6	0.01	15.7	0.91	–178.1
225	0.94	178.5	0.77	46.1	0.01	23.9	0.92	–178.5
250	0.95	178.0	0.66	43.3	0.01	33.6	0.93	–178.9
275	0.95	177.4	0.58	40.1	0.01	43.6	0.94	–179.3
300	0.95	176.7	0.50	37.5	0.01	51.8	0.94	–179.7
350	0.96	175.5	0.40	33.5	0.01	65.7	0.95	179.4
400	0.97	174.8	0.32	30.6	0.01	74.5	0.96	178.4
450	0.97	173.6	0.27	27.7	0.01	80.0	0.97	177.4
500	0.98	172.5	0.22	25.8	0.02	83.0	0.97	176.4
600	0.99	170.3	0.16	24.0	0.02	86.7	0.98	174.6
700	1.00	168.2	0.13	24.7	0.03	88.5	0.99	172.8
800	1.05	165.0	0.10	27.6	0.03	90.1	0.99	170.9
900	1.03	158.5	0.09	31.5	0.04	91.0	1.00	168.9
1000	1.00	156.6	0.08	38.7	0.04	92.1	1.00	167.1

Note

1. For more extensive s-parameters see internet: http://www.semiconductors.philips.com/markets/communications/wirelesscommunications/broadcast

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 6 leads **SOT119A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	b_2	c	D	D_1	e	F	H	H_1	p	Q	q	U_1	U_2	U_3	w_1	w_2	w_3
mm	7.39 6.32	5.59 5.33	5.34 5.08	4.07 3.81	0.15 0.10	12.86 12.59	12.83 12.57	6.48	2.54 2.29	21.97 21.21	18.55 18.28	3.30 3.05	4.57 4.06	18.42	24.89 24.64	6.48 6.22	12.32 12.07	0.25	0.51	0.25
inches	0.291 0.249	0.220 0.210	0.210 0.200	0.160 0.150	0.006 0.004	0.505 0.496	0.505 0.495	0.255	0.100 0.090	0.865 0.835	0.730 0.720	0.130 0.120	0.180 0.160	0.725	0.980 0.970	0.255 0.245	0.485 0.475	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT119A						99-03-29

VHF power MOS transistor BLF346

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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