

NTB0101-Q100

Dual supply translating transceiver; auto direction sensing;
3-state

Rev. 1 — 3 July 2014

Product data sheet

1. General description

The NTB0101-Q100 is a 1-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2 V and 3.6 V. $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V. It makes the device suitable for translating between the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V).

Pins A and OE are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Wide supply voltage range:
 - ◆ $V_{CC(A)}$: 1.2 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- ESD protection:
 - ◆ MIL-STD-883, method 3015 Class 2 exceeds 2500 V for A port
 - ◆ MIL-STD-883, method 3015 Class 3B exceeds 15000 V for B port
 - ◆ HBM JESD22-A114E Class 2 exceeds 2500 V for A port
 - ◆ HBM JESD22-A114E Class 3B exceeds 15000 V for B port
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
NTB0101GW-Q100	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
NTB0101GW-Q100	t1

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

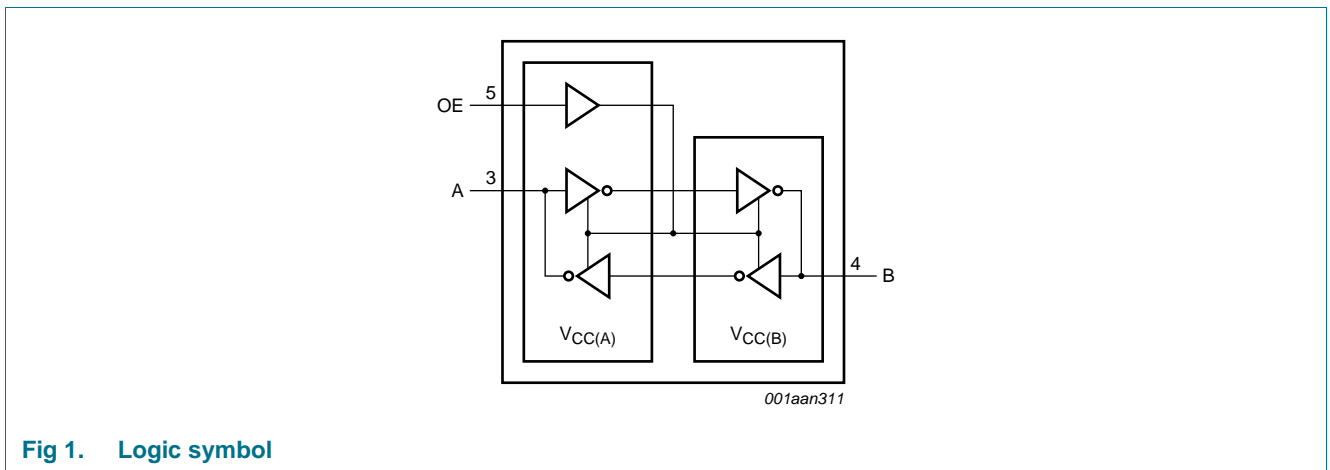


Fig 1. Logic symbol

6. Pinning information

6.1 Pinning

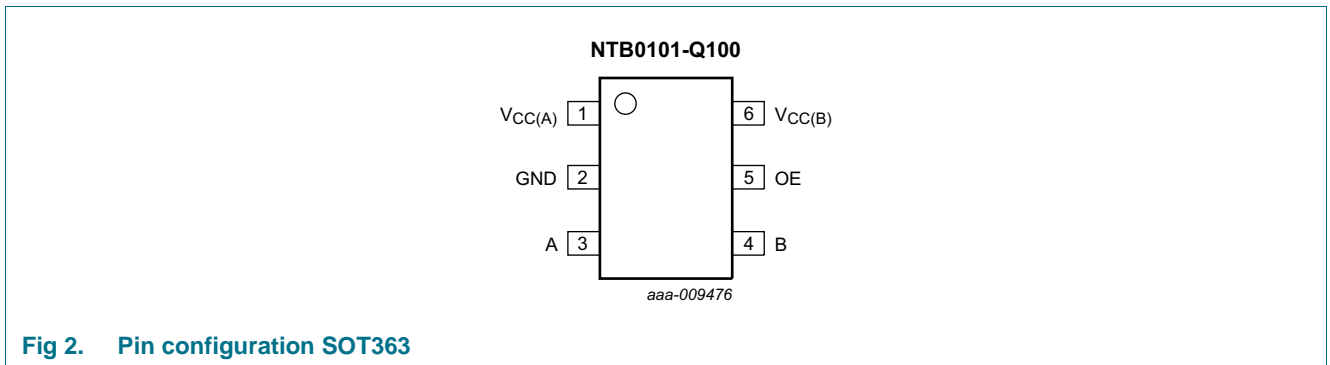


Fig 2. Pin configuration SOT363

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V _{CC(A)}	1	supply voltage A
GND	2	ground (0 V)
A	3	data input or output (referenced to V _{CC(A)})
B	4	data input or output (referenced to V _{CC(B)})
OE	5	output enable input (active HIGH; referenced to V _{CC(A)})
V _{CC(B)}	6	supply voltage B

7. Functional description

Table 4. Function table^[1]

Supply voltage		Input	Input/output	
V _{CC(A)}	V _{CC(B)}	OE	A	B
1.2 V to V _{CC(B)}	1.65 V to 5.5 V	L	Z	Z
1.2 V to V _{CC(B)}	1.65 V to 5.5 V	H	input or output	output or input
GND ^[2]	GND ^[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either V_{CC(A)} or V_{CC(B)} is at GND level, the device goes into Power-down mode.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(A)}	supply voltage A		-0.5	+6.5	V
V _{CC(B)}	supply voltage B		-0.5	+6.5	V
V _I	input voltage		^[1] -0.5	+6.5	V
V _O	output voltage	Active mode	^{[1][2][3]} -0.5	V _{CCO} + 0.5	V
		Power-down or 3-state mode	^[1] -0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	V _O = 0 V to V _{CCO}	^[2] -	±50	mA
I _{CC}	supply current	I _{CC(A)} or I _{CC(B)}	-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[4] -	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

[3] V_{CCO} + 0.5 V should not exceed 6.5 V.

[4] For SC-88 package: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions^{[1][2]}

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.2	3.6	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Power-down or 3-state mode; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$			
		A port	0	3.6	V
		B port	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	40	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

10. Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	A port; $V_{CC(A)} = 1.2\text{ V}; I_O = -20\text{ }\mu\text{A}$	-	1.1	-	V
V_{OL}	LOW-level output voltage	A port; $V_{CC(A)} = 1.2\text{ V}; I_O = 20\text{ }\mu\text{A}$	-	0.09	-	V
I_I	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}; V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	-	± 1	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V to }V_{CCO}; V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	[1]	-	± 1	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V to }3.6\text{ V};$ $V_{CC(A)} = 0\text{ V}; V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	-	± 1	μA
		B port; V_I or $V_O = 0\text{ V to }5.5\text{ V};$ $V_{CC(B)} = 0\text{ V}; V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	-	± 1	μA
C_I	input capacitance	OE input; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	1.0	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	4.0	-	pF
		B port; $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V}; V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	7.5	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

[2] V_{CCI} is the supply voltage associated with the input.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	10	10	10	10	10	20	10	1050	nA
1.5 V	10	10	10	10	10	10	10	650	nA
1.8 V	10	10	10	10	10	10	10	350	nA
2.5 V	-	-	10	10	10	10	10	40	nA
3.3 V	-	-	-	-	10	10	10	10	nA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	0.65 V_{CCI}	-	0.65 V_{CCI}	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input [1]					
		$V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	0.35 V_{CCI}	-	0.35 V_{CCI}	V
V_{OH}	HIGH-level output voltage	$I_O = -20\text{ }\mu\text{A}$ [2]					
		A port; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}$	$V_{CCO} - 0.4$	-	$V_{CCO} - 0.4$	-	V
		B port; $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	$V_{CCO} - 0.4$	-	$V_{CCO} - 0.4$	-	V
V_{OL}	LOW-level output voltage	$I_O = 20\text{ }\mu\text{A}$ [2]					
		A port; $V_{CC(A)} = 1.4\text{ V to }3.6\text{ V}$	-	0.4	-	0.4	V
		B port; $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	0.4	-	0.4	V
I_I	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V};$ $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	± 2	-	± 5	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO};$ $V_{CC(A)} = 1.2\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$ [2]	-	± 2	-	± 10	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V to }3.6\text{ V};$ $V_{CC(A)} = 0\text{ V}; V_{CC(B)} = 0\text{ V to }5.5\text{ V}$	-	± 2	-	± 10	μA
		B port; V_I or $V_O = 0\text{ V to }5.5\text{ V};$ $V_{CC(B)} = 0\text{ V}; V_{CC(A)} = 0\text{ V to }3.6\text{ V}$	-	± 2	-	± 10	μA

Table 9. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{CC}	supply current	V _I = 0 V or V _{CCI} ; I _O = 0 A [1]					
		I _{CC(A)}					
		OE = LOW; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	3	-	15	μA
		OE = HIGH; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	3	-	20	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	2	-	15	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V	-	-2	-	-15	μA
		I _{CC(B)}					
		OE = LOW; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	5	-	15	μA
		OE = HIGH; V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	5	-	20	μA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	-2	-	-15	μA
		V _{CC(A)} = 0 V; V _{CC(B)} = 5.5 V	-	2	-	15	μA
		I _{CC(A)} + I _{CC(B)}					
V _{CC(A)} = 1.4 V to 3.6 V; V _{CC(B)} = 1.65 V to 5.5 V	-	8	-	40	μA		

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

11. Dynamic characteristics

Table 10. Typical dynamic characteristics for temperature 25 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for waveforms, see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V _{CC(B)}				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
V_{CC(A)} = 1.2 V							
t _{pd}	propagation delay	A to B	5.9	4.8	4.4	4.2	ns
		B to A	5.6	4.8	4.5	4.4	ns
t _{en}	enable time	OE to A, B	0.5	0.5	0.5	0.5	μs
t _{dis}	disable time	OE to A; no external load [2]	6.9	6.9	6.9	6.9	ns
		OE to B; no external load [2]	9.5	8.6	8.5	8.0	ns
		OE to A	81	69	83	68	ns
		OE to B	81	69	83	68	ns

Table 10. Typical dynamic characteristics for temperature 25 °C^[1] ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for waveforms, see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V _{CC(B)}				Unit
			1.8 V	2.5 V	3.3 V	5.0 V	
t _t	transition time	A port	4.0	4.0	4.1	4.1	ns
		B port	2.6	2.0	1.7	1.4	ns
t _W	pulse width	data inputs	15	13	13	13	ns
f _{data}	data rate		70	80	80	80	Mbps

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}.

- [2] Delay between OE going LOW and when the outputs are disabled.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V _{CC(B)}								Unit
			1.8 V ± 0.15		2.5 V ± 0.2		3.3 V ± 0.3		5.0 V ± 0.5		
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.5 V ± 0.1											
t _{pd}	propagation delay	A to B	1.4	12.9	1.2	10.1	1.1	10.0	0.8	9.9	ns
		B to A	0.9	14.2	0.7	12.0	0.4	11.7	0.3	13.7	ns
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load ^[2]	1.0	11.9	1.0	11.9	1.0	11.9	1.0	11.9	ns
		OE to B; no external load ^[2]	1.0	16.9	1.0	15.2	1.0	14.1	1.0	13.8	ns
		OE to A	-	320	-	260	-	260	-	280	ns
		OE to B	-	200	-	200	-	200	-	200	ns
t _t	transition time	A port	0.9	5.1	0.9	5.1	0.9	5.1	0.9	5.1	ns
		B port	0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
t _W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f _{data}	data rate		-	40	-	40	-	40	-	40	Mbps
V_{CC(A)} = 1.8 V ± 0.15											
t _{pd}	propagation delay	A to B	1.6	11.0	1.4	7.7	1.3	6.8	1.2	6.5	ns
		B to A	1.5	12.0	1.3	8.4	1.0	7.6	0.9	7.1	ns
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load ^[2]	1.0	11.0	1.0	11.0	1.0	11.0	1.0	11.0	ns
		OE to B; no external load ^[2]	1.0	15.4	1.0	13.5	1.0	12.4	1.0	12.1	ns
		OE to A	-	260	-	230	-	230	-	230	ns
		OE to B	-	200	-	200	-	200	-	200	ns
t _t	transition time	A port	0.8	4.1	0.8	4.1	0.8	4.1	0.8	4.1	ns
		B port	0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
t _W	pulse width	data inputs	20	-	17	-	17	-	17	-	ns
f _{data}	data rate		-	49	-	60	-	60	-	60	Mbps

Table 11. Dynamic characteristics for temperature range $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ ^[1] ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$								Unit
			$1.8\text{ V} \pm 0.15$		$2.5\text{ V} \pm 0.2$		$3.3\text{ V} \pm 0.3$		$5.0\text{ V} \pm 0.5$		
			Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 2.5\text{ V} \pm 0.2$											
t_{pd}	propagation delay	A to B	-	-	1.1	6.3	1.0	5.2	0.9	4.7	ns
		B to A	-	-	1.2	6.6	1.1	5.1	0.9	4.4	ns
t_{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load ^[2]	-	-	1.0	9.2	1.0	9.2	1.0	9.2	ns
		OE to B; no external load ^[2]	-	-	1.0	11.9	1.0	10.7	1.0	10.2	ns
		OE to A	-	-	-	200	-	200	-	200	ns
		OE to B	-	-	-	200	-	200	-	200	ns
t_t	transition time	A port	-	-	0.7	3.0	0.7	3.0	0.7	3.0	ns
		B port	-	-	0.7	3.2	0.5	2.5	0.4	2.7	ns
t_W	pulse width	data inputs	-	-	12	-	10	-	10	-	ns
f_{data}	data rate		-	-	-	85	-	100	-	100	Mbps
$V_{CC(A)} = 3.3\text{ V} \pm 0.3$											
t_{pd}	propagation delay	A to B	-	-	-	-	0.9	4.7	0.8	4.0	ns
		B to A	-	-	-	-	1.0	4.9	0.9	3.8	ns
t_{en}	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	μs
t_{dis}	disable time	OE to A; no external load ^[2]	-	-	-	-	1.0	9.2	1.0	9.2	ns
		OE to B; no external load ^[2]	-	-	-	-	1.0	10.1	1.0	9.6	ns
		OE to A	-	-	-	-	-	260	-	260	ns
		OE to B	-	-	-	-	-	200	-	200	ns
t_t	transition time	A port	-	-	-	-	0.7	2.5	0.7	2.5	ns
		B port	-	-	-	-	0.5	2.5	0.4	2.7	ns
t_W	pulse width	data inputs	-	-	-	-	10	-	10	-	ns
f_{data}	data rate		-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .
 t_t is the same as t_{THL} and t_{TLH} .

[2] Delay between OE going LOW and when the outputs are disabled.

Table 12. Dynamic characteristics for temperature range –40 °C to +125 °C^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V _{CC(B)}								Unit
			1.8 V ± 0.15		2.5 V ± 0.2		3.3 V ± 0.3		5.0 V ± 0.5		
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 1.5 V ± 0.1											
t _{pd}	propagation delay	A to B	1.4	15.9	1.2	13.1	1.1	13.0	0.8	12.9	ns
		B to A	0.9	17.2	0.7	15.0	0.4	14.7	0.3	16.7	ns
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load [2]	1.0	12.5	1.0	12.5	1.0	12.5	1.0	12.5	ns
		OE to B; no external load [2]	1.0	18.1	1.0	16.2	1.0	14.9	1.0	14.6	ns
		OE to A	-	340	-	280	-	280	-	300	ns
		OE to B	-	220	-	220	-	220	-	220	ns
t _t	transition time	A port	0.9	7.1	0.9	7.1	0.9	7.1	0.9	7.1	ns
		B port	0.9	6.5	0.6	5.2	0.5	4.8	0.4	4.7	ns
t _W	pulse width	data inputs	25	-	25	-	25	-	25	-	ns
f _{data}	data rate		-	40	-	40	-	40	-	40	Mbps
V_{CC(A)} = 1.8 V ± 0.15											
t _{pd}	propagation delay	A to B	1.6	14.0	1.4	10.7	1.3	9.8	1.2	9.5	ns
		B to A	1.5	15.0	1.3	11.4	1.0	10.6	0.9	10.1	ns
t _{en}	enable time	OE to A, B	-	1.0	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load [2]	1.0	11.5	1.0	11.5	1.0	11.5	1.0	11.5	ns
		OE to B; no external load [2]	1.0	16.5	1.0	14.5	1.0	13.3	1.0	12.7	ns
		OE to A	-	280	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	-	220	ns
t _t	transition time	A port	0.8	6.2	0.8	6.1	0.8	6.1	0.8	6.1	ns
		B port	0.9	5.8	0.6	5.2	0.5	4.8	0.4	4.7	ns
t _W	pulse width	data inputs	22	-	19	-	19	-	19	-	ns
f _{data}	data rate		-	45	-	55	-	55	-	55	Mbps
V_{CC(A)} = 2.5 V ± 0.2											
t _{pd}	propagation delay	A to B	-	-	1.1	9.3	1.0	8.2	0.9	7.7	ns
		B to A	-	-	1.2	9.6	1.1	8.1	0.9	7.4	ns
t _{en}	enable time	OE to A, B	-	-	-	1.0	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load [2]	-	-	1.0	9.6	1.0	9.6	1.0	9.6	ns
		OE to B; no external load [2]	-	-	1.0	12.6	1.0	11.4	1.0	10.8	ns
		OE to A	-	-	-	220	-	220	-	220	ns
		OE to B	-	-	-	220	-	220	-	220	ns
t _t	transition time	A port	-	-	0.7	5.0	0.7	5.0	0.7	5.0	ns
		B port	-	-	0.7	4.6	0.5	4.8	0.4	4.7	ns
t _W	pulse width	data inputs;	-	-	14	-	13	-	10	-	ns
f _{data}	data rate		-	-	-	75	-	80	-	100	Mbps

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C^[1] ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	V _{CC(B)}								Unit
			1.8 V ± 0.15		2.5 V ± 0.2		3.3 V ± 0.3		5.0 V ± 0.5		
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC(A)} = 3.3 V ± 0.3											
t _{pd}	propagation delay	A to B	-	-	-	-	0.9	7.7	0.8	7.0	ns
		B to A	-	-	-	-	1.0	7.9	0.9	6.8	ns
t _{en}	enable time	OE to A, B	-	-	-	-	-	1.0	-	1.0	µs
t _{dis}	disable time	OE to A; no external load ^[2]	-	-	-	-	1.0	9.5	1.0	9.5	ns
		OE to B; no external load ^[2]	-	-	-	-	1.0	10.7	1.0	9.6	ns
		OE to A	-	-	-	-	-	280	-	280	ns
		OE to B	-	-	-	-	-	220	-	220	ns
t _t	transition time	A port	-	-	-	-	0.7	4.5	0.7	4.5	ns
		B port	-	-	-	-	0.5	4.1	0.4	4.7	ns
t _W	pulse width	data inputs	-	-	-	-	10	-	10	-	ns
f _{data}	data rate		-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
 t_{en} is the same as t_{PZL} and t_{PZH}.
 t_{dis} is the same as t_{PLZ} and t_{PHZ}.
 t_t is the same as t_{THL} and t_{TLH}.

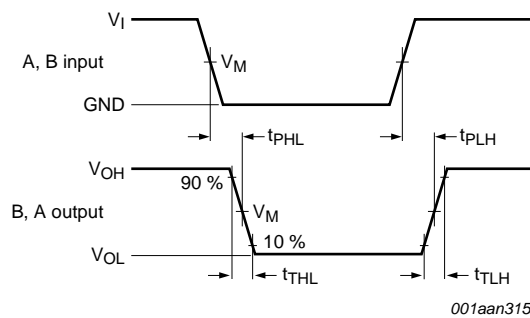
[2] Delay between OE going LOW and when the outputs are disabled.

Table 13. Typical power dissipation capacitance
 Voltages are referenced to GND (ground = 0 V); $T_{amb} = 25\text{ }^{\circ}\text{C}$. [1][2]

Symbol	Parameter	Conditions								Unit
V_{CC}	supply voltage	on pin $V_{CC(A)}$	1.2	1.2	1.5	1.8	2.5	2.5	3.3	V
		on pin $V_{CC(B)}$	1.8	5.0	1.88	1.8	2.5	5.0	3.3 to 5.0	V
C_{PD}	power dissipation capacitance	outputs enabled; $OE = V_{CC(A)}$								
		A port: (direction A to B)	5	5	5	5	5	5	5	pF
		A port: (direction B to A)	8	8	8	8	8	8	8	pF
		B port: (direction A to B)	18	18	18	18	18	18	18	pF
		B port: (direction B to A)	13	16	12	12	12	12	13	pF
		outputs disabled; $OE = GND$								
		A port: (direction A to B)	0.12	0.12	0.04	0.05	0.08	0.08	0.07	pF
		A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
B port: (direction A to B)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF		
B port: (direction B to A)	0.07	0.09	0.07	0.07	0.05	0.09	0.09	pF		

- [1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
- [2] $f_i = 10\text{ MHz}$; $V_i = GND$ to V_{CC} ; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\text{ }\Omega$.

12. Waveforms



Measurement points are given in [Table 14](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 3. Data input (A, B) to data output (B, A) propagation delay times

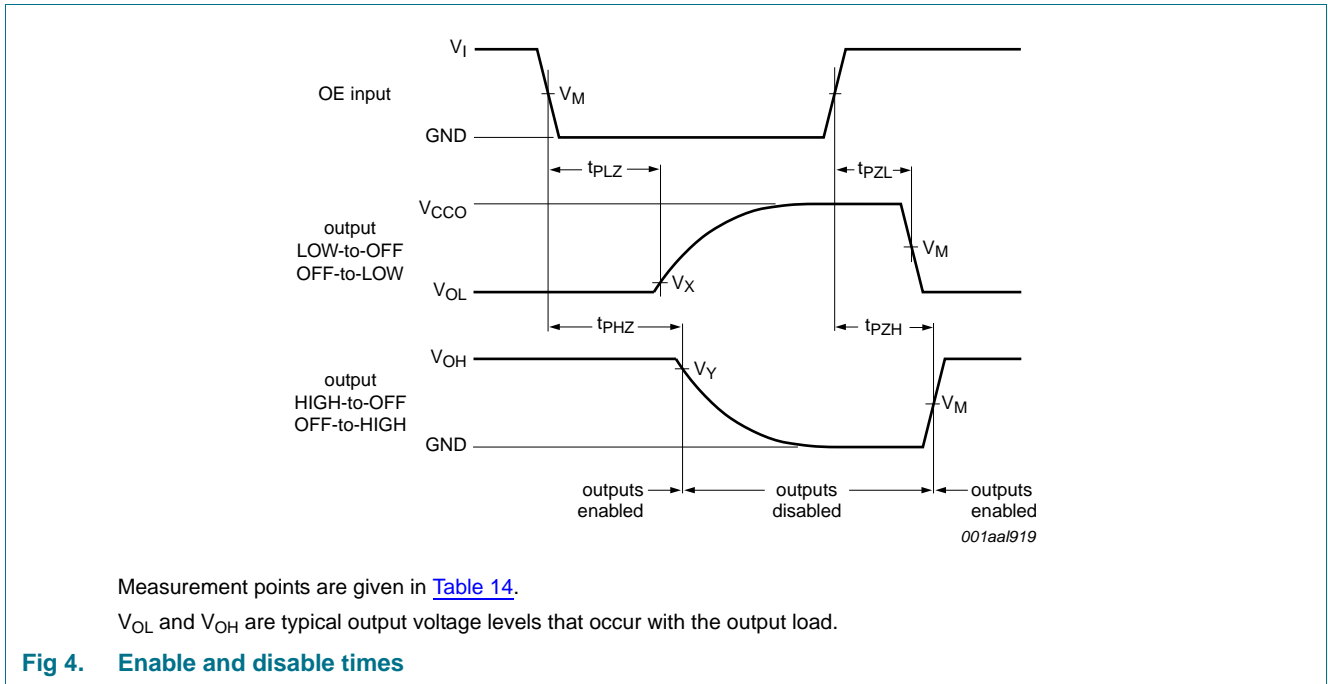


Table 14. Measurement points^[1]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
$1.5 V \pm 0.1 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1 V$	$V_{OH} - 0.1 V$
$1.8 V \pm 0.15 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
$2.5 V \pm 0.2 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
$3.3 V \pm 0.3 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$5.0 V \pm 0.5 V$	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

[1] V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

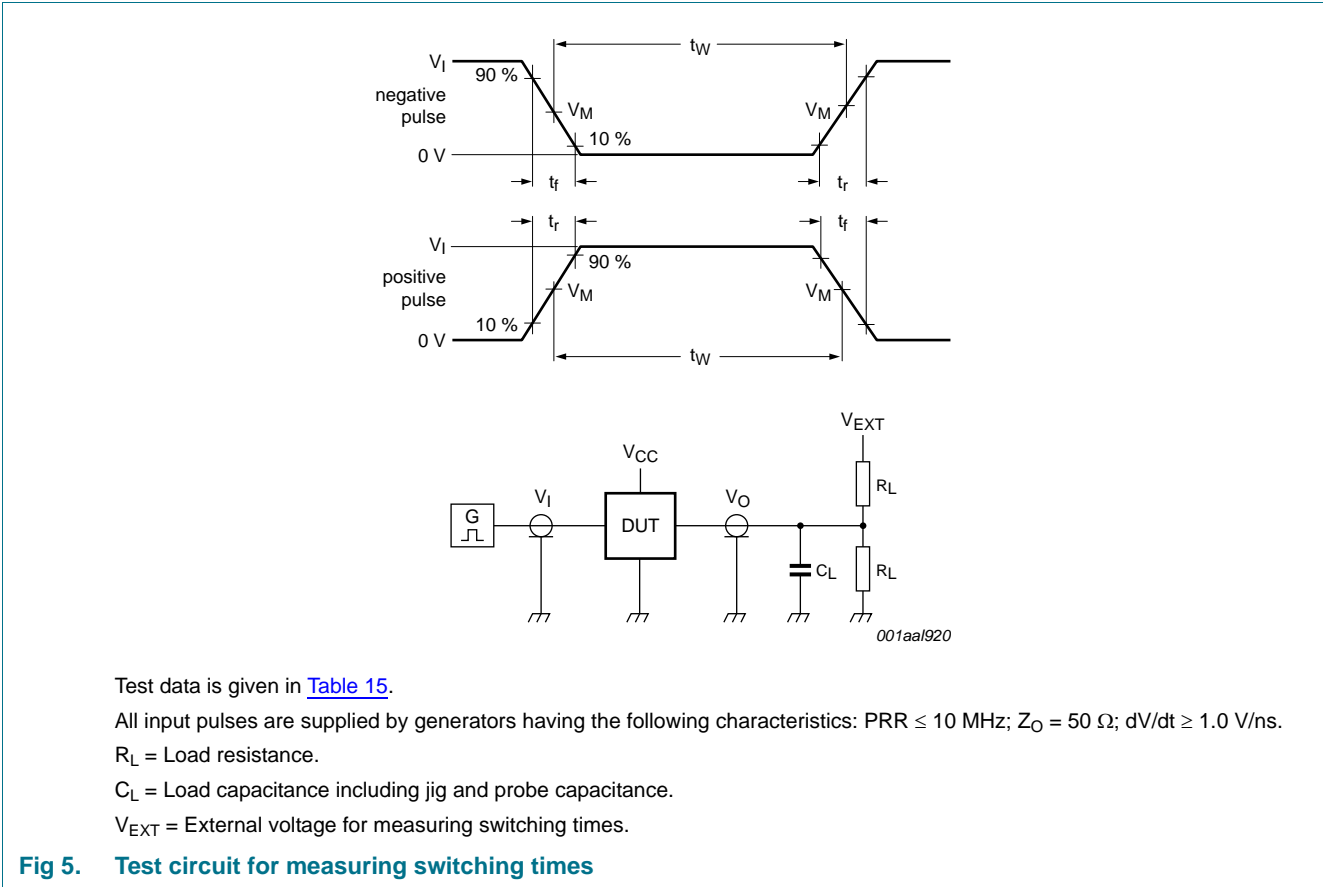


Table 15. Test data

Supply voltage		Input		Load		V _{EXT}		
V _{CC(A)}	V _{CC(B)}	V _I ^[1]	Δt/ΔV	C _L	R _L ^[2]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ} ^[3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V _{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V _{CCO}

- [1] V_{CCI} is the supply voltage associated with the input.
- [2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ. For measuring enable and disable times, R_L = 50 kΩ.
- [3] V_{CCO} is the supply voltage associated with the output.

13. Application information

13.1 Applications

Voltage level-translation applications. The NTB0101-Q100 can be used to interface between devices or systems operating at different supply voltages. See [Figure 6](#) for a typical operating circuit using the NTB0101-Q100.

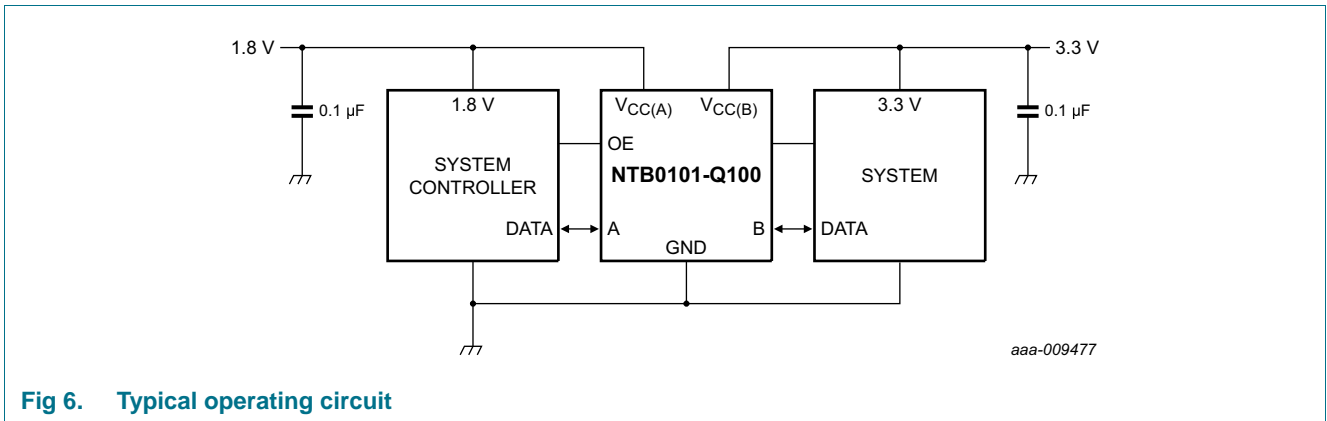


Fig 6. Typical operating circuit

13.2 Architecture

The architecture of the NTB0101-Q100 is shown in [Figure 7](#). The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the NTB0101-Q100 can maintain a defined output level. However, the output architecture is designed so that an external driver can override them when data on the bus starts flowing in the opposite direction. The output of one-shot circuits detect rising or falling edges on the A or B ports. During a rising edge, the one-shot circuits turn on the PMOS transistors (T1, T3) for a short duration, accelerating the LOW-to-HIGH transition. Similarly, during a falling edge, the one-shot circuits turn on the NMOS transistors (T2, T4) for a short duration, accelerating the HIGH-to-LOW transition. During output transitions, the typical output impedance is 70 Ω at $V_{CC0} = 1.2\text{ V}$ to 1.8 V. It is 50 Ω at $V_{CC0} = 1.8\text{ V}$ to 3.3 V and 40 Ω at $V_{CC0} = 3.3\text{ V}$ to 5.0 V.

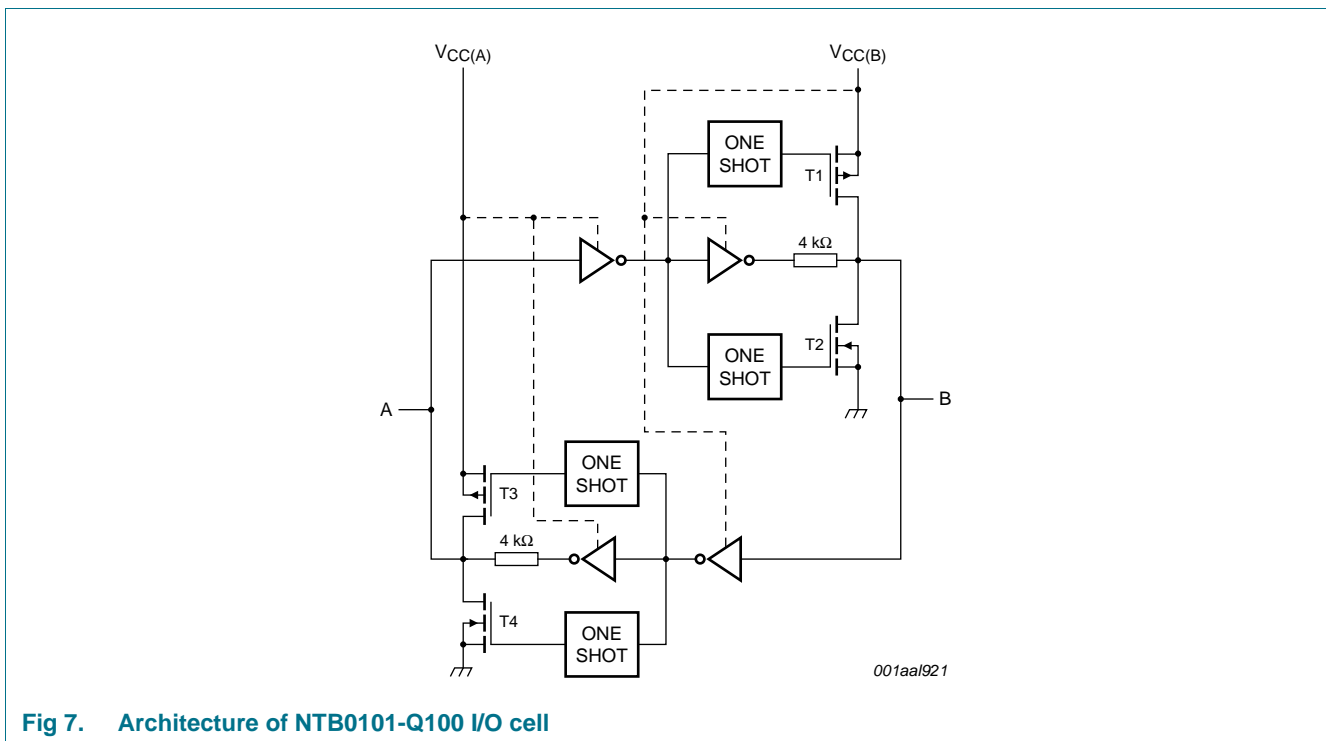
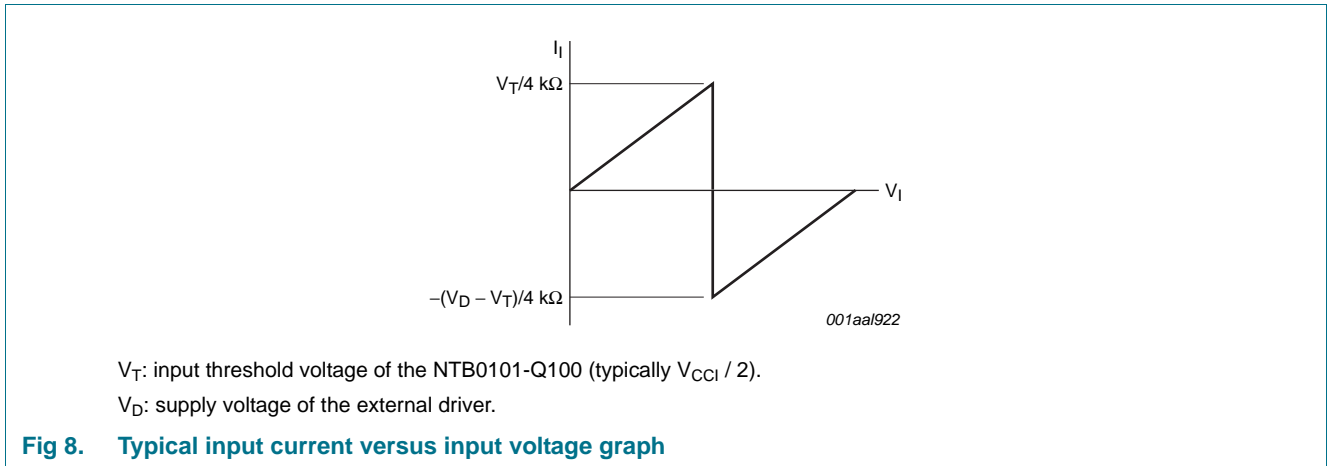


Fig 7. Architecture of NTB0101-Q100 I/O cell

13.3 Input driver requirements

For correct operation, the device driving the data I/Os of the NTB0101-Q100 must have a minimum drive capability of ± 2 mA. See [Figure 8](#) for a plot of typical input current versus input voltage.



13.4 Power-up

During operation, $V_{CC(A)}$ must never be higher than $V_{CC(B)}$. However, during power-up, $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTB0101-Q100 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

13.5 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

13.6 Pull-up or pull-down resistors on I/O lines

As mentioned previously the NTB0101-Q100 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be above 50 kΩ. For this reason, the NTB0101-Q100 is not recommended for use in open-drain driver applications such as 1-Wire or I²C-bus. For these applications, the NTS0101-Q100 level translator is recommended.

14. Package outline

Plastic surface-mounted package; 6 leads

SOT363

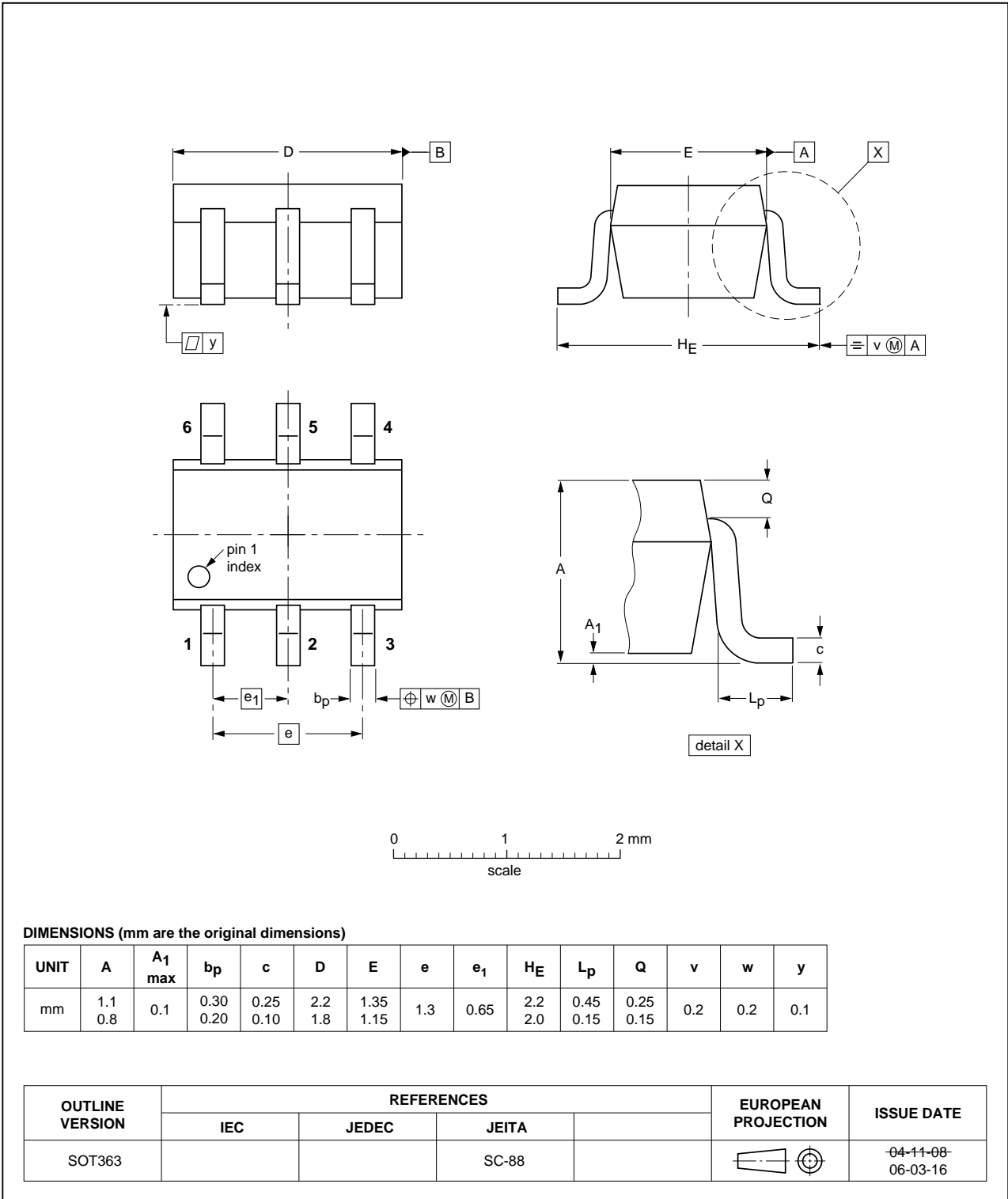


Fig 9. Package outline SOT363 (SC-88)

15. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
PRR	Pulse Repetition Rate

16. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTB0101_Q100 v.1	20140703	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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