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TDA19997HL

Smart HDMI 1.4a (4 : 1) switch with auto-adaptive equalizer

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The High-Definition Multimedia Interface (HDMI) switch enables connection of multiple DVI/HDMI inputs to a receiver with at least one input. The TDA19997HL is a switch with four HDMI 1.4a compliant DVI/HDMI inputs and one DVI/HDMI output. Each HDMI input has its own dedicated embedded EDID memory. A fifth DDC-bus input is available for VGA or second HDMI input of SoC. The built-in auto-adaptive equalizer improves signal quality, allowing the use of cable lengths up to 30 m.

The TDA19997HL supports Deep Color mode in 10-bit and 12-bit per channel up to 1920 × 1080p at 50/60 Hz. The TDA19997HL supports DVI/HDMI streams with or without High-bandwidth Digital Content Protection (HDCP 1.3) and all Data Island packets.

The TDA19997HL settings are controllable via the I2C-bus.

Features and benefits

- Complies with the HDMI 1.4a, DVI 1.0, EIA/CEA-861D and HDCP 1.3 standards
- Four independent DVI/HDMI inputs, up to 2.25 gigasamples per second
- Pin compatible with TDA9996/TDA9995
- Robust auto-adaptive equalizer (up to 20 m AWG26 at 2.25 Gbit/s)
- Robust auto-adaptive equalizer (up to 30 m AWG24 at 1.5 Gbit/s)
- Integrated 50 Ω single-ended termination resistors
- +5 V signal detection for each HDMI input
- Supports color depth processing at 24-bit, 30-bit or 36-bit per pixel
- Supports all Data Island packets
- Activity detection on each input, manages output activity and power consumption
- Extended mode: re-generate output TMDS waveform removing jitter and skew
- Frequency measurement allowing direct reading of format/resolution
- Automatic mode for main features:
 - Automatic Hot Plug Detect (HPD) generation and termination resistors management
 - Automatic HPD generation with programmable duration
 - Automatic EDID load
- Display Data Channel (DDC) bus:
 - 5 V tolerant, DDC-bus inputs with bit rates up to 400 kbit/s
 - One DDC-bus output with the same latency as the HDMI stream pipeline delay
 - DDC-bus master switch functionality avoids bus corruption
 - DDC-bus level-shifting buffer with digital lock-up protection
 - A fifth DDC-bus input available for VGA or second HDMI input of SoC
- I2C-bus controllable at bit rates up to 400 kbit/s
- Non-volatile memory for switch management (Hot Plug Detect, Power-down)
- Non-volatile storage for EDID's allowing easy loading
- Embedded Extended Display Identification Data (EDID) memory:
 - 253-byte shared and 3-byte of dedicated EDID memory per HDMI input
 - Non-volatile memory for programming default EDID content
 - Supports sources without +5 V
 - 5 embedded EDID memory supplied by +5 V from HDMI source
 - An extra 128-byte blocks for DVI or PC formats
 - EDID update by I2C-bus, example for AVR applications
- Fail-safe output in Idle mode
- Mute pin preventing from pop noise/image noise
- ATC/Rx compliant for 36-bit Deep Color 1080p 60 Hz
- ATC/Tx eye diagram compliant for 36-bit Deep color 1080p 60 Hz
- Programmable slave address for easy cascade approach
- Ready for HDMI Audio return Channel (HDMI 1.4a features refer to AN907)
- 3.3 V and 1.8 V power supplies
- Additional ESD protection pin for CEC line
- ESD protection:
 - HBM: class 2
 - MM: class B
 - FCDM: class IV
 - IEC 61000-4-2 class 3 for HDMI inputs
- Power-down mode with dedicated pin
- CMOS process
- Lead (Pb) free LQFP100 14 × 14 × 1 mm package, pitch 0.5 mm

Applications

- HDTV (plasma, Rear projection TV and LCD TV)
- YCbCr or RGB Hi-Speed video digitizer
- Projector
- Home theater
- AVR
- Switch box

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