PTN36221A

Single-channel SuperSpeed USB 3.0 redriver

Rev. 2.1 — 25 August 2015 Product data sheet

1. General description

The PTN36221A is a small, low power, high performance SuperSpeed USB 3.0 redriver that enhances signal quality by performing receive equalization on the deteriorated input signal followed by transmit de-emphasis maximizing system link performance. With its superior differential signal conditioning and enhancement capability, the device delivers significant flexibility and performance scaling for various systems with different PCB trace and cable channel conditions and still benefit from optimum power consumption. PTN36221A is a single-channel device that supports data signaling rate of 5 Gbit/s.

The PTN36221A has built-in advanced power management capability that enables significant power saving under various different USB 3.0 Low-power modes (U2/U3). The device performs these actions without host software intervention and conserves power.

The PTN36221A is powered by a 1.8 V supply. It is available in X2QFN12 1.6 mm × 1.6 mm × 0.35 mm package with 0.4 mm pitch.

2. Features and benefits

- Supports single-channel USB 3.0 redriver at 5 Gbit/s
- Compliant to SuperSpeed USB 3.0 standard
- Supports Low Frequency Periodic Signaling (LFPS) and is USB3.0 compatible
- Adjustable receive equalization, transmit de-emphasis and output swing functions
    - Selectable receive equalization to recover from InterSymbol Interference (ISI) and high-frequency losses
    - Selectable transmit de-emphasis and output swing delivers pre-compensation suited to channel conditions
    - Selectable output swing adjustment
- Integrated termination resistors provide impedance matching on both transmit and receive paths
- Automatic receiver termination detection
- Low power management scheme (When V_{DD} = 1.8 V, V_{os} = 1000 mV)
    - 97 mW active power
    - 5 mW in U2/U3 state
    - 1 mW with no connection
    - 18 μW in Deep power saving state
- Support hot plug with automatic receiver detect
- Power supply: 1.8 V ± 5 %
- ESD 8 kV HBM, 1 kV CDM for data path
- Operating temperature range: –40 °C to +85 °C

- Package offered: X2QFN12 package 1.6 mm × 1.6 mm × 0.35 mm, 0.4 mm pitch

3. Applications

- Smart phones, tablets
- Active cables
- Notebook/netbook/nettop platforms
- Docking stations
- Desktop and AIO platforms
- Server and storage platforms
- USB 3.0 peripherals such as consumer/storage devices, printers, or USB 3.0 capable hubs/repeaters

4. System context diagrams

The system context diagrams in Figure 1 illustrate PTN36221A usage.

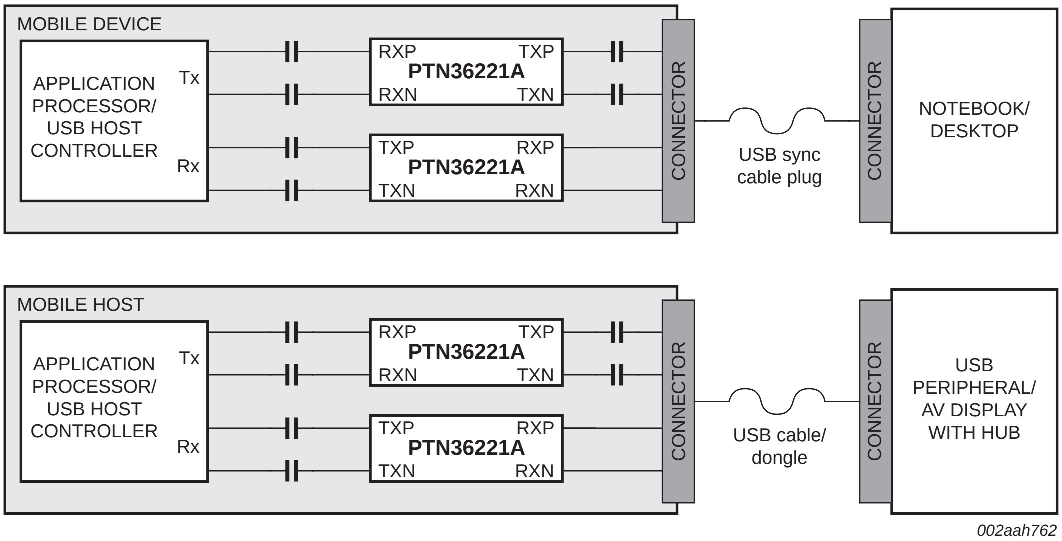


Fig 1. PTN36221A context diagrams

5. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PTN36221AHX	1A*[1]	X2QFN12	plastic, super thin quad flat package; no leads; 12 terminals; body 1.6 × 1.6 × 0.35 mm[2]	SOT1355-1

[1] Where * = week of the month.

[2] Maximum package height = 0.4 mm.

5.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN36221AHX	PTN36221AHXHP	X2QFN12	Reel 13” Q2/T3 *Standard mark SMD	10000	T_{amb} = –40 °C to +85 °C
	PTN36221AHXZ	X2QFN12	Reel 7” Q2/T3 *Standard mark	5000	T_{amb} = –40 °C to +85 °C

6. Block diagram

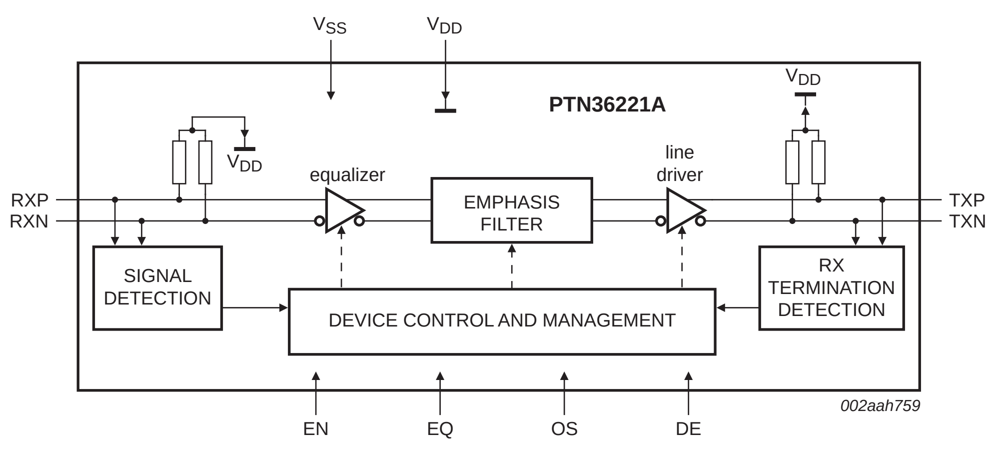
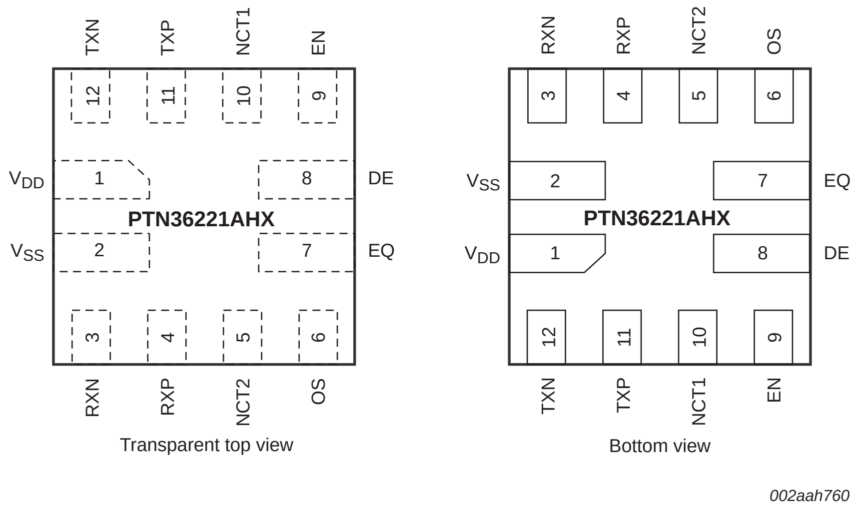


Fig 2. Block diagram of PTN36221A

7. Pinning information

7.1 Pinning



Refer to Section 12 for package-related information.

Fig 3. Pin configuration for X2QFN12

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
High-speed differential signals			
RXP	4	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. RXP makes a differential pair with RXN. The input to this pin must be AC-coupled externally.
RXN	3	self-biasing differential input	Differential signal from SuperSpeed USB 3.0 transmitter. RXN makes a differential pair with RXP. The input to this pin must be AC-coupled externally.
TXP	11	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. TXP makes a differential pair with TXN. The output of this pin must be AC-coupled externally.
TXN	12	self-biasing differential output	Differential signal to SuperSpeed USB 3.0 receiver. TXN makes a differential pair with TXP. The output of this pin must be AC-coupled externally.
Control and configuration signals			
NCT1	10	CMOS input	Test pin 1. Leave open or connect to ground for functional mode.
NCT2	5	analog input	Test pin 2. Leave open or connect to ground for functional mode.
EN	9	CMOS input	Chip enable input (active HIGH); internal 260 kΩ pull-up resistor.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
DE	8	Trinary input	Programmable output de-emphasis level setting for the output channel. [DE] = LOW: 0 dB open: −3.5 dB (default) HIGH: −6 dB
EQ	7	Trinary input	Equalizer control for the input channel. [EQ] = LOW: 3 dB open: 6 dB (default) HIGH: 9 dB
OS	6	Trinary input	Differential output swing control. [OS] = LOW: 900 mV open: 1000 mV (default) HIGH: 1100 mV
Supply voltage			
V_{DD}	1	Power	1.8 V supply.
Ground connection			
V_{SS}	2	Ground	Ground supply (0 V).

8. Functional description

Refer to Figure 2 “Block diagram of PTN36221A”.

PTN36221A is a single-channel SuperSpeed USB 3.0 redriver meant to be used for signal integrity enhancement on various platforms — smart phone, tablet, active cable, notebooks, docking station, desktop, AIO, peripheral devices, etc. With its high fidelity differential signal conditioning capability and wide configurability, this chip is flexible enough for use under a variety of system environments.

The following sections describe the individual block functions and capabilities of the device in more detail.

8.1 Receive equalization

On the high-speed signal path, the device performs receive equalization providing frequency selective gain to configuration pin EQ setting. Table 4 lists the configuration options available in this device.

Table 4. EQ configuration options

EQ	SuperSpeed USB 3.0 signal equalization gain at 2.5 GHz
LOW (0 V)	3 dB
Open	6 dB (default)
HIGH (1.8 V)	9 dB

8.2 Transmit de-emphasis

The PTN36221A device enhances High Frequency (HF) signal content further by performing de-emphasis on the high-speed signals. In addition, the device provides flat frequency gain by boosting output signal. Both flat and frequency selective gains prepare the system to cover up for losses further down the link. Table 5 lists de-emphasis configuration options of PTN36221A.

Table 5. DE configuration options

DE	SuperSpeed USB 3.0 signal de-emphasis gain
LOW (0 V)	0 dB
Open	−3.5 dB (default)
HIGH (1.8 V0	−6 dB

Figure 4 illustrates de-emphasis as a function of time.

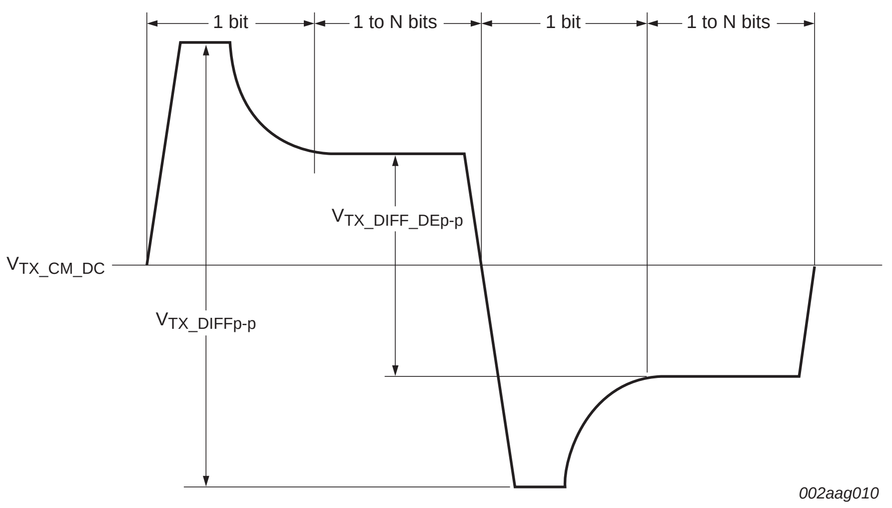


Fig 4. Differential output with de-emphasis

8.3 Device states and power management

PTN36221A has implemented an advanced power management scheme that operates in tune with USB 3.0 bus electrical condition. Though the device does not decode USB power management commands (related to USB 3.0 U1/U2/U3 transitions) exchanged between USB 3.0 host and peripheral/device, it relies on bus electrical conditions to decide to be in one of the following states:

- **Active state** wherein device is fully operational, USB data is transported. In this state, USB connection exists, but there is no need for Receive Termination detection.
- **Power-saving states**:
  - U2/U3 state
  - No connection state
- **Deep power-saving state**: When EN is LOW, this chip is in shut-down state.

The Receive Termination Detection circuitry is implemented as part of a transmitter and detect whether a load device with equivalent DC impedance Z_{RX_DC} is present.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	[1]	–0.3	+2.5	V
V_I	input voltage	[1]	–0.3	V_{DD} + 0.5	V
T_{stg}	storage temperature		–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM for high-speed pins [2]	-	8000	V
		HBM for control pins [2]	-	4000	V
		CDM for high-speed pins [3]	-	1000	V
		CDM for control pins [3]	-	500	V

[1] All voltage values (except differential voltages) are with respect to network ground terminal.

[2] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[3] Charged Device Model; JESD22-C101E December 2009 (Revision of JESD220C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

10. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	1.8 V supply option	1.71	1.8	1.89	V
V_I	input voltage	control and configuration pins (for example, EQ, DE, OS and EN)	–0.3	V_{DD}	V_{DD} + 0.3	V
T_{amb}	ambient temperature	operating in free air	–40	-	+85	°C

11. Characteristics

11.1 Device characteristics

Table 8. Device characteristics

V_{DD} = 1.8 V ± 5 %; T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup}$	start-up time	between supply voltage within operating range to specified operating characteristics (90 % of V_{DD}) until first automatic receiver termination detection	-	-	6	ms
$t_{s(HL)}$	HIGH to LOW settling time	enable to disable; power-down time; EN HIGH → LOW change to deep power-saving state; device is supplied with valid supply voltage	-	-	1	ms
$t_{s(LH)}$	LOW to HIGH settling time	disable to enable; start-up time; EN LOW → HIGH change to specified operating characteristics; device is supplied with valid supply voltage	-	-	6	ms
t_{rcfg}	reconfiguration time	any configuration pin change (from one setting to another setting) to specified operating characteristics; device is supplied with valid supply voltage	-	-	115	ms
$t_{PD(dif)}$	differential propagation delay	between 50 % level at input and output; see Figure 5	-	-	0.5	ns
t_{idle}	idle time	default wait time to wait before getting into Power-saving state	-	300	400	ms
$t_{d(pwrsave-act)}$	delay time from power-save to active	time for exiting from Power-saving state and get into Active state; see Figure 7	-	0.1	115[1]	μs
$t_{d(act-idle)}$	delay time from active to idle	reaction time for squelch detection circuit and transmitter output buffer; see Figure 6	-	9	14	ns
$t_{d(idle-act)}$	delay time from idle to active	reaction time for squelch detection circuit and transmitter output buffer; see Figure 6	-	9	14	ns
I_{DD}	supply current	Active state; Tx de-emphasis = −3.5 dB; Rx equalization gain = 6 dB; Tx output signal swing (peak-to-peak) = 1000 mV	-	57	-	mA
		U2/U3 Power-saving state	-	2.8		mA
		no USB connection state	-	0.4		mA
		Deep power-saving state; EN = LOW	-	10		μA
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC still air test environment	-	138.5	-	°C/W

[1] When special U2/U3 Power-saving mode is ON.

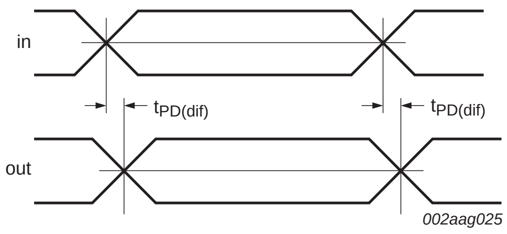


Fig 5. Propagation delay

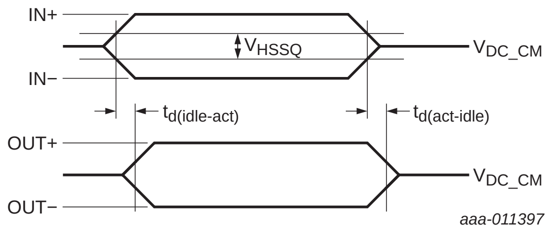


Fig 6. Electrical idle transitions in U0/U1 modes

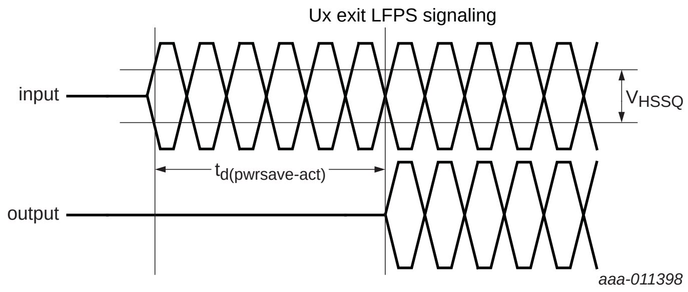


Fig 7. Power-save exit time

11.2 Receiver AC/DC characteristics

Table 9. Receiver AC/DC characteristics

V_{DD} = 1.8 V ± 5 %; T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{RX_DC}	receiver DC common-mode impedance		18	-	30	Ω
$Z_{RX\_DIFF\_DC}$	DC differential impedance	RX pair	72	-	120	Ω
Z_{IH}	HIGH-level input impedance	DC input; common-mode	25	-	-	kΩ
$V_{RX\_DIFFp-p}$	differential input peak-to-peak voltage	receiver	100	-	1200	mV
$V_{RX\_DC\_CM}$	RX DC common mode voltage		-	1.8	-	V
$V_{RX\_CM\_AC\_P}$	RX AC common-mode voltage	peak	-	-	150	mV
$V_{th(i)}$	input threshold voltage	differential peak-to-peak value	100	-	-	mV
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)	differential peak-to-peak value	-	100	-	mV

11.3 Transmitter AC/DC characteristics

Table 10. Transmitter AC/DC characteristics

V_{DD} = 1.8 V ± 5 %; T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Z_{TX_DC}	transmitter DC common-mode impedance		18	-	30	Ω
$Z_{TX\_DIFF\_DC}$	DC differential impedance	TX pair	72	-	120	Ω
$V_{TX\_DIFFp-p}$	differential peak-to-peak output voltage	R_L = 100 Ω				
		OS = open	900	1000	1100	mV
		OS = HIGH	1000	1100	1200	mV
		OS = LOW	800	900	1000	mV
$V_{TX\_DC\_CM}$	transmitter DC common-mode voltage		-	1.3	V_{DD}	V
$V_{TX\_CM\_ACpp\_ACTIV}$	TX AC common-mode peak-to-peak output voltage (active state)	device input fed with differential signal	-	-	100	mV
$V_{TX\_IDL\_DIFF\_ACpp}$	electrical idle differential peak-to-peak output voltage	when link is in electrical idle	-	-	10	mV
$V_{TX\_RCV\_DETECT}$	voltage change allowed during receiver detection	positive voltage swing to sense the receiver termination detection	-	-	600	mV
$t_{r(tx)}$	transmit rise time	measured using 20 % and 80 % levels; see Figure 8	40	55	75	ps
$t_{f(tx)}$	transmit fall time	measured using 80 % and 20 % levels; see Figure 8	40	55	75	ps
$t_{(r-f)tx}$	difference between transmit rise and fall time	measured using 20 % and 80 % levels	-	-	15	ps

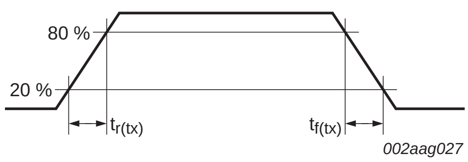


Fig 8. Output rise and fall times

11.4 Jitter performance

Table 11 provides jitter performance of PTN36221A under a specific set of conditions that is illustrated by Figure 9.

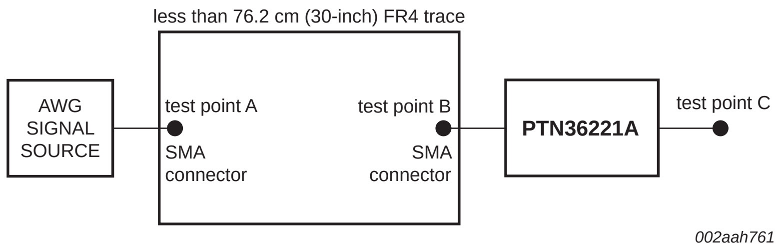
Table 11. Jitter performance characteristics

Unit Interval (UI) = 200 ps.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{jit(o)(p-p)}$	peak-to-peak output jitter time	total jitter at test point C [1]	-	0.19	-	UI
$t_{jit(dtrm)(p-p)}$	peak-to-peak deterministic jitter time	[1]	-	0.11	-	UI
$t_{jit(rndm)(p-p)}$	peak-to-peak random jitter time	[1][2]	-	0.08	-	UI

[1] Measured at test point C with K28.5 pattern, V_{ID} = 1000 mV (peak-to-peak), 5 Gbit/s; −3.5 dB de-emphasis from source.

[2] Random jitter calculated as 14.069 times the RMS random jitter for 10^{-12} bit error rate.



Source jitter measurements:

total peak-to-peak jitter = 21 ps

peak-to-peak deterministic jitter = 8 ps

random jitter = 0.95 ps (RMS value)

Fig 9. Jitter measurement setup

11.5 Control inputs

Table 12. Control input characteristics for EN pin

V_{DD} = 1.8 V ± 5 %; T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.35 \times V_{DD}$	V
I_{LI}	input leakage current	measured with input at $V_{IH(max)}$ and $V_{IL(min)}$	-	7	20	μA
$R_{pu(int)}$	internal pull-up resistance		-	230	-	kΩ

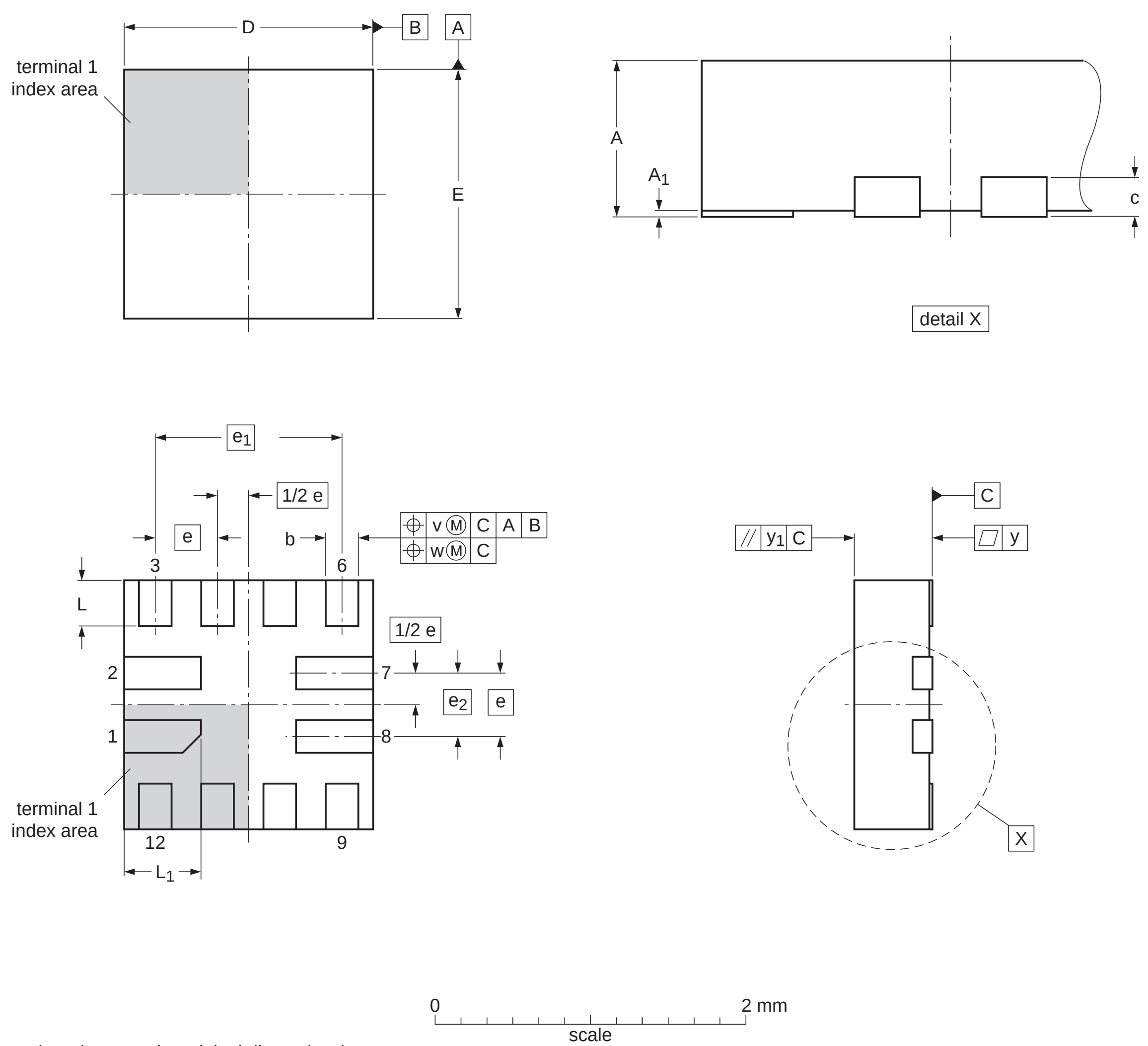
Table 13. Trinary control input characteristics for DE, EQ, and OS pins

V_{DD} = 1.8 V ± 5 %; T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.75 × V_{DD}	V_{DD}	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	0	0.25 × V_{DD}	V
I_{IH}	HIGH-level input current		-	-	45	μA
I_{IL}	LOW-level input current		−45	-	-	μA
$Z_{ext(open)}$	external impedance	for detection of open condition	250	-	-	kΩ
I_L	leakage current	of external GPIO; for detection of open condition	−6	-	+6	μA
C_L	load capacitance	for reliable detection of open condition	-	-	35	pF
I_{LI}	input leakage current	EN = LOW; measured with input at $V_{IH(max)}$ and $V_{IL(min)}$	-	-	1	μA
$R_{pu(int)}$	internal pull-up resistance	for detection of trinary setting	-	50	-	kΩ
$R_{pd(int)}$	internal pull-down resistance	for detection of trinary setting	-	50	-	kΩ

12. Package outline

X2QFN12: plastic, super thin quad flat package; no leads; 12 terminals; body 1.6 x 1.6 x 0.35 mm **SOT1355-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	c	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.40	0.05	0.25		1.65	1.65				0.4	0.6				
	nom	0.35		0.20	0.127	1.60	1.60	0.4	1.2	0.4	0.3	0.5	0.07	0.05	0.05	0.05
	min	0.30	0.00	0.15		1.55	1.55				0.2	0.4				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1355-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1355-1	- - -	MO-255	- - -			~~13-12-23~~ 14-01-13

Fig 10. Package outline SOT1355-1 (X2QFN12)

13. Packing information

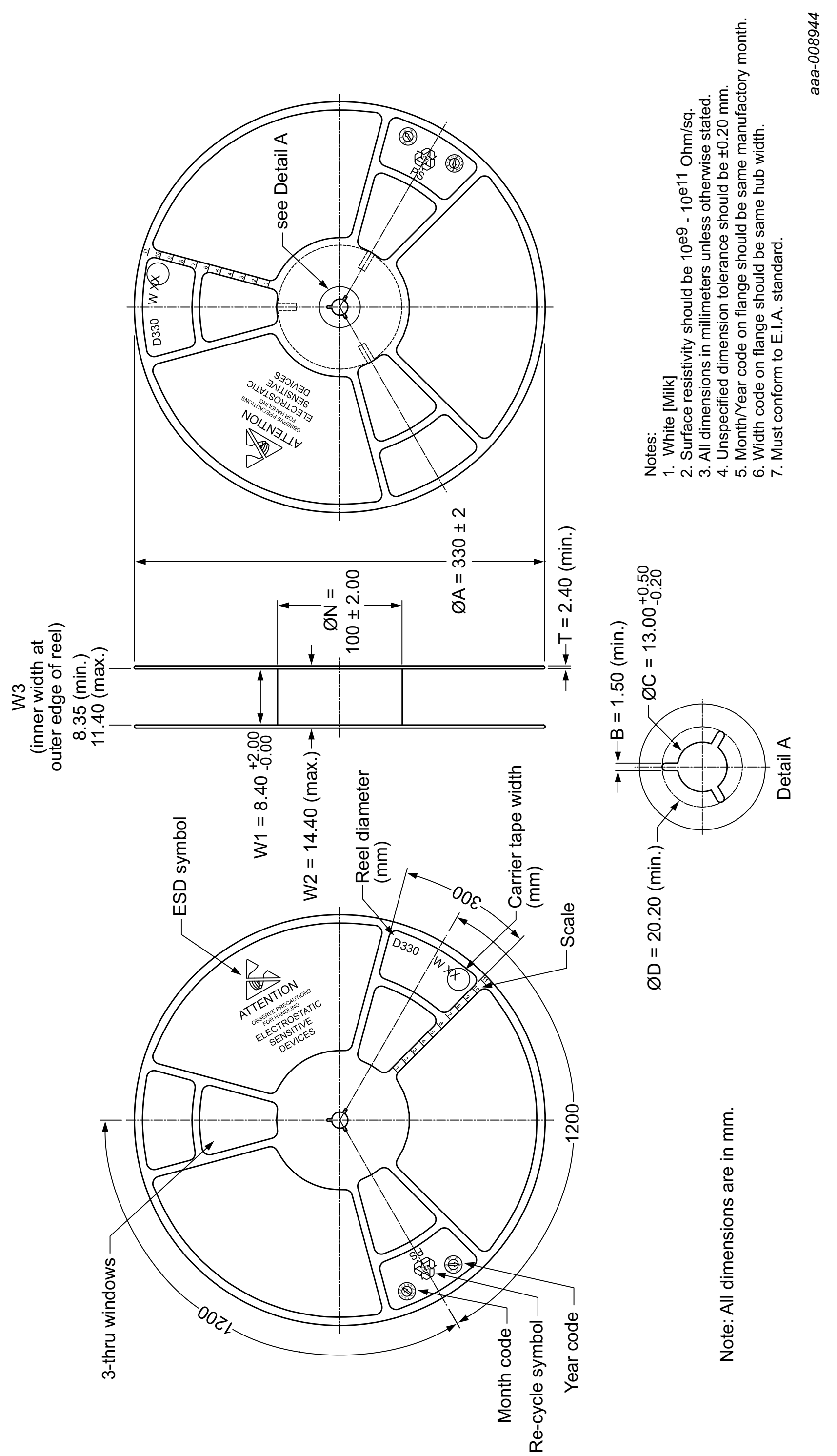
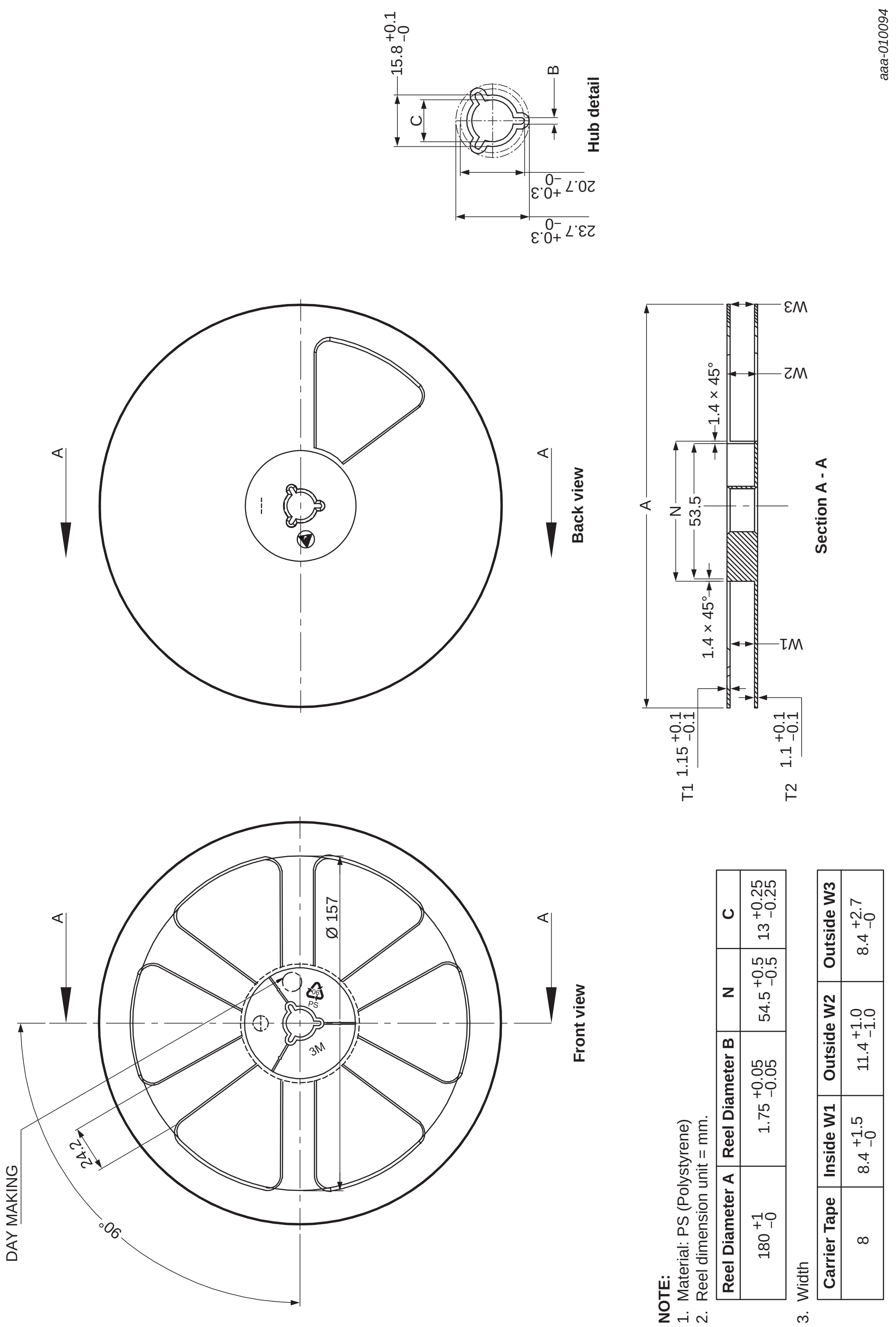


Fig 11. 13” reel dimensions (13-inch diameter; 4-inch hub; 8 mm carrier tape)



NOTE:

1. Material: PS (Polystyrene)
2. Reel dimension unit = mm.

Reel Diameter A	Reel Diameter B	N	C
180 +1 −0	1.75 +0.05 −0.05	54.5 +0.5 −0.5	13 +0.25 −0.25

3. Width

Carrier Tape	Inside W1	Outside W2	Outside W3
8	8.4 +1.5 −0	11.4 +1.0 −1.0	8.4 +2.7 −0

Fig 12. 7” reel dimensions (7-inch diameter; 2-inch hub; 8 mm carrier tape)

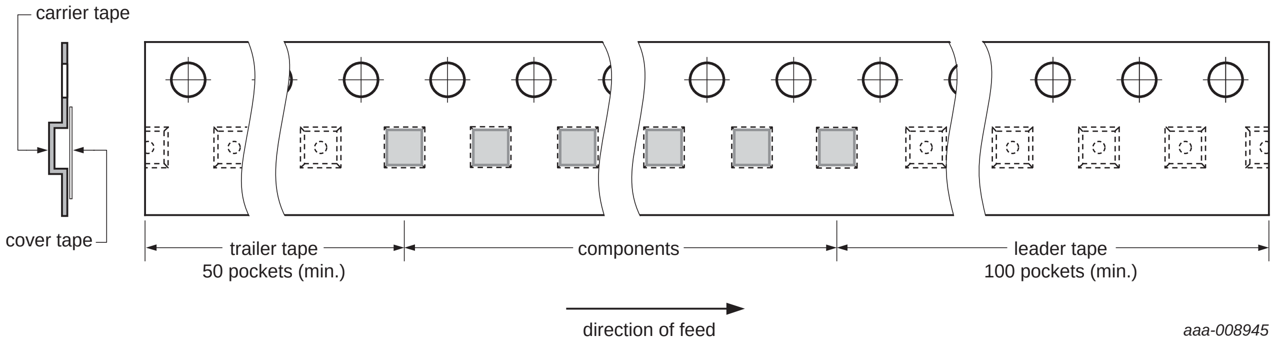


Fig 13. Tape leader and trailer configuration

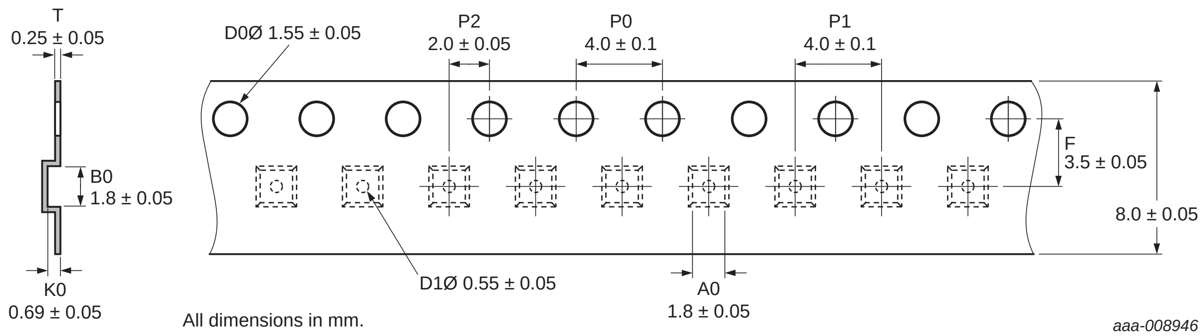


Fig 14. Carrier tape

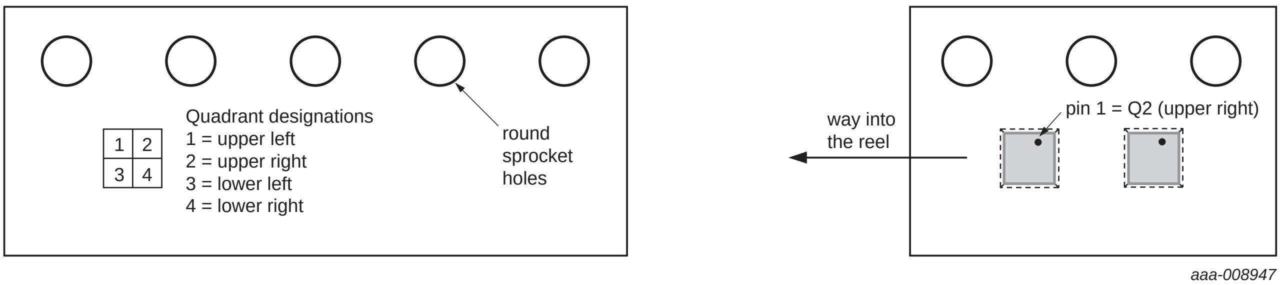


Fig 15. Pin 1 orientation

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020D)

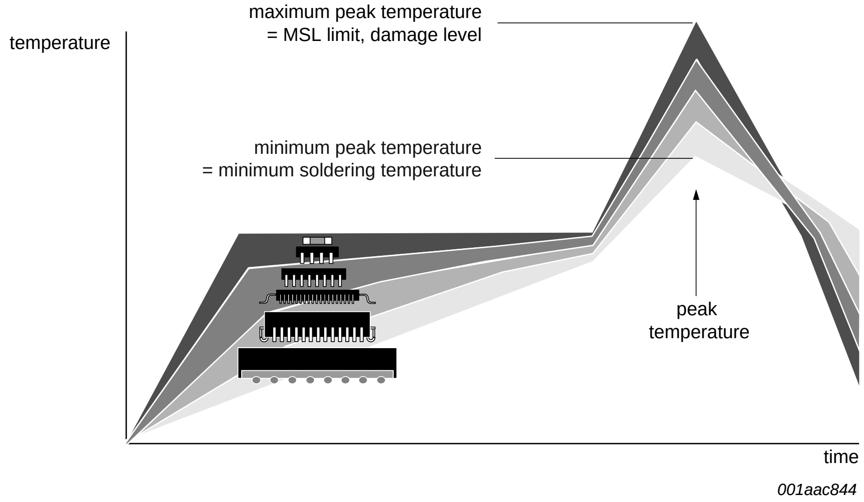
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Soldering: PCB footprints

Footprint information for reflow soldering of X2QFN12 package

SOT1355-1

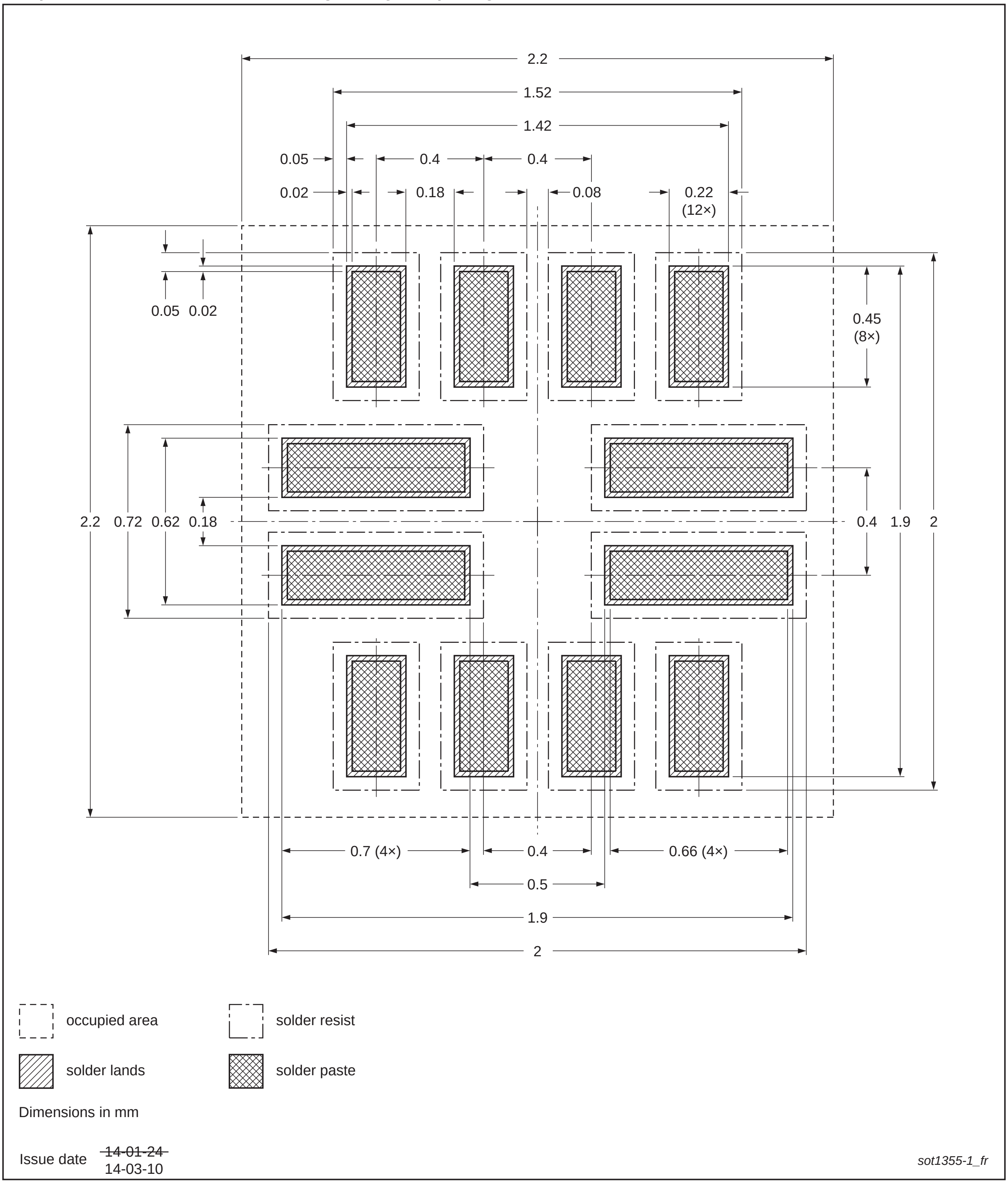


Fig 17. PCB footprint for SOT1355-1 (X2QFN12); reflow soldering

16. Abbreviations

Table 16. Abbreviations

Acronym	Description
AIO	All In One computer platform
CDM	Charged-Device Model
HBM	Human Body Model
IC	Integrated Circuit
LFPS	Low Frequency Periodic Sampling
PCB	Printed-Circuit Board
Rx	Receive
SI	Signal Integrity
Tx	Transmit
UI	Unit Interval
USB	Universal Serial Bus

17. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN36221A v.2.1	20150825	Product data sheet	-	PTN36221A v.2
Modifications:	• Table 13 “Trinary control input characteristics for DE, EQ, and OS pins”: Added V_{IH}, V_{IL}, I_{IH}, I_{IL}, $Z_{ext(open)}$, I_I, and C_L.			
PTN36221A v.2	20140909	Product data sheet	-	PTN36221A v.1
Modifications:	• Added Section 15 “Soldering: PCB footprints”			
PTN36221A v.1	20140120	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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