AN11516

TFF1024 EVB and application recommendations

Rev. 1 — 20 June 2014 Application note

Document information

Info	Content
Keywords	VSAT, Ku band, L-band, Down-Converter, LNB, Satellite communication
Abstract	Application note in which the customer evaluation board is described and recommendations are listed for the use of the NXP TFF1024 DCV IC.

Revision history

Rev	Date	Description
1	20140620	First publication

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1. Introduction

1.1 TFF1024, functional description

The TFF1024HN is an integrated, single-in/single out, down-converter for use in Low Noise Block (LNB) convertors in a 10.70 GHz to 12.75 GHz Ku band satellite receiver system.

1.2 Features and benefits

- Low current consumption integrated pre-amplifier, mixer, buffer amplifier and PLL synthesizer
- Flat gain over frequency
- Single 5 V supply pin
- Low cost 25 MHz crystal
- Crystal controlled LO frequency generation
- Switched LO frequency (selectable to 9.75 GHz, 10.00 GHz, 10.25 GHz, 10.55 GHz,10.60 GHz, 10.75 GHz, 11.25 GHz or 11.30 GHz) with a 25 MHz crystal as reference
- Other LO frequencies within the 9.75 GHz to 11.30 GHz range can be realized by using an alternative reference frequency
- Low phase noise
- Low spurious
- Low external component count
- Alignment-free concept
- ESD protection on all pins

1.3 Applications

- Ku band LNB converters for VSAT and digital satellite reception (DVB-S / DVB-S2)

1.4 Content for this document

A description of the Evaluation board, the usage and settings are given. Also some examples of measurement set-ups and measurement results are shown.

Concerning LNB design and PCB layout recommendations are given as well as some tricks to avoid loss in performance.

2. The customer Evaluation Board for TFF1024

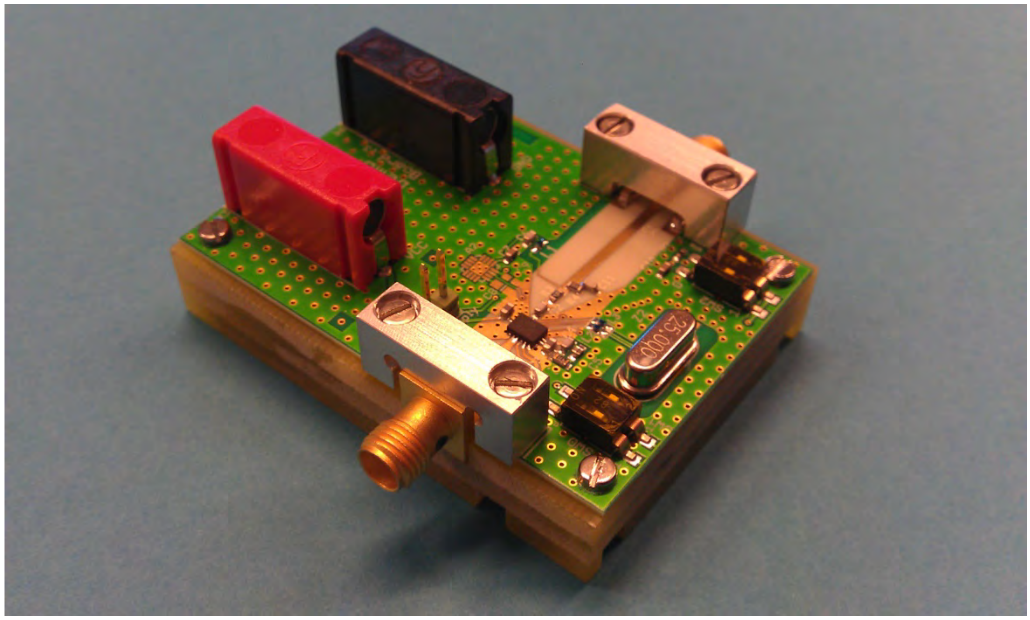


Fig 1. OM7985, TFF1024, demo-board

2.1 Target specifications for the demonstrator

2.1.1 Functional description:

- The demonstrator should down-convert blocks of signals from Ku band (10.7GHz – 12.75GHz) to L-band (950MHz – 2150MHz)
- The demonstrator supply could be external or via the IF output by an integrated bias-Tee
- LO frequency selection is implemented by DIP switches
- The demonstrators in- and output signals will be single ended (SMA connector)

2.1.2 Key specifications:

- LO frequencies: 9.750, 10.000, 10.250, 10.550, 10.600, 10.750, 11.250, 11.300GHz selectable by three logic inputs
- Input frequency range 10.70GHz – 12.85GHz
- Typical RF input levels: -85dBm….-40dBm per carrier
- Typical IF output levels: -10dBm …-55dBm per carrier
- Supply voltage typical 5.0V, when supplied via banana sockets, 12V to 18V when supplied via IF
- Supply current: 54mA typ.
- For other specification please refer to the product datasheet

2.1.3 Mechanical requirements

- used material Rogers 4233, 2o mil (0.5mm) thickness
- PCB layer stack: double side copper, bottom layer used as RF GND layer
- Applied RF connectors: SMA type

2.2 EVB schematic

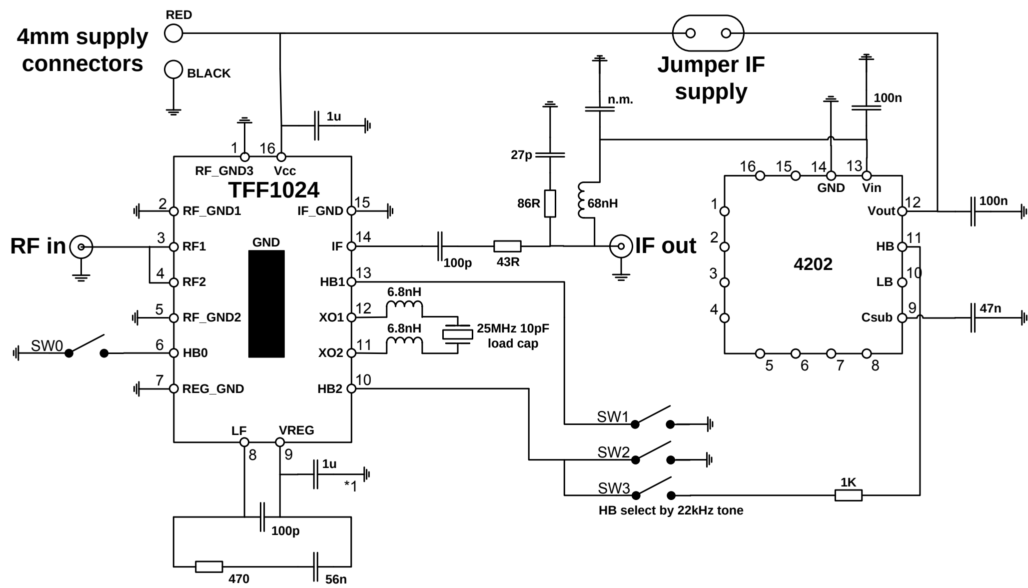


Fig 2. Schematic of NXP OM7985 EVB

2.3 Connecting the demonstrator

Basically three connections are required, the Power Supply Unit (PSU), RF input signal and IF output signal.

2.3.1 Required equipment

- Power Supply Unit (PSU), 5 Volts, min. 300mA (peak current during start-up), 55mA average consumption during normal operation
- Spectrum Analyzer, SA, (up to 14 GHz)
- A signal generator (up to min. 12.85 GHz)
- A Noise Gain analyzer

2.3.2 Demonstrator connected using direct supply

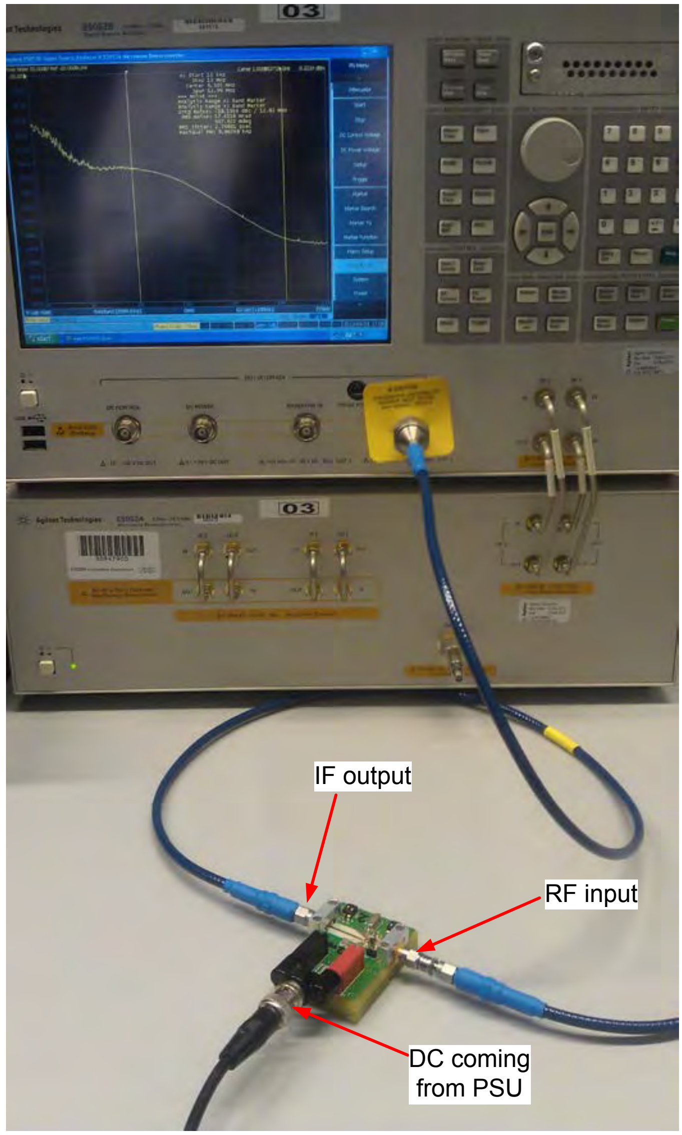


Fig 3. EVB in measurement set-up, directly fed

Remarks:

- PSU has to be 5.0Volts
- RF input can be connected to noise source, network analyzer or signal generator depending on required analyzed parameter
- To enable easy measurement interfacing the IF output is implemented by a 50 Ohms SMA connector although the TFF1024 output impedance is typical 75 Ohms.

2.3.3 Demonstrator connected using IF supply

The EVB is routed to be used with an external bias/regulator device. For this the Zetex ZXNB4202 device can be used. It has an integrated 5 Volts regulator and can bias the GaAs LNA stages.

The bias Tee implemented on the EVB uses an SMD inductor and decoupling capacitor to ground. It should create a high impedance, referred to 75 Ohms, in the IF frequency range.

In case the external bias mode has to be used the ZXNB4202 has to be mounted and the external bias jumper needs to be placed.

2.4 Jumper / DIP switch settings

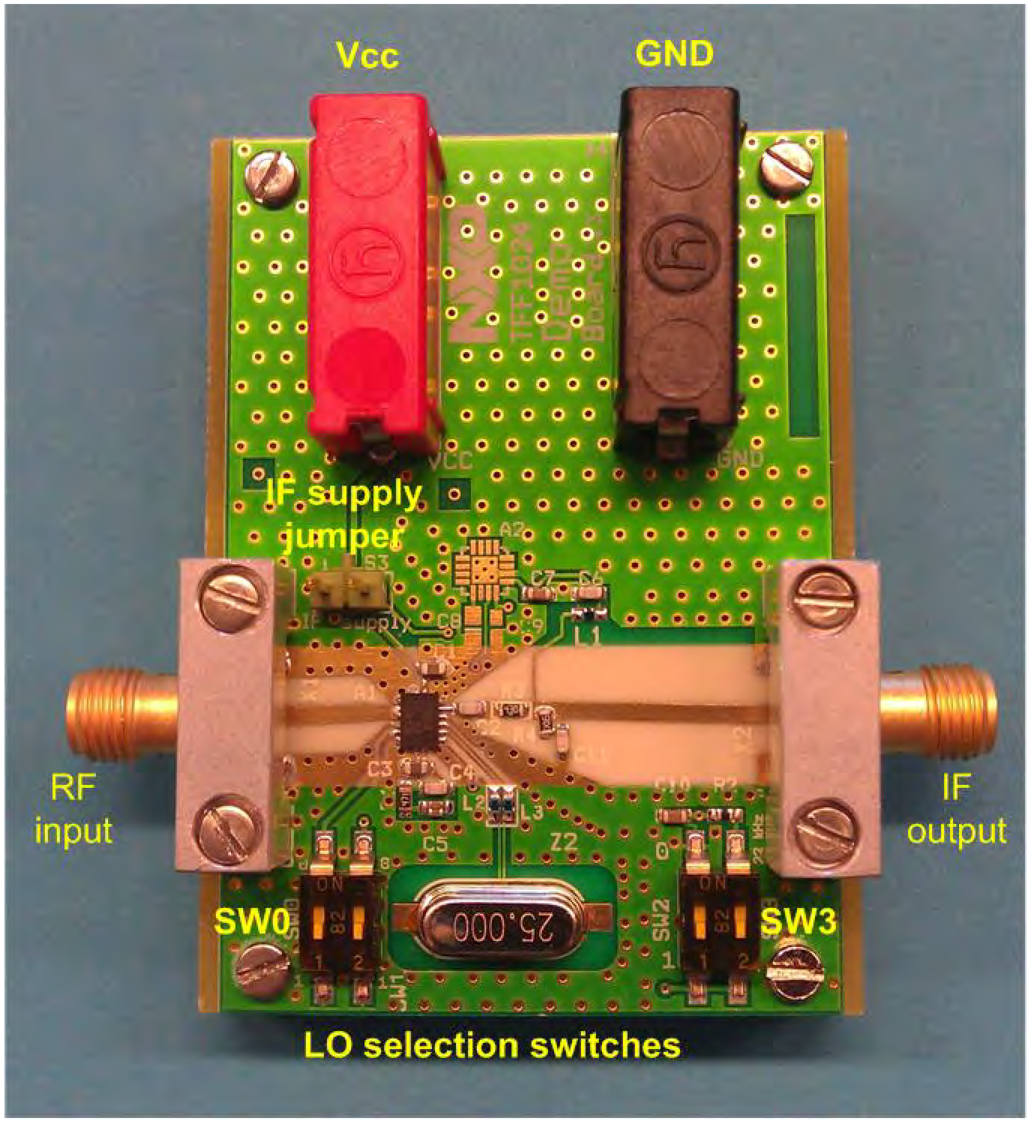


Fig 4. TFF1024 demo-board switches

Remarks

- SW0 – SW2 (all in 0 position = 9.75GHz LO), SW3 = not connected
- After changing the LO frequency a "power on reset" has to be generated to enable the optimum sub-band selection for the VCO.

Table 1. LO Frequency selection table

Please refer to the product datasheet for logic levels)

Flo [GHz]	HB2 (pin 10)	HB1 (pin 13)	HB0 (pin 6)
9.75	0	0	0
10.00	0	0	1
10.25	0	1	0
10.55	0	1	1
10.60	1	0	0
10.75	1	0	1
11.25	1	1	0
11.30	1	1	1

2.4.1 Applied Connectors

Table 2. Description of applied connectors

Table description (optional)

Component Identifier	Connector Type	Function
X1	SMA launcher	RF input
X2	SMA launcher	IF output / DC feed
X3	4mm banana connector	Connection of Vcc
X4	4mm banana connector	Connection for GND

3. TFF1024 functional blocks description

In following sections the various parts of the circuit that may be used as DCV part for a LNB design are described. If necessary the configuration, choice of components and recommendations to avoid performance degradation are described.

3.1 The RF input signal path

The RF input uses two pins, 3 and 4, on the TFF1024. This is done in order to have optimum matching with 50Ω transmission lines implemented on 0.5mm PCB material. Make sure the ground that is associated with this input micro-strip is grounded properly at the two adjacent ground pins 2 and 5. As a DC blocking capacitor is integrated the input TL may contain a DC component.

3.2 The IF output signal path

The IF output of the TFF1024 is available at pin 14, it is DC biased hence a decoupling capacitor is required. Be sure to use a capacitor that has low impedance and low ESR in the 950 MHz – 2150 MHz frequency range. Please note that the nominal output impedance at IF is 75Ω, to simplify connection to most measurement equipment for the EVB a conversion to 50Ω was chosen.

3.3 The PLL loop-filter

The loop-filter components applied are tuned for optimum RMS PJ, the loop bandwidth is approximately 150 kHz.

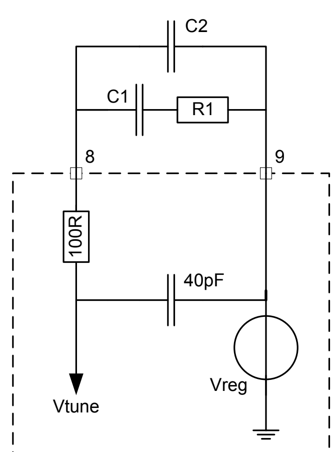


Fig 5. TFF1024 PLL loop filter

Table 3. Default PLL loop filter component values

Comp Identifier	Value
C1	56nF
C2	100pF
R1	470Ω

3.4 The XO tank circuit

The reference for the PLL is implemented by an integrated crystal oscillator (XO). The crystal has to be connected to pins 11 and 12 of the TFF1024. The load capacitance provided by the TFF1024 itself is approximately 7pF. We recommend using a crystal with 8pF load capacitance. In case a crystal with higher load capacitance has to be used the LO frequency will become too high and may be tuned down by applying additional load capacitance. In that case we recommend two capacitors to GND (one from each XO pin); however applying capacitors with a value larger than a few pF might cause XO start up problems at extreme conditions.
For optimizing the so called NXO spurious performance we recommend to use a SMD inductor (6.8nH) in series with each XO line, see also section 4.1.

3.5 The Divider Ratio setting inputs

The LO selection is implemented by 3 logic inputs. The possible configurations are shown in table 1. The TFF1024 can be used in static mode (HB0 till HB2 pins hardwired) or in dynamic mode. In dynamic mode it is possible to modify the LO frequency during operation, after changing the LO a new VCO sub-band calibration will be initiated.

This is done by applying a particular sequence in modifying the values of pins HB0, HB1 and HB2. Starting from initial value of HB0 HB1 HB2, the following sequence must be applied:

1) Unset HB0 value by applying 0
2) Unset HB1 value by applying 0
3) Set HB1 value (can remain 0)
4) Set HB0 value (can remain 0)
5) Trigger one or two changes on HB2 pin to set HB2 value
    - Apply sequence low-high-low if initial state was low and new state is low
    - Apply sequence high-low-high if initial state was high and new state is high
    - Apply sequence high-low if initial state was high and new state is low
    - Apply sequence low-high if initial state was low and new state is high

As soon as a movement is applied on HB2, automatic selection of VCO sub-band is triggered and calibration phase ends once PLL is locked again.

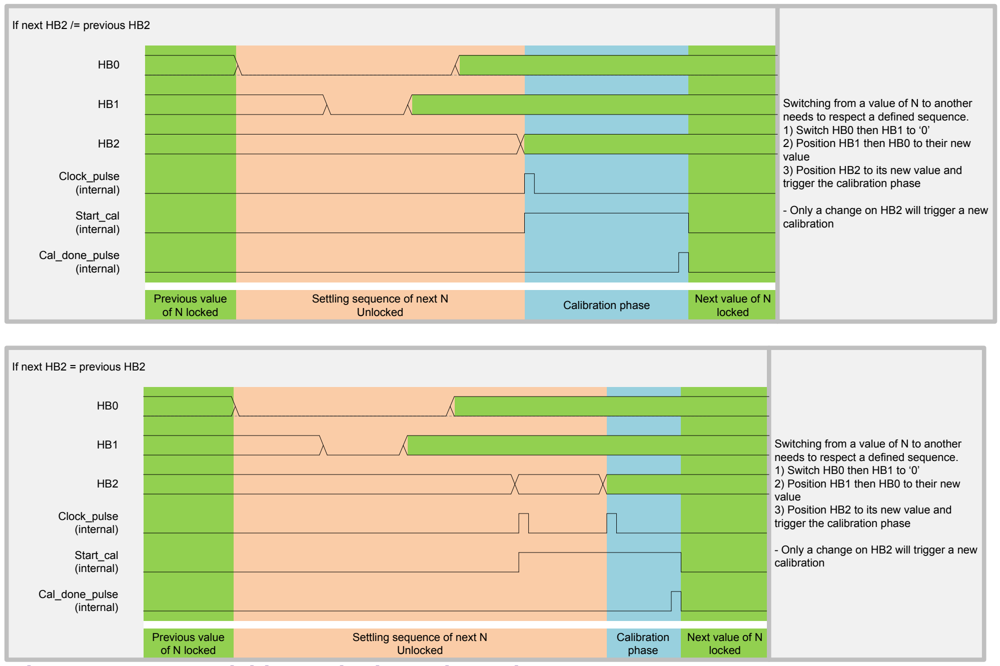


Fig 6. TFF1024 Divider Ratio dynamic setting

The next figures show examples of sequences to apply on HB0 to HB2 pins

	initial value	final value	sequence to apply on HB pins (nextHB2 /= previous HB2)								
HB0	0	1	0	0	0	0	1	1	1	1	1
HB1	0	1	0	0	0	1	1	1	1	1	1
HB2	0	1	0	0	0	0	0	1	1	1	1

	initial value	final value	sequence to apply on HB pins (nextHB2 /= previous HB2)								
HB0	0	0	0	0	0	0	0	0	0	0	0
HB1	0	0	0	0	0	0	0	0	0	0	0
HB2	0	1	0	0	0	0	0	1	1	1	1

	initial value	final value	sequence to apply on HB pins (nextHB2 /= previous HB2)								
HB0	1	1	1	0	0	0	1	1	1	1	1
HB1	0	0	0	0	0	0	0	0	0	0	0
HB2	0	1	0	0	0	0	0	1	1	1	1

	initial value	final value	sequence to apply on HB pins (nextHB2 = previous HB2)								
HB0	0	1	0	0	0	0	1	1	1	1	1
HB1	0	0	0	0	0	0	0	0	0	0	0
HB2	0	0	0	0	0	0	0	1	0	0	0

	initial value	final value	sequence to apply on HB pins (nextHB2 = previous HB2)								
HB0	1	0	1	0	0	0	0	0	0	0	0
HB1	1	0	1	1	0	0	0	0	0	0	0
HB2	1	1	1	1	1	1	1	0	1	1	1

Green : Valid data

Orange : Sequence data

Blue : Triggering calibration

Total sequence time do not exceed a few us, depending on master speed.

Total sequence time to be compared to the time required for powering off/on the chip.

Fig 7. TFF1024 Divider Ratio dynamic setting examples

	initial value		final value	sequence to apply on HB pins						
HB0	0		1	0		0		1		1
HB1	0	⇨	1	0	⇨	1	⇨	1	⇨	1
HB2	0		1	0		0		0		1

	initial value		final value	sequence to apply on HB pins		
HB0	0		0	0		0
HB1	0	⇨	0	0	⇨	0
HB2	0		1	0		1

	initial value		final value	sequence to apply on HB pins		
HB0	1		1	1		1
HB1	0	⇨	0	0	⇨	0
HB2	0		1	0		1

	initial value		final value	sequence to apply on HB pins						
HB0	0		1	0		1		1		1
HB1	0	⇨	0	0	⇨	0	⇨	0	⇨	0
HB2	0		0	0		0		1		0

	initial value		final value	sequence to apply on HB pins								
HB0	1		0	1		0		0		0		0
HB1	1	⇨	0	1	⇨	1	⇨	0	⇨	0	⇨	0
HB2	1		1	1		1		1		0		1

It is possible to reduce the number of steps of the full sequence in some particular cases:

- when HB0 or HB1 do not change
- when they were initially 0, or when they will be finally 0

Fig 8. TFF1024 Divider Ratio dynamic setting optimized examples

3.5.1 Remark on the HB-pins PCB routing

If long tracks to the HB pins are used it is recommended to put some decoupling capacitors on those tracks to GND to avoid parasitic coupling of RF signals (inside the TFF1024 there are small value decoupling capacitors to suppress energy in the microwave frequency range.

4. Application recommendations / hints

4.1 Improvement on NXO spurious

For each frequency down-converter with integrated PLL a spurious in the IF can be expected in case the IF frequency is close to a multiple of the reference frequency applied by the PLL. This is caused by an amount of energy in the IF (at integer multiple of the XO frequency) that radiates back into the PLL reference.

The reference signal for the PLL in the time domain can be considered as a 25 MHz CW sine wave with a multiple of this reference superposed on it (induced by the IF) as shown in the figure below.

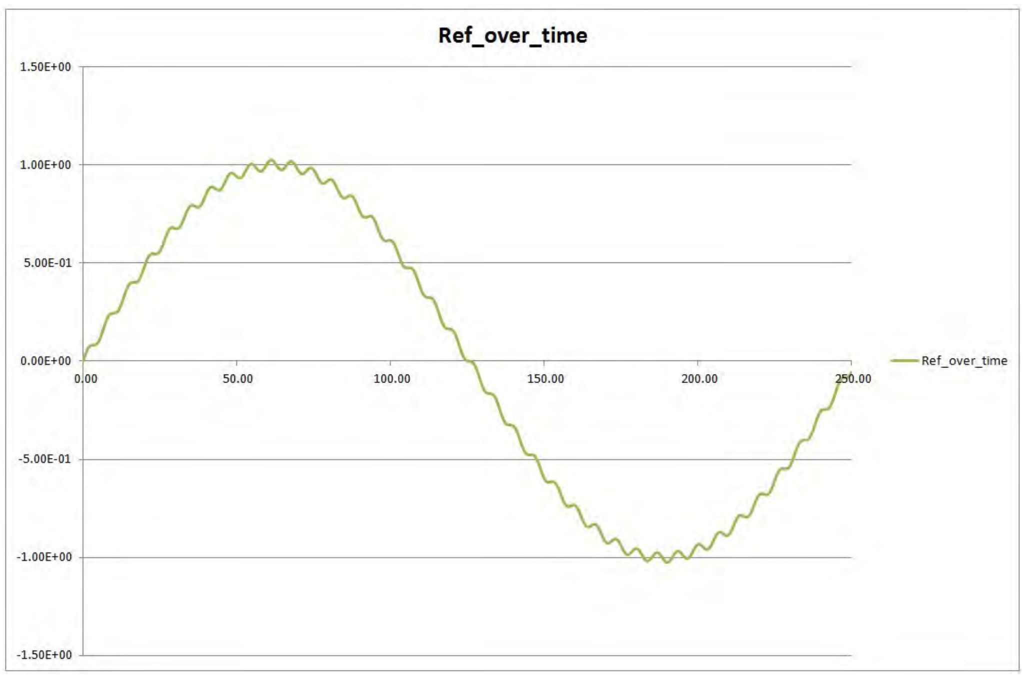


Fig 9. PLL reference signal with 950MHz CW IF supper-posed

In this figure we see the reference in the time domain (sine wave as Vxo2-xo1) at 25MHz with a 950 MHz sine wave with 2.5% amplitude, compared to 25 MHz, on top.

If we zoom in at the zero crossings, of which the timing can induce current pulses for the charge pumps, we see that some uncertainty occurs due to the presence of the N times XO component.

To minimize the NXO ripple on the reference we should:
A) keep the amount of cross-talk as small as possible;
B) modify the circuit such to get a high impedance at the Reference inputs for frequencies significantly higher than the reference;
C) optimize the balance in the Reference inputs.

Example:

assume the LO is running at 10.25 MHz, the XO exactly at 25.000 MHz and the RF input frequency is at 11.200 GHz. Then the IF will be at 11.20 – 10.25 = 0.950 GHz. This is exactly at 38 times the XO, in case we feed the TFF1024 with a CW signal at 11.2000 GHz in the IF spectrum we will observe a CW signal at 950 MHz. If we shift the RF frequency by a small amount (i.e. 10 kHz) we will see three frequency components in the IF spectrum (assuming the RF power is sufficiently strong). These three frequencies are 950.000 MHz, 950.010 MHz and 950.020 MHz. See figure below as example.

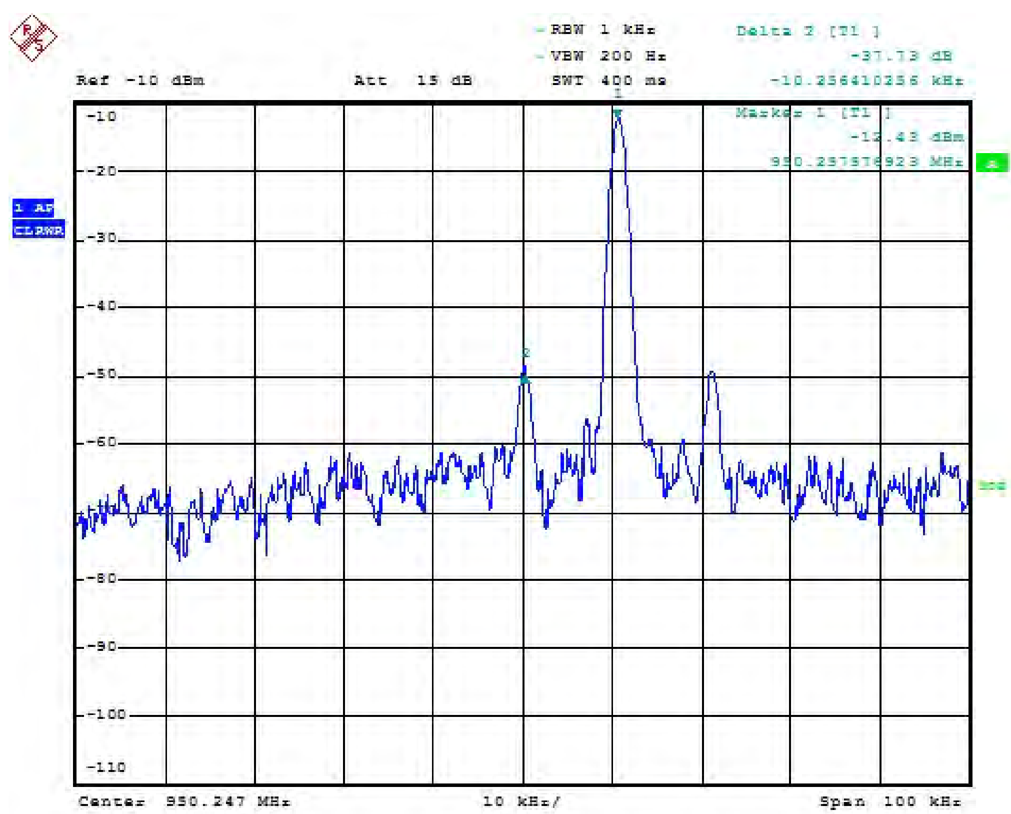


Fig 10. Example for NXO spurious

Figure 11 shows the NXO spurious, in this case the RF signal frequency is adjusted to have the IF at approximately 10 kHz offset from the 38th XO harmonic.

In case the RF signal is switched off we get following IF spectrum:

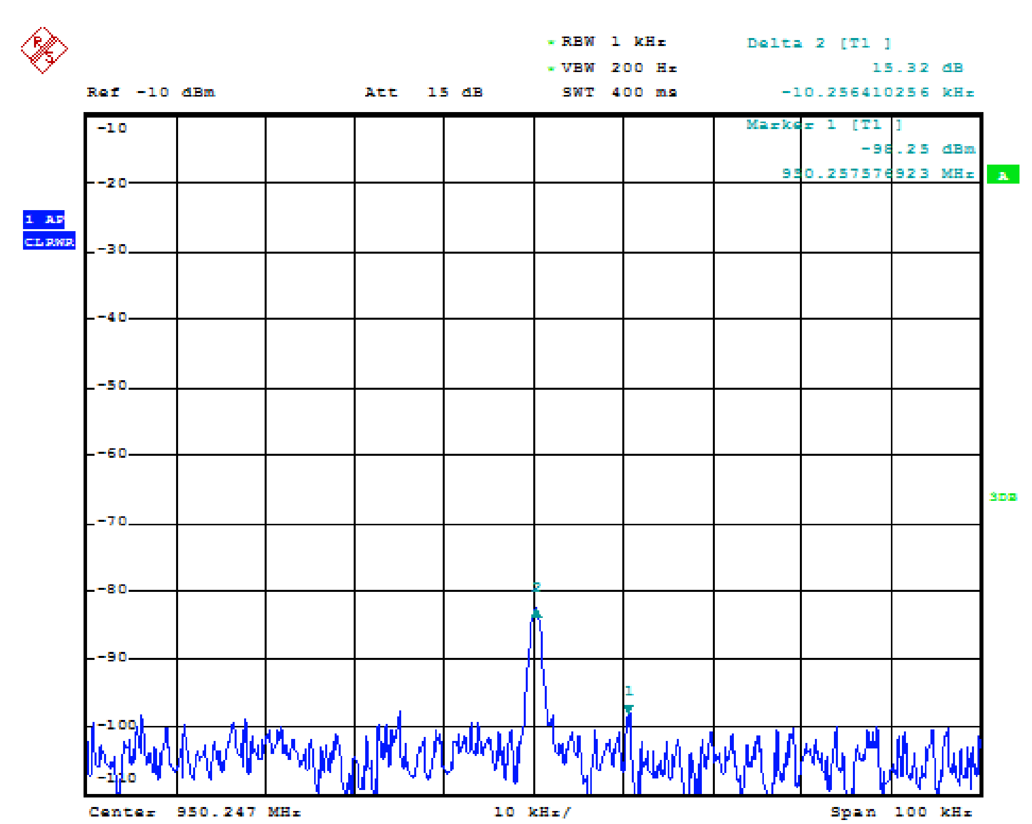


Fig 11. IF spectrum around 38th XO harmonic, no RF input signal

Now clearly only the 38th harmonic of the XO becomes visible at an absolute level of -83 dBm. This spurious is independent from the presence of a RF input frequency. Remark: the spurious is at 950.247 MHz; hence the XO frequency has a small offset from the 25 MHz (0.0065 MHz). This offset can be tuned out by using a crystal with proper load capacitance and/or using additional load capacitance to GND.

The NXO spurious behavior over Spurious Offset Frequency is shown in the figure below. For spurious frequencies above the PLL loop-filter BW the spurious ratio improves.

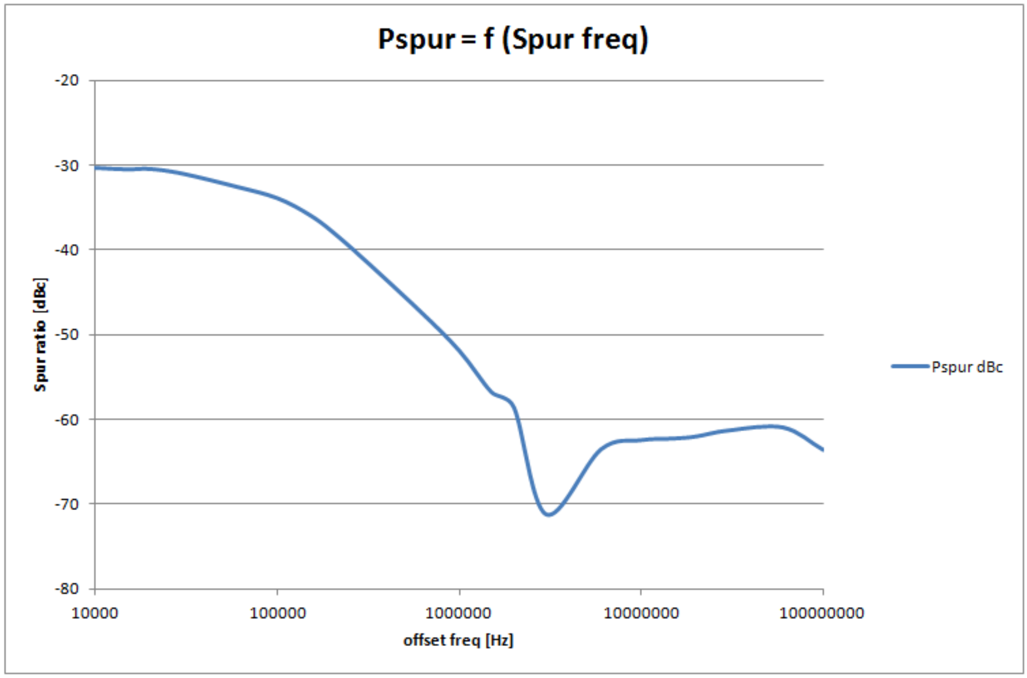


Fig 12. NXO spurious ratio = f (offset frequency)

4.1.1 Do's and don'ts with respect to NXO spurious

1) Keep tracks to the crystal as balanced as possible, meaning use two 0.15mm lines with 0.1mm spacing. Avoid large differences in line length between XO1 and XO2 connections.
2) Avoid to have the IF output TL running parallel to the XO lines, if this cannot be avoided create isolation by putting GND strips in between (with via holes connected to the GND plane).
3) Insert a serial SMD inductor (NXP reference Murata LQG15 series, 6.8nH) in each XO line, possibly close to the TFF1024.

4.2 Loop filter optimization

The PLL loop filter determines the LO phase Noise / Phase Jitter properties (within certain borders) and is dimensioned such to get optimum performance for all LO frequencies. In case one wants to experiment with this design a SW tool, called PLL applet running under Java, can be found on the NXP internet pages (search for "LO PLL calculator" or "PLL Applet").
An example for the TFF1024 settings is shown in the figure below. By clicking on the subjects (bold text) a help function should pop up.

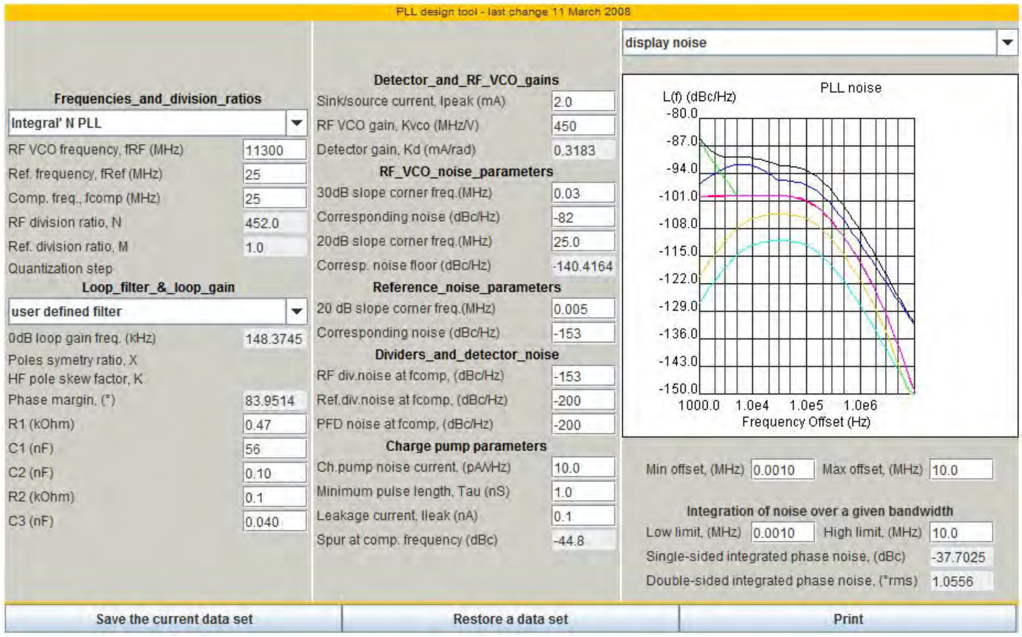


Fig 13. PLL design tool with 11.3 GHz settings

Measured the PN looks like this:

Fig 14. Measure Phase Noise and Jitter at 11.3 GHz

4.3 Using an external reference clock

In some applications, like multiple feed-horn LNB, multi IF LNB or LNB that require high frequency accuracy, there is a need to share the same reference amongst the various Down Converter IC's (DCV) or to supply the XO1/XO2 pins with an external reference.
In case multiple TFF1024 devices are used in one application it is important that the LO's of all DCV should be frequency and phase locked, if not pulling issues might rise.

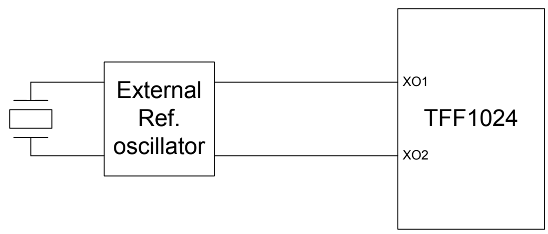


Fig 15. TFF1024 using external PLL reference

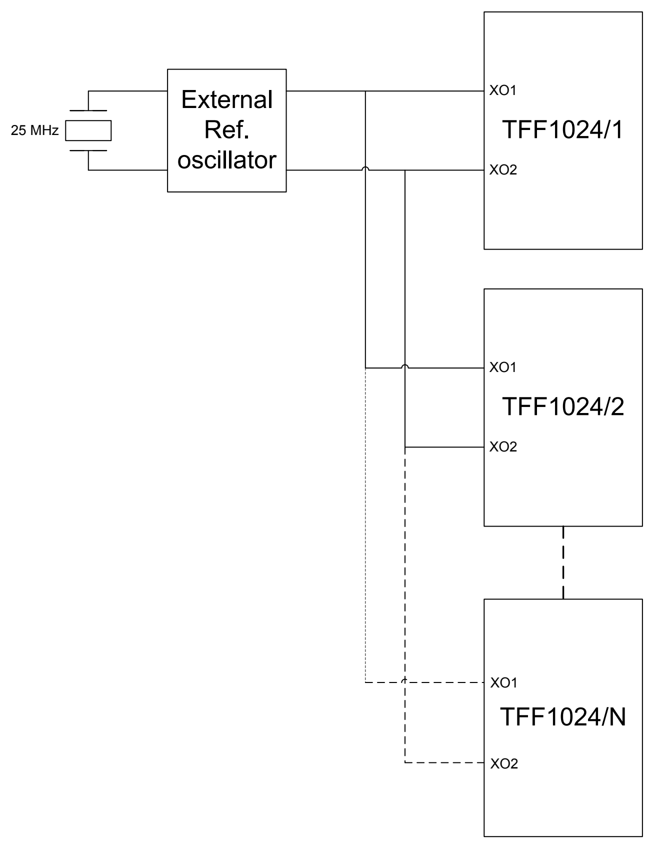


Fig 16. Multiple TFF1024 using single PLL reference

Please note that the DC blocking capacitors are not drawn. Also to improve NXO performance it is recommended to put a 6.8nH 0402 inductor in each XO line as close to the TFF1024 as possible.

Using one X-tal parallel on more than 2 DCV XO's will change the load and driver level on the X-tal during the start up and switching off not used LNC's. This has negative impact on the integrated phase noise and reference signal frequency accuracy.
To avoid those negative impacts an X-tal oscillator driver (74LVC1GX04) is used.
The TFF1024 LO needs differential signal as reference, therefore the X-tal driver should have two outputs with 180 deg phase shift.

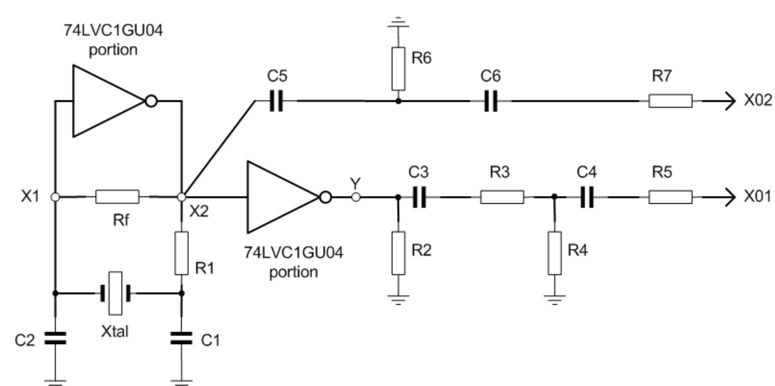
4.3.1 Application Circuit for X-tal driver 74LVC1GX04

To get the best phase noise performance, the TFF1024 LO needs a differential reference signal with a peak to peak value of 1.5V. And high isolation between the X-tal driver output and the X-tal, this will avoid frequency shift at different X-tal driver output loadings.

The X-tal driver provides a differential output (180 degree phase shift) but the output levels and acceptable loads are not identical.

To get the same level (1.5Vpp) at both TFF1024 LO-inputs, resistor dividers are used at the X-tal driver outputs. The resistors also give enough isolation between the LO's and the Crystal.

The used resistors matching circuit can be changed / simplified to own requirements.



(1)

Fig 17. X-tal driver application circuit for differential output (1.5 Vpp)

4.3.2 X-tal driver BOM

Table 4. X-tal driver Components

Component	Description	Remark
C1	12 pF	X-tal load C
C2	12 pF	X-tal load C
C3-C6	68 nF	DC-block
Rf	1 M ohm	feedback
R1	330 ohm	drive-limiting
R2	510 ohm	load resistor
R3	51 ohm	output match
R4	1100 ohm	output match

Component	Description	Remark
R5	300 ohm	output match
R6	2000 ohm	output match
R7	300 ohm	output match
X-tal	25 MHz	Crystal
74LVC1GX04	X-tal driver	

4.3.3 Measurements (X-tal driver output signal)

The picture shows the reference signal (25 MHz / 1.5 Vpp) using the schematic above and driving three LO's.

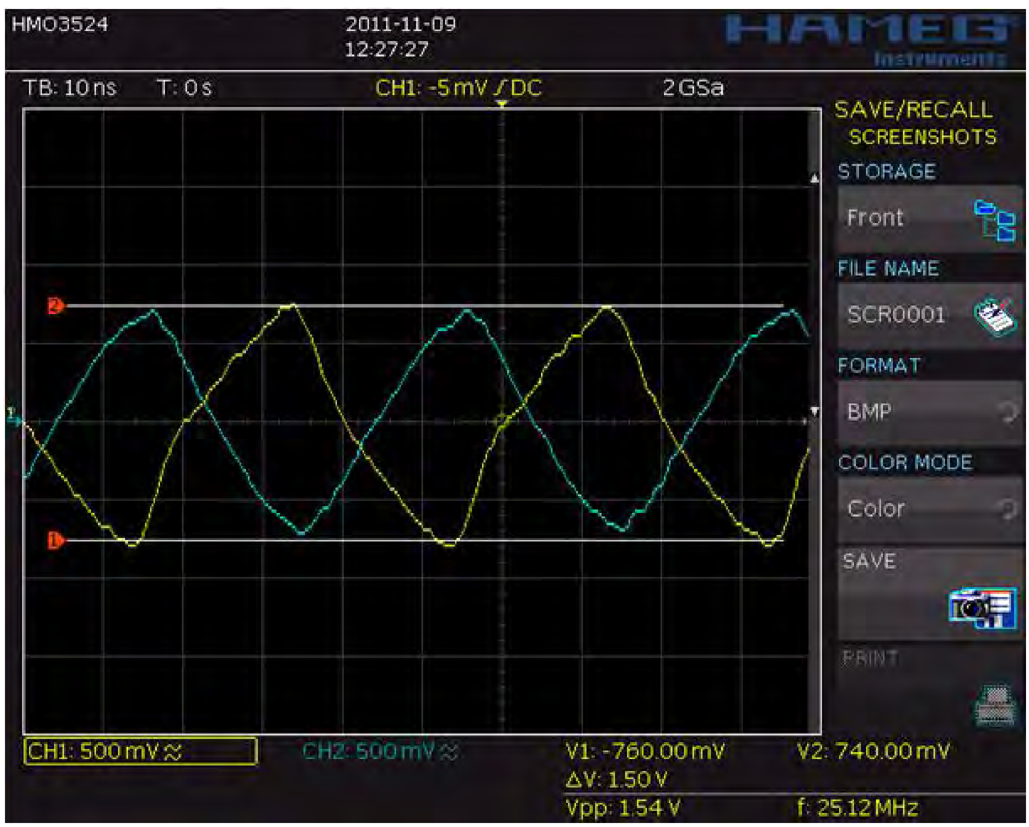


Fig 18. X-tal driver output signals over time

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6. List of figures

7. List of tables

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