

# DATA SHEET

## **TDA8706A**

**6-bit analog-to-digital converter  
with multiplexer and clamp**

Product specification  
Supersedes data of 1996 Jul 30

2003 Jul 21

## 6-bit analog-to-digital converter with multiplexer and clamp

## TDA8706A

### FEATURES

- 6-bit resolution
- Binary CMOS compatible outputs
- CMOS compatible digital inputs
- TLL clock input
- Three multiplexed video inputs
- R, G and B clamps on code 0
- Single 6-bit Analog-to-Digital Converter (ADC) operation allowed up to 40 MSPS
- External control of clamping level
- Internal reference voltage (external reference allowed)
- Power dissipation only 36 mW (typical)
- Operating temperature of  $-40$  to  $+85$  °C
- Operating between 2.7 and 3.6 V
- Sine wave clock allowed.

### APPLICATIONS

- General purpose video applications
- R, G and B signals
- Automotive (car navigation)
- LCD systems
- Frame grabber.

### GENERAL DESCRIPTION

The TDA8706A is a 6-bit ADC with three analog multiplexed inputs. Each input has an analog clamp on code 0 for RGB video processing. Clamping level can also be adjusted externally up to code 20. It can also be used as a single 6-bit ADC.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDA}$	analog supply voltage		2.7	3.3	3.6	V
$V_{DDD}$	digital supply voltage		2.7	3.3	3.6	V
$V_{DDO}$	output stage supply voltage		2.7	3.3	3.6	V
$I_{DDA}$	analog supply current		–	6.4	10	mA
$I_{DDD}$	digital supply current		–	4.4	8.5	mA
$I_{DDO}$	output stage supply current	$f_{clk} = 40$ MHz; ramp input	–	–	1.8	mA
INL	integral non-linearity	$f_{clk} = 40$ MHz; ramp input	–	$\pm 0.20$	$\pm 0.5$	LSB
DNL	differential non-linearity	$f_{clk} = 40$ MHz; ramp input	–	$\pm 0.10$	$\pm 0.35$	LSB
$f_{clk(max)}$	maximum clock frequency		40	–	–	MHz
$P_{tot}$	total power dissipation	$f_{clk} = 40$ MHz; ramp input	–	36	73	mW

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8706AM	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

# 6-bit analog-to-digital converter with multiplexer and clamp

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## BLOCK DIAGRAM

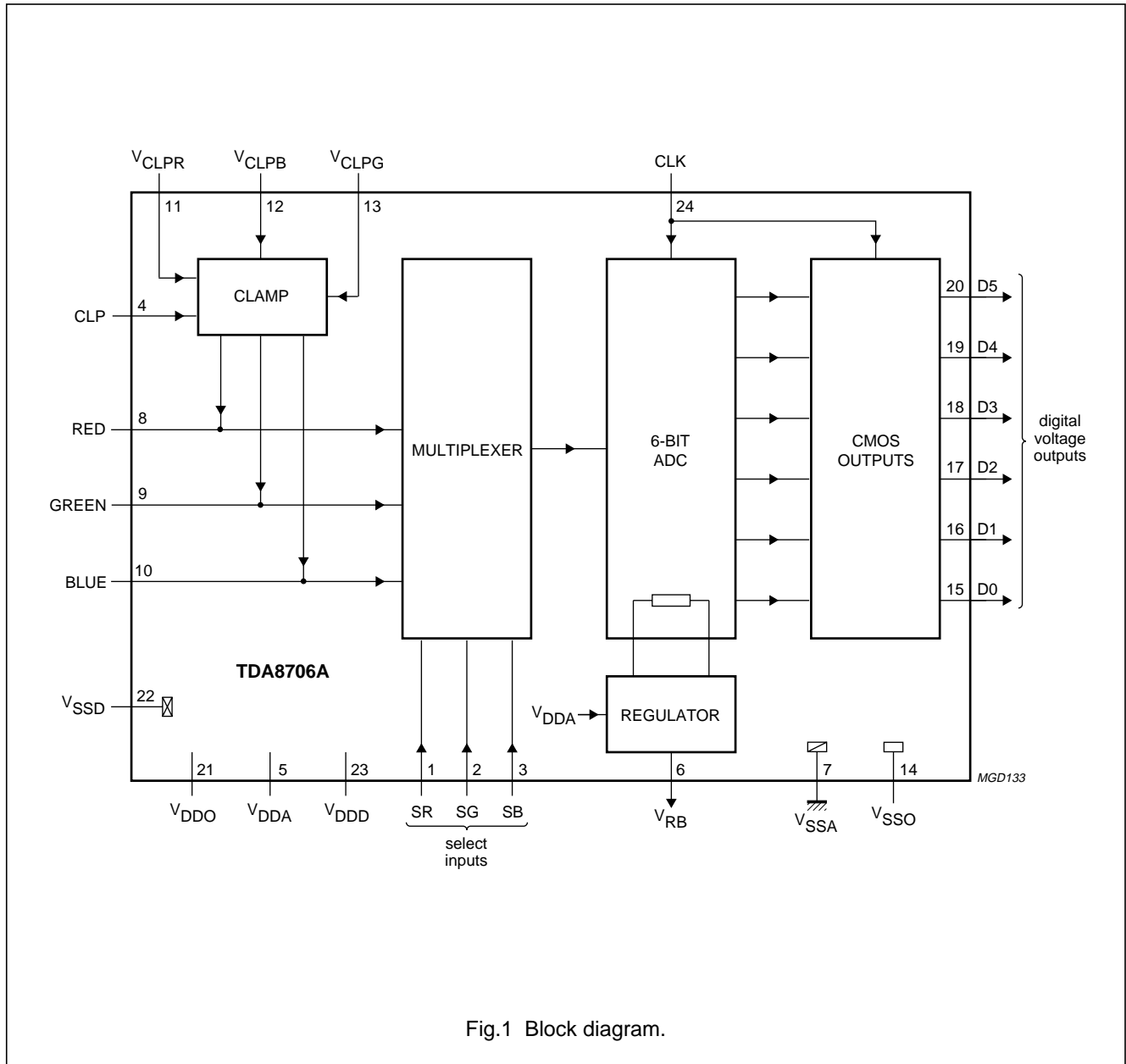


Fig.1 Block diagram.

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### PINNING

SYMBOL	PIN	DESCRIPTION
SR	1	select input RED
SG	2	select input GREEN
SB	3	select input BLUE
CLP	4	clamping pulse input (positive pulse)
V <sub>DDA</sub>	5	analog supply voltage
V <sub>RB</sub>	6	reference voltage BOTTOM output
V <sub>SSA</sub>	7	analog ground
RED	8	RED input
GREEN	9	GREEN input
BLUE	10	BLUE input
V <sub>CLPR</sub>	11	RED clamping voltage level input
V <sub>CLPB</sub>	12	BLUE clamping voltage level input
V <sub>CLPG</sub>	13	GREEN clamping voltage level input
V <sub>SSO</sub>	14	output stage ground
D0	15	digital voltage output; bit 0 (LSB)
D1	16	digital voltage output; bit 1
D2	17	digital voltage output; bit 2
D3	18	digital voltage output; bit 3
D4	19	digital voltage output; bit 4
D5	20	digital voltage output; bit 5
V <sub>DDO</sub>	21	output stage supply voltage
V <sub>SSD</sub>	22	digital ground
V <sub>DDD</sub>	23	digital supply voltage
CLK	24	clock input

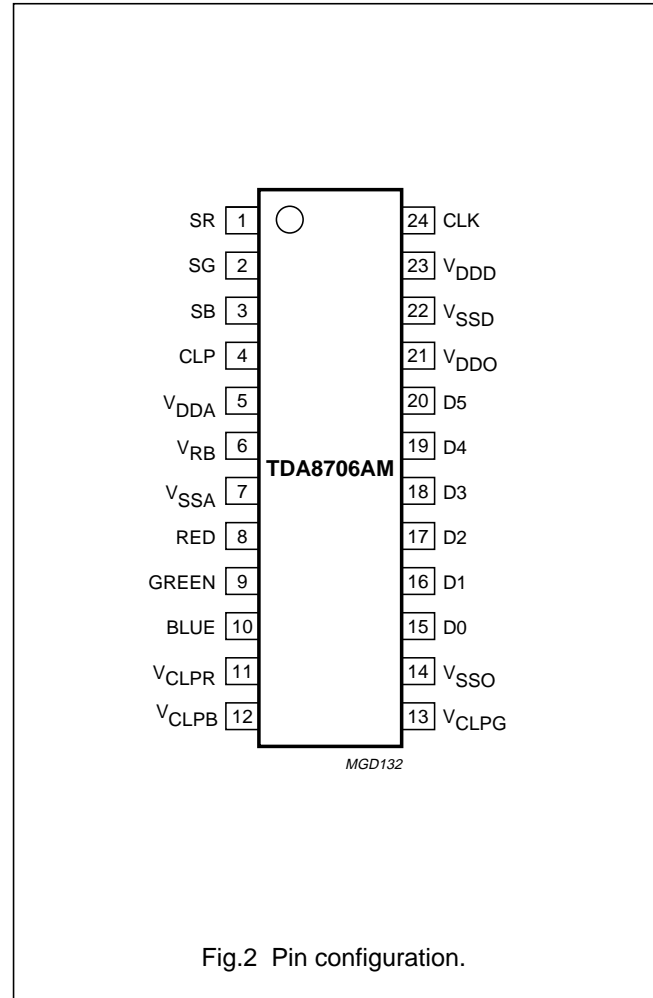


Fig.2 Pin configuration.

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DDA}$	analog supply voltage	-0.3	+7.0	V
$V_{DDD}$	digital supply voltage	-0.3	+7.0	V
$\Delta V_{DD}$	supply voltage difference			
	$V_{DDA} - V_{DDD}$	-1.0	+1.0	V
	$V_{DDA} - V_{DDO}$	-1.0	+1.0	V
	$V_{DDD} - V_{DDO}$	-1.0	+1.0	V
$V_I$	input voltage	-0.3	+7.0	V
$I_O$	output current	-	10	mA
$T_{stg}$	storage temperature	-55	+150	°C
$T_{amb}$	operating ambient temperature	-40	+85	°C
$T_j$	junction temperature	-	150	°C

### HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	119	K/W

### CHARACTERISTICS

$V_{DDA} = 2.7$  to  $3.6$  V;  $V_{DDD} = 2.7$  to  $3.6$  V;  $V_{DDO} = 2.7$  to  $3.6$  V;  $V_{SSA}$ ,  $V_{SSD}$  and  $V_{SSO}$  shorted together;  $V_{i(p-p)} = 0.7$  V;  $T_{amb} = -40$  to  $+85$  °C; typical values measured at  $V_{DDA} = V_{DDD} = V_{DDO} = 3.3$  V and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{DDA}$	analog supply voltage		2.7	3.3	3.6	V
$V_{DDD}$	digital supply voltage		2.7	3.3	3.6	V
$V_{DDO}$	output stage supply voltage		2.7	3.3	3.6	V
$\Delta V_{DD}$	supply voltage difference					
	$V_{DDA} - V_{DDD}$		-0.3	-	+0.3	V
	$V_{DDA} - V_{DDO}$		-0.3	-	+0.3	V
	$V_{DDD} - V_{DDO}$		-0.3	-	+0.3	V
$I_{DDA}$	analog supply current		-	6.4	10	mA
$I_{DDD}$	digital supply current		-	4.4	8.5	mA
$I_{DDO}$	output stage supply current	$f_{clk} = 40$ MHz; ramp input	-	-	1.8	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$P_{\text{tot}}$	total power dissipation		–	36	73	mW
<b>Inputs</b>						
CLOCK INPUT CLK (REFERENCED TO $V_{\text{SSD}}$ ); note 1						
$V_{\text{IL}}$	LOW-level input voltage		0	–	0.8	V
$V_{\text{IH}}$	HIGH-level input voltage		2.0	–	$V_{\text{DDD}}$	V
$I_{\text{IL}}$	LOW-level input current	$V_{\text{clk}} = 0.8 \text{ V}$	–1	0	+1	$\mu\text{A}$
$I_{\text{IH}}$	HIGH-level input current	$V_{\text{clk}} = 2.0 \text{ V}$	–	2	10	$\mu\text{A}$
$Z_{\text{i}}$	input impedance	$f_{\text{clk}} = 40 \text{ MHz}$	–	4	–	$\text{k}\Omega$
$C_{\text{i}}$	input capacitance	$f_{\text{clk}} = 40 \text{ MHz}$	–	3	–	pF
INPUTS SR, SG, SB AND CLP (REFERENCED TO $V_{\text{SSD}}$ )						
$V_{\text{IL}}$	LOW-level input voltage		0	–	$V_{\text{DDD}} \times 0.3$	V
$V_{\text{IH}}$	HIGH-level input voltage		$V_{\text{DDD}} \times 0.7$	–	$V_{\text{DDD}}$	V
$I_{\text{IL}}$	LOW-level input current	$V_{\text{IL}} = V_{\text{DDD}} \times 0.2$	–1	–	–	$\mu\text{A}$
$I_{\text{IH}}$	HIGH-level input current	$V_{\text{IH}} = V_{\text{DDD}} \times 0.8$	–	–	+1	$\mu\text{A}$
INPUTS $V_{\text{CLPR}}$ , $V_{\text{CLPG}}$ AND $V_{\text{CLPB}}$ (REFERENCED TO $V_{\text{SSA}}$ ); see Tables 1 and 2						
$V_{\text{CLP}}$	input voltage for clamping		$V_{\text{code}(-9)}$	–	$V_{\text{code}(20)}$	V
$I_{\text{CLP}}$	input current		–	–	30	$\mu\text{A}$
$A_{\text{CLP}}$	clamp accuracy	between inputs RED, GREEN and BLUE of each device; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	–1	–	+1	LSB
ANALOG INPUTS RED, GREEN AND BLUE; see Table 1						
$V_{\text{i(p-p)}}$	input voltage amplitude (peak-to-peak value)		0.63	0.70	0.77	V
$I_{\text{i}}$	input current		–	–	10	$\mu\text{A}$
$C_{\text{clamp}}$	clamp coupling capacitance		1	10	100	nF
<b>Reference voltages for the resistor ladder; see Table 1</b>						
$V_{\text{RB}}$	BOTTOM reference voltage		$V_{\text{DDA}} - 1.29$	$V_{\text{DDA}} - 1.21$	$V_{\text{DDA}} - 1.13$	V
<b>Outputs</b>						
DIGITAL OUTPUTS D5 TO D0 (REFERENCED TO $V_{\text{SSD}}$ )						
$V_{\text{OL}}$	LOW-level output voltage	$I_{\text{O}} = 1 \text{ mA}$	0	–	0.5	V
$V_{\text{OH}}$	HIGH-level output voltage	$I_{\text{O}} = -1 \text{ mA}$	$V_{\text{DDO}} - 0.5$	–	$V_{\text{DDO}}$	V
<b>Switching characteristics</b>						
CLOCK INPUT CLK; see Fig.3; note 1						
$f_{\text{clk(max)}}$	maximum clock frequency		40	–	–	MHz
$f_{\text{mux(max)}}$	maximum multiplexer frequency		20	–	–	MHz
$t_{\text{CPH}}$	clock pulse width HIGH		9	–	–	ns
$t_{\text{CPL}}$	clock pulse width LOW		9	–	–	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_r$	clock rise time	10% to 90%; $f_{clk} \leq 40$ MHz; LOW = 0.8 V, HIGH = 2.0 V	–	–	7	ns
$t_f$	clock fall time	90% to 10%; $f_{clk} \leq 40$ MHz; LOW = 0.8 V, HIGH = 2.0 V	–	–	7	ns
<b>Analog signal processing</b>						
LINEARITY						
INL	integral non-linearity	$f_{clk} = 40$ MHz; ramp input	–	$\pm 0.20$	$\pm 0.5$	LSB
DNL	differential non-linearity	$f_{clk} = 40$ MHz; ramp input	–	$\pm 0.10$	$\pm 0.35$	LSB
EFFECTIVE BITS; note 2						
EB	effective bits	$f_{clk} = 40$ MHz; $f_i = 4.43$ MHz	5.5	5.8	–	bits
<b>Timing (<math>f_{clk} = 40</math> MHz; <math>C_L = 10</math> pF); see Fig.3</b>						
OUTPUT DATA; note 3						
$t_{ds}$	sampling delay time		–	–	7	ns
$t_h$	output hold time		6.5	9.0	–	ns
$t_d$	output delay time		–	12	19	ns
SELECT INPUT SIGNALS SR, SG, SB AND CLP						
$t_{su}$	set-up time SR, SG and SB	with no overlap; see Fig.3	10	–	–	ns
		with overlap; see Fig.4	–	–	–	ns
$t_r$	rise time SR, SG and SB	10% to 90%	4	6	–	ns
$t_f$	fall time SR, SG and SB	90% to 10%	4	6	–	ns
$t_{over}$	RED, GREEN and BLUE (active) overlap time with respect to select signals SR, SG and SB	see Fig.4	0	–	–	ns
$t_{CLPP}$	clamp pulse time	$C_{CLP} = 10$ nF	–	3	–	$\mu$ s
$t_{MH}$	multiplexer hold time SR, SG and SB		9	–	–	ns

### Notes

- In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns. A sine wave with specified amplitude is also allowed.
- Effective bits are derived from a Fast Fourier Transform (FFT) processing taking 2K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio:  $S/N = EB \times 6.02 + 1.76$  dB.
- Output data acquisition: the output data is available after the maximum delay time  $t_d$ .

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**Table 1** Output coding and input voltage (typical values);  $V_{DDA} = V_{DDD} = 3.3\text{ V}$ 

STEP	$V_i$ (V)	BINARY OUTPUT BITS					
		D5	D4	D3	D2	D1	D0
Underflow	$<V_{DDA} - 1.12$	0	0	0	0	0	0
0	$V_{DDA} - 1.12$	0	0	0	0	0	0
1	.	0	0	0	0	0	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
62	.	1	1	1	1	1	0
63	$V_{DDA} - 0.42$	1	1	1	1	1	1
Overflow	$>V_{DDA} - 0.42$	1	1	1	1	1	1

**Table 2** Clamping input level ( $V_{CLPR}$ ,  $V_{CLPG}$  and  $V_{CLPB}$ )

$V_{CLPR}$ , $V_{CLPG}$ , $V_{CLPB}$	CLAMPING LEVEL
Open-circuit <sup>(1)</sup>	code 0
$V_{code(-9)}$ to $V_{code(20)}$	code -9 to code 20

**Note**

- Use capacitor  $\geq 10\text{ pF}$  to  $V_{SSA}$ .

**Table 3** Clamp and inputs RED, GREEN and BLUE;  $V_{DDA} = V_{DDD} = V_{DDO} = 3.3\text{ V}$ 

SR or SG or SB	CLAMP	$V_{CLPR}$ , $V_{CLPG}$ or $V_{CLPB}$	$V_i$ RED or GREEN or BLUE	DIGITAL OUTPUTS
0	1	open	$V_{DDA} - 1.12\text{ V}$	don't care
		$V_{CLP}$	$V_{CLP}$	
1		open	$V_{DDA} - 1.12\text{ V}$	0
		$V_{CLP}$	$V_{CLP}$	code ( $V_{CLP}$ )



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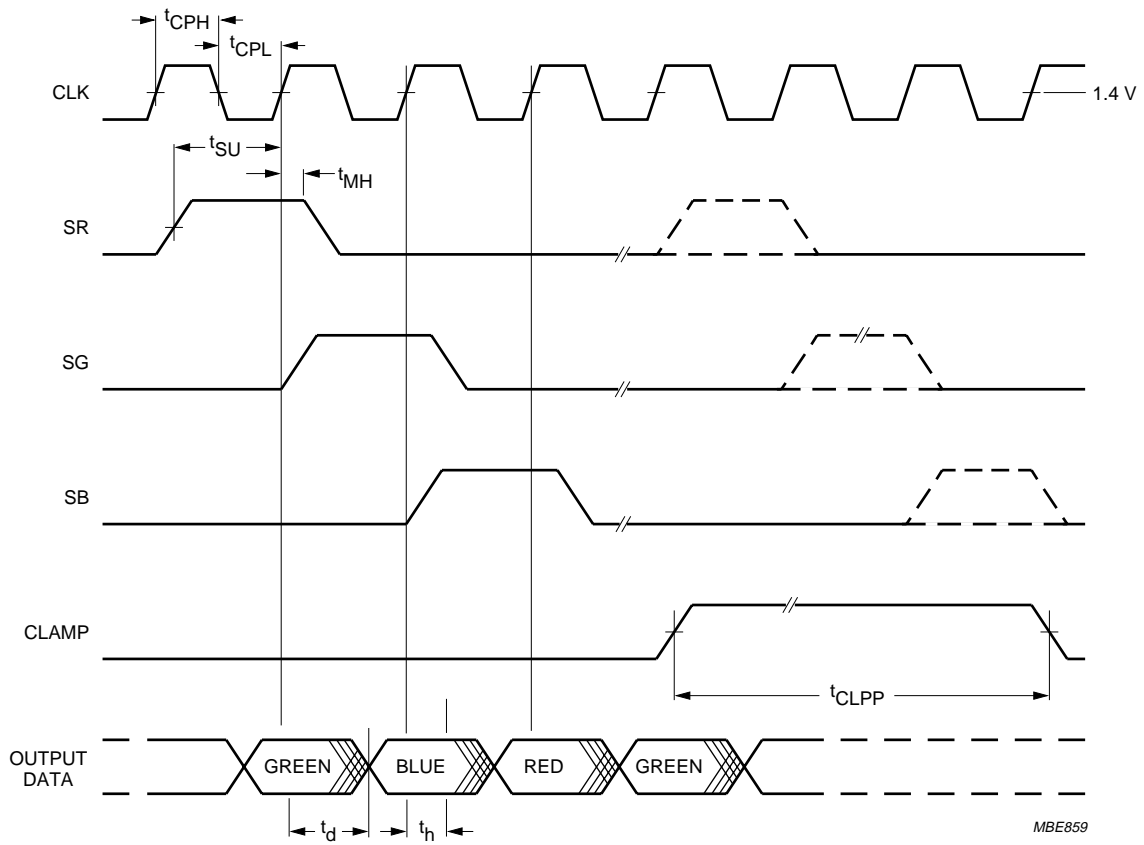


Fig.3 AC characteristics select signals, clamp and output data.

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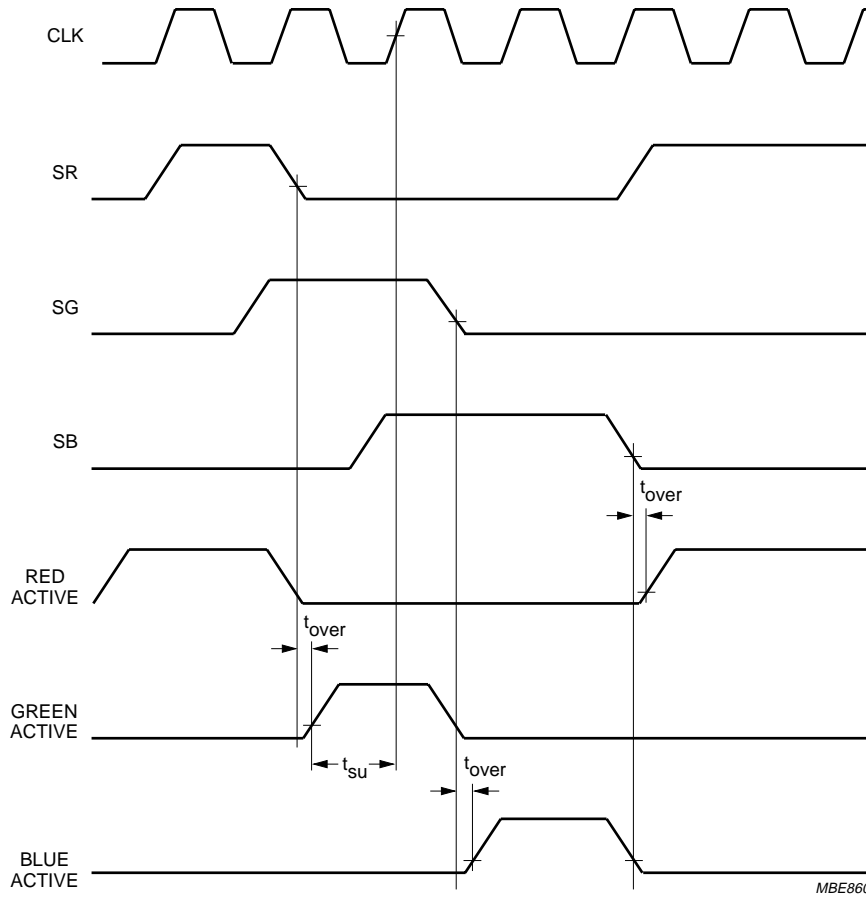


Fig.4 Anti-overlap system for analog multiplexer.

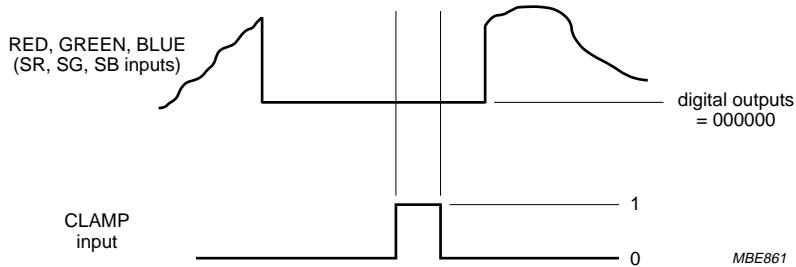
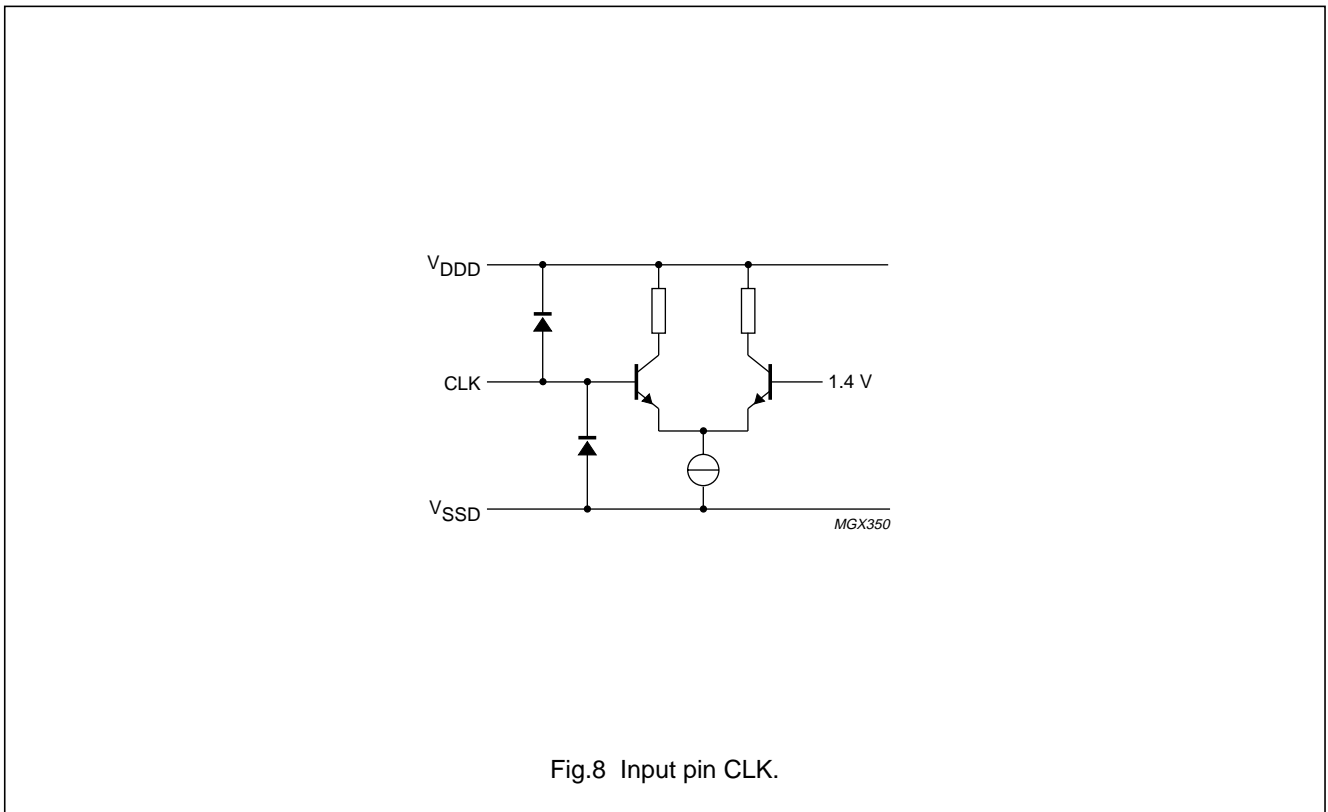
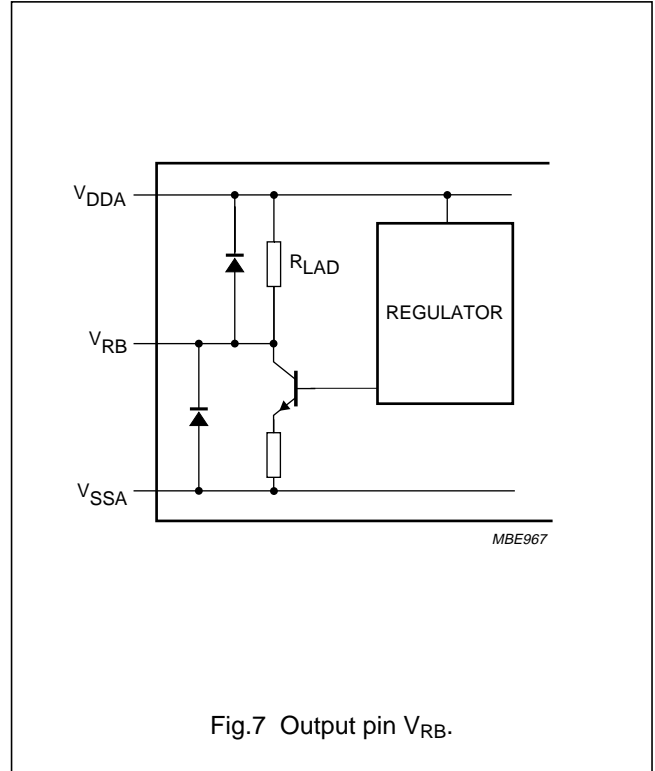
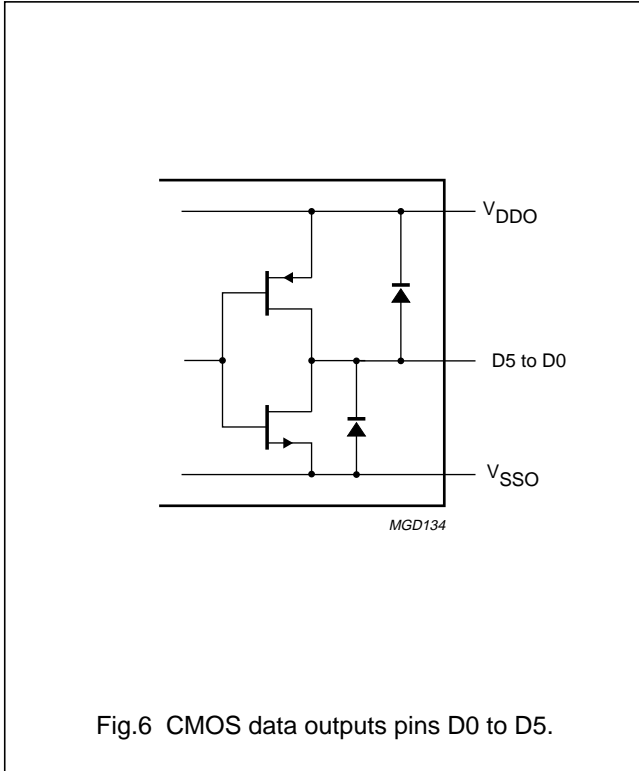


Fig.5 AC characteristics select signals; clamp and data.

# 6-bit analog-to-digital converter with multiplexer and clamp

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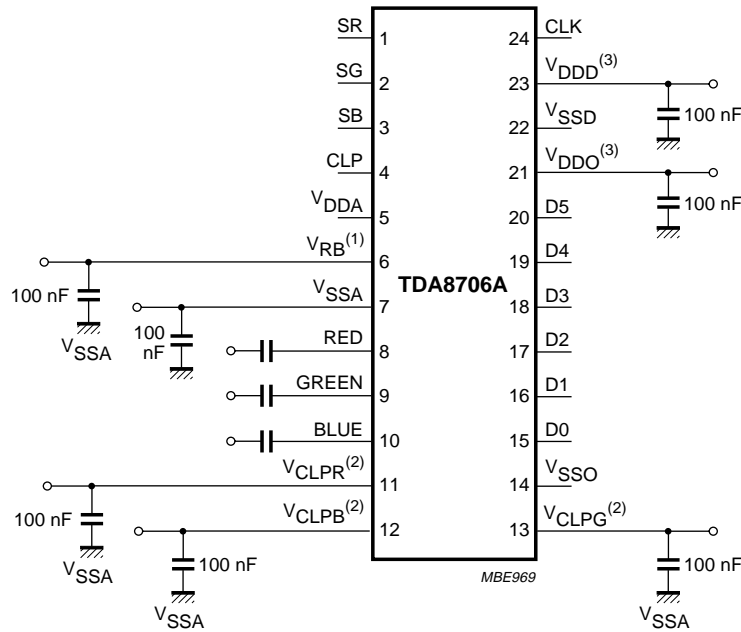
## INTERNAL PIN CONFIGURATIONS



# 6-bit analog-to-digital converter with multiplexer and clamp

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### APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

$V_{DDO}$  should be well decoupled with its capacitor in order to be as close as possible to its pin.

$V_{RB}$  must not be connected to  $V_{CLPR}$ ,  $V_{CLPB}$  or  $V_{CLPG}$  pins.

For applications where the black level is clamped to code 0,  $V_{CLPR}$ ,  $V_{CLPB}$  and  $V_{CLPG}$  must be left open-circuit with their respective decoupling capacitors. In that event, they may also be connected together in order to use only one single decoupling capacitor.

- (1)  $V_{RB}$  is decoupled to  $V_{SSA}$ . An external regulator can also be connected to  $V_{RB}$ .
- (2)  $V_{CLPR}$ ,  $V_{CLPB}$  and  $V_{CLPG}$  are decoupled to  $V_{SSA}$ . External voltages can also be forced on  $V_{CLPR}$ ,  $V_{CLPB}$  and  $V_{CLPG}$ .
- (3)  $V_{DDO}$  and  $V_{DDO}$  can be shorted together but the decoupling capacitors should remain as close as possible to its pin.

Fig.9 Application diagram.

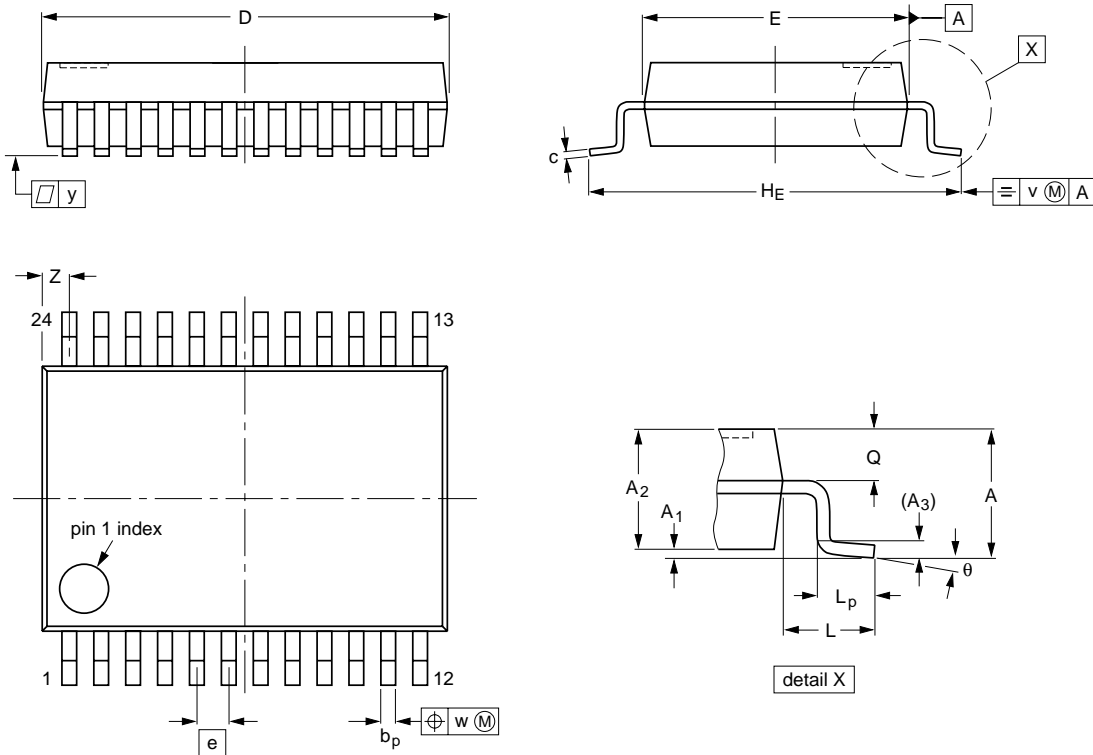
# 6-bit analog-to-digital converter with multiplexer and clamp

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## PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				99-12-27 03-02-19

## 6-bit analog-to-digital converter with multiplexer and clamp

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness  $\geq 2.5$  mm and packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages
- below 235 °C for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(3)</sup>	suitable
PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(6)</sup>	suitable

#### Notes

- For more detailed information on the BGA packages refer to the "*(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*".
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

### Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

### DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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