UM11385

P3A9606JK-EVB evaluation board

Rev. 1.0 — 21 June 2020 **User manual**

Document information

Information	Content
Keywords	P3A9606JK, Level Shifter, Level Translator, P3A9606JK-EVB evaluation board
Abstract	The P3A9606JK is a 2-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation. This user manual describes the setup, configuration and operation of the P3A9606JK-EVB evaluation board.

Revision history

Rev	Date	Description
v.1.0	20210621	Initial version

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1 Introduction

The P3A9606JK is a 2-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation. It features two 1-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (VCC(A) and VCC(B)). VCC(A) can be supplied at any voltage between 0.7 V and 1.98 V and VCC(B) can be supplied at any voltage between 0.7 V and 1.98 V, making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V and 1.8 V). VCC(A) must be ≤ VCC(B) for minimum current consumption.

P3A9606JK can be used for both Open Drain as well as push-pull application which allows for level translation applications using SPMI, I2C and SPI protocols (see datasheet application section).

This document is intended to help the users to quickly setup, configure and operate the P3A9606JK-EVB evaluation board in the users' hardware platform.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for P3A9606JK-EVB evaluation board is at https://www.nxp.com/P3A9606JK-EVB.

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3 Getting to know the hardware

3.1 Kit overview

P3A9606JK can be used as a stand-alone level shifter when a CERES is not available for evaluation and testing. The user can manually connect the signals to be shifted to port A1/A0 and B1/B0 of the P3A9606JK. External VCCA/VCCB can be manually selected and connected to the evaluation board.

As default, P3A9606JK-EVB evaluation board is configured (with jumper settings) to be mated to a CERES motherboard serial expansion bus as a level shifter on the SPMI bus. If needed, P3A9606JK-EVB evaluation board can be bypassed using jumper settings to remove it from the SPMI bus.

The evaluation boards are shipped with a P3A9606JK soldered on as U1; a socket (U2 on the schematic) can be used in place of U1 to allow the user the flexibility of repeatedly replacing P3A9606JK multiple times. U1 and U2 share the same PCB footprint, therefore, U1 must be removed first before U2 as a socket can be installed.

3.2 Connectors and jumpers

Please refer to Figure 1 to find the location of connectors and jumpers on the evaluation board.

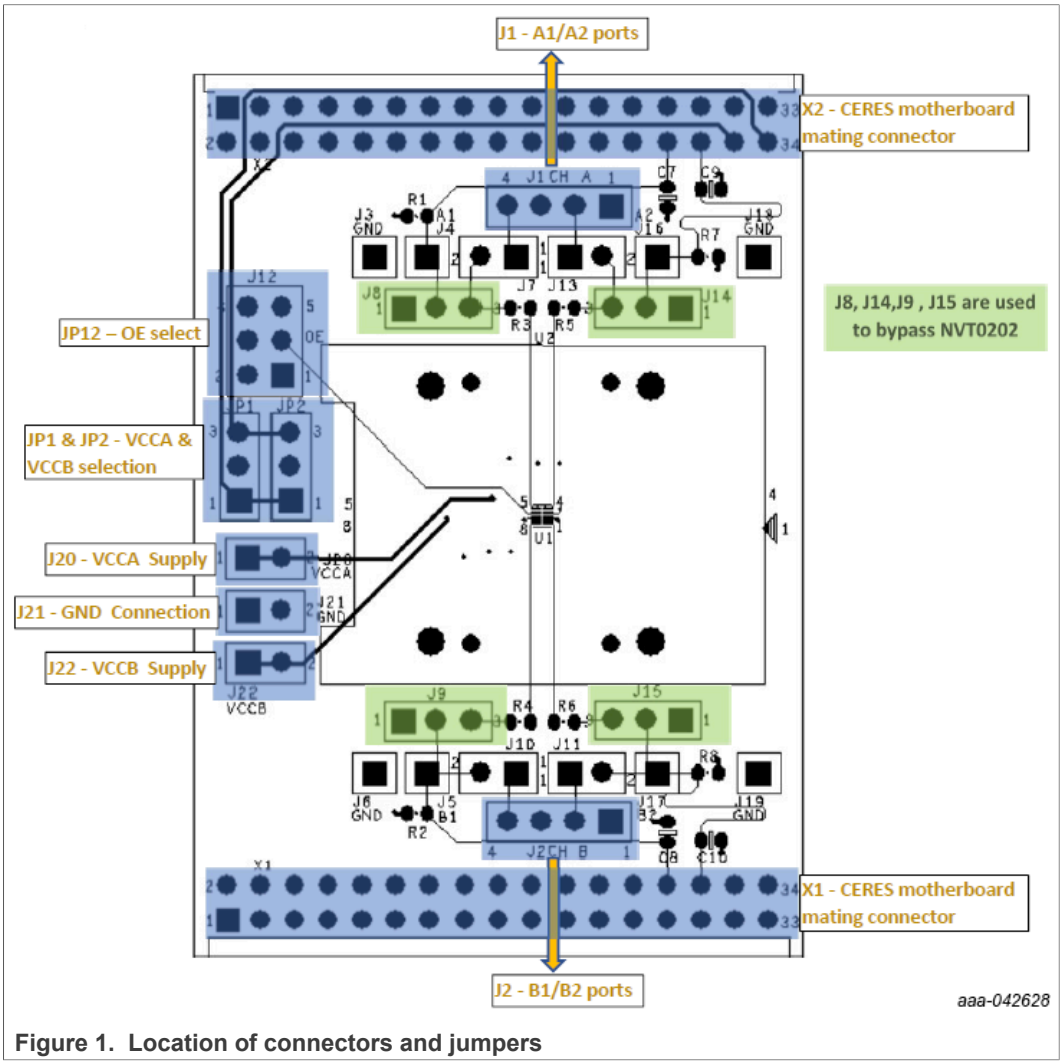

Figure 1. Location of connectors and jumpers

3.3 Default jumper settings (CERES motherboard SPMI bus option)

As default, P3A9606JK-EVB evaluation board is configured to be mated to a CERES motherboard serial expansion bus as a level shifter on the SPMI bus as shown in Table 1.

Table 1. Default jumper settings

Header	Jumper on	Comment
J8	2-3	Select P3A9606JK port A1
J9	2-3	Select P3A9606JK port B1
J14	2-3	Select P3A9606JK port A2
J15	2-3	Select P3A9606JK port B2
J12	1-3	OE is connected to VCCA

Table 1. Default jumper settings...*continued*

Header	Jumper on	Comment
JP2	Open	VCCA is supplied from external, J20
JP1	Open	VCCB is supplied from external, J22
J7	Open	Not used, CERES motherboard is on port A1
J10	Open	Not used, CERES motherboard is on port B1
J13	Open	Not used, CERES motherboard is on port B1
J11	Open	Not used, CERES motherboard is on port B2

3.4 Non-CERES motherboard jumper settings

P3A9606JK can be used as a stand-alone level shifter when a CERES is not available for evaluation and testing. The user can manually connect the signals to be shifted to port A1/A2 and B1/B2 of the P3A9606JK through jumpers J7, J13, J10, J11 as shown in Table 2.

Table 2. Non-CERES motherboard jumper settings

Header	Jumper on	Comment
J8	2-3	Select P3A9606JK port A1
J9	2-3	Select P3A9606JK port B1
J14	2-3	Select P3A9606JK port A2
J15	2-3	Select P3A9606JK port B2
J12	1-3	OE is connected to VCCA
JP2	Open	VCCA is supplied from external, J20
JP1	Open	VCCB is supplied from external, J22
J7	1-2	Port A1 of signal to be shifted
J10	1-2	Port B1 of signal to be shifted
J13	1-2	Port A2 of signal to be shifted
J11	1-2	Port B2 of signal to be shifted

3.5 P3A9606JK bypass

P3A9606JK can be electrically removed and bypassed from the bus at any time, such as during debugging a level shifting issue. Once bypassed using the jumper settings from Table 3, signal on A1 is directly connected to B1 and signal on A2 is directly connected to B2.

Table 3. Bypass jumper settings

Header	Jumper on	Comment
J8	1-2	Select P3A9606JK port A1
J9	1-2	Select P3A9606JK port B1
J14	1-2	Select P3A9606JK port A2
J15	1-2	Select P3A9606JK port B2

3.6 Test points

There are a number of test points to allow the user to monitor and observe signals coming in and out of P3A9606JK.

Table 4. Test points

Signal	Test point	Alternative test point
A1	J4	J1 pin 4
A2	J13	J1 pin 2
B1	J10	J2 pin 4
B2	J11	J2 pin 2

4 Errata list

Table 5. Errata list

Date	Errata Description	Impact to evaluation board	Solution
-	None	None	None

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