TEF6721HL

Car radio tuner front-end for digital IF

Rev. 04 — 20 December 2005 Product data sheet

1. General description

The TEF6721HL is a single chip car radio tuner for AM, FM standard, FM In-Band On-Channel Digital Audio Broadcast (IBOC DAB) and weather band providing combined AM and FM gain controlled differential Intermediate Frequency (IF) output for the SAF7730H including the following functions:

- AM up-conversion tuner to an IF frequency of 10.7 MHz for Long Wave (LW)/Medium Wave (MW)/Short Wave (SW) (31 m, 41 m and 49 m bands)
- FM single conversion tuner to an IF frequency of 10.7 MHz with integrated image rejection for US FM, Europe FM, Japan FM, East Europe FM and weather band reception; all bands can be selected using high side or low side Local Oscillator (LO) injection
- Tuning system includes Voltage-Controlled Oscillator (VCO), crystal oscillator and Phase-Locked Loop (PLL) synthesizer on one chip.

2. Features

- FM mixer for conversion of FM Radio Frequency (RF) (64 MHz to 108 MHz and US weather band) to an IF of 10.7 MHz; the mixer provides inherent image rejection and can be switched from low injection to high injection Local Oscillator (LO) via the I^2C-bus; two different mixer conversion gains can be selected via the I^2C-bus
- Automatic Gain Control (AGC) PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input and IF AGC amplifier input; AGC threshold for detection at FM mixer input is a programmable and keyed function switchable via the I^2C-bus; the AGC PIN diode drive can be activated via the I^2C-bus as a local function for search tuning; in AM mode the AGC PIN diode drive can be activated via the I^2C-bus if required
- Digital alignment circuit for bus controlled matching of oscillator tuning voltage to FM antenna tank circuit tuning voltage
- Buffer output for weather band flag
- Combined AM and FM IF AGC amplifier with high dynamic input range; one of the four gain settings is selected automatically via two control signals from IF Digital Signal Processor (DSP); combined differential AM and FM IF output signal to analog-to-digital converter of IF DSP
- AM mixer for conversion of AM RF to AM IF 10.7 MHz
- AM RF PIN diode drive circuit and RF Junction Field Effect Transistor (JFET) conductance control by AGC cascode drive circuit; AGC threshold detection at AM mixer and IF AGC input; threshold for detection at AM mixer is programmable via the I^2C-bus
- AM and FM RF AGC monitor output intended for gain control of active antennas

- Inductor Capacitor (LC) tuner oscillator providing mixer frequencies for FM and AM mixers
- Crystal oscillator providing reference frequencies for synthesizer PLL and timing for Alternative Frequency (AF) updating
- Optional crystal oscillator frequency pulling possibility via I^2C-bus
- Fast synthesizer PLL tuning system with local control for inaudible AF updating
- Timing function for AF updating algorithm and control signal output for interfacing with IF DSP
- Three hardware programmable I^2C-bus addresses; pin BUSENABLE; two software controlled flag outputs
- Several test modes for fast Integrated Circuit (IC) tests.

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(n)}$	analog supply voltages 1 to 5		8	8.5	9	V
V_{DDA6}	analog supply voltage 6		4.75	5	5.25	V
V_{DDD}	digital supply voltage		4.75	5	5.25	V
$I_{DDA(n)}$	sum of analog supply currents 1 to 5	FM Japan mode	35	44	55	mA
		AM mode	28	38	48	mA
I_{DDA6}	analog supply current 6 for on-chip power supply	FM Japan mode	2.2	3.2	4.3	mA
		AM mode	10	14	18	mA
I_{DDD}	digital supply current	FM Japan mode	23	30	39	mA
		AM mode	17	23	30	mA
$f_{AM(ant)}$	AM input frequency	LW	0.144	-	0.288	MHz
		MW	0.522	-	1.710	MHz
		SW	5.73	-	9.99	MHz
$f_{FM(ant)}$	FM input frequency		64	-	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	-	162.55	MHz
T_{amb}	ambient temperature		–40	-	+85	°C
AM overall system parameters (based on 15 pF/60 pF dummy aerial; m = 0.3; 2.5 kHz audio bandwidth in IF DSP; voltages in RMS value at input of dummy aerial); see Figure 9						
$V_{i(RF)(IFAGC)}$	RF input voltage for start of IF AGC	first step	-	5.5	-	mV
		second step	-	11	-	mV
		third step	-	22	-	mV
$V_{i(RF)(RFAGC)}$	RF input voltage for start of RF AGC	in-band; m = 0	-	31	-	mV
		wideband; m = 0				
		AGC[1:0] = 00	-	92	-	mV
		AGC[1:0] = 01	-	126	-	mV
		AGC[1:0] = 10	-	168	-	mV
		AGC[1:0] = 11	-	210	-	mV

Table 1: Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{26dB}	sensitivity	f = 990 kHz	-	42	-	μV
IP3	3rd-order input intercept point	$\Delta f_{undesired}$ = 50 kHz	-	130	-	dBμV
		$\Delta f_{undesired}$ = 300 kHz	-	135	-	dBμV
IP2	2nd-order input intercept point		-	140	-	dBμV
FM overall system parameters (based on 75 Ω dummy aerial; Δf = 22.5 kHz; de-emphasis is 50 μs in IF DSP; voltages in RMS value at input of dummy aerial); see Figure 9						
$V_{i(RF)(IFAGC)}$	RF input voltage for start of IF AGC	first step	-	0.57	-	mV
		second step	-	1.1	-	mV
		third step	-	2.3	-	mV
$V_{i(RF)(RFAGC)}$	RF input voltage for start of wideband AGC	in-band	-	4.5	-	mV
		wideband				
		AGC[1:0] = 11	-	8	-	mV
		AGC[1:0] = 10	-	12	-	mV
		AGC[1:0] = 01	-	17	-	mV
		AGC[1:0] = 00	-	21	-	mV
α_{26dB}	sensitivity	f = 97 MHz	-	1.4	-	μV
IP3	3rd-order input intercept point	$\Delta f_{undesired}$ = 400 kHz	-	117	-	dBμV

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TEF6721HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

5. Block diagram

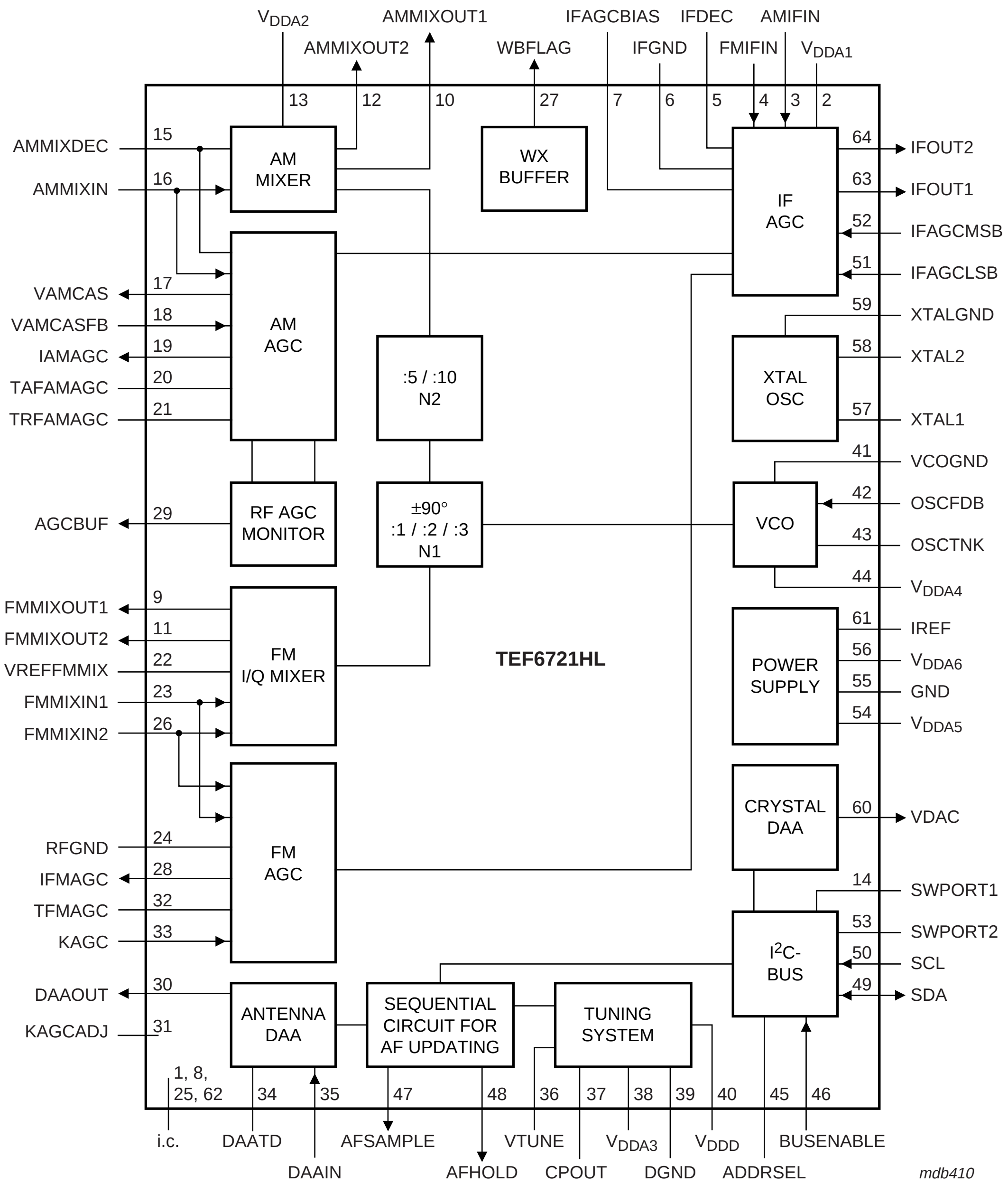


Fig 1. Block diagram of TEF6721HL

6. Pinning information

6.1 Pinning

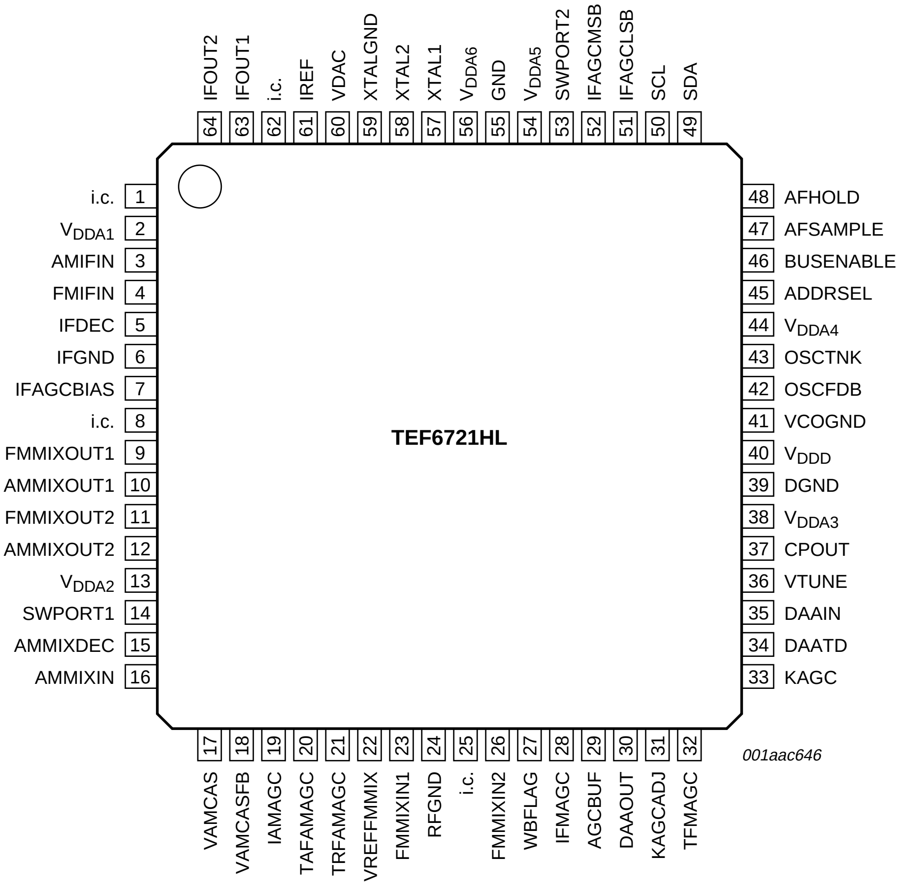


Fig 2. Pin configuration for LQFP64

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
i.c.	1	internally connected for test purposes; leave open-circuit
V_{DDA1}	2	analog supply voltage 1 (8.5 V) for IF AGC amplifier
AMIFIN	3	IF AGC amplifier AM input (10.7 MHz)
FMIFIN	4	IF AGC amplifier FM input (10.7 MHz)
IFDEC	5	IF AGC amplifier AM and FM decoupling
IFGND	6	IF AGC amplifier ground
IFAGCBIAS	7	bias voltage for IF AGC amplifier decoupling
i.c.	8	internally connected for test purposes; connect to ground
FMMIXOUT1	9	FM mixer IF output 1 (10.7 MHz)
AMMIXOUT1	10	AM mixer IF output 1 (10.7 MHz)

Table 3: Pin description *…continued*

Symbol	Pin	Description
FMMIXOUT2	11	FM mixer IF output 2 (10.7 MHz)
AMMIXOUT2	12	AM mixer IF output 2 (10.7 MHz)
V_{DDA2}	13	analog supply voltage 2 (8.5 V) for FM and AM RF
SWPORT1	14	software programmable port 1
AMMIXDEC	15	AM mixer decoupling
AMMIXIN	16	AM mixer input
VAMCAS	17	output for AM RF cascode AGC
VAMCASFB	18	feedback input for AM RF cascode AGC
IAMAGC	19	PIN diode drive current output of AM front-end AGC
TAFAMAGC	20	AF time constant of AM front-end AGC
TRFAMAGC	21	RF time constant of AM front-end AGC
VREFFMMIX	22	reference voltage for FM RF mixer
FMMIXIN1	23	FM mixer input 1
RFGND	24	RF ground
i.c.	25	internally connected; connect to ground
FMMIXIN2	26	FM mixer input 2
WBFLAG	27	buffered weather band flag output
IFMAGC	28	PIN diode drive current output of FM front-end AGC
AGCBUF	29	monitor current output of FM and AM front-end AGC
DAAOUT	30	output of Digital Auto Alignment (DAA) circuit for antenna tank circuit
KAGCADJ	31	adjustment for FM keyed AGC function; leave open-circuit
TFMAGC	32	time constant of FM front-end AGC
KAGC	33	level input for FM keyed AGC function from IF DSP
DAATD	34	temperature compensation diode of DAA circuit for antenna tank circuit
DAAIN	35	input of DAA circuit for antenna tank circuit
VTUNE	36	VCO tuning voltage
CPOUT	37	charge pump output
V_{DDA3}	38	analog supply voltage 3 (8.5 V) for tuning PLL
DGND	39	digital ground
V_{DDD}	40	digital supply voltage (5 V)
VCOGND	41	VCO ground
OSCFDB	42	VCO feedback input
OSCTNK	43	VCO tank circuit
V_{DDA4}	44	analog supply voltage 4 (8.5 V) for VCO
ADDRSEL	45	hardware address select for I^2C-bus
BUSENABLE	46	enable input for I^2C-bus
AFSAMPLE	47	AF sample flag output for IF DSP
AFHOLD	48	AF hold flag output for IF DSP
SDA	49	I^2C-bus Serial Data (SDA) line input and output

Table 3: Pin description *...continued*

Symbol	Pin	Description
SCL	50	I^2C-bus Serial Clock (SCL) line input
IFAGCLSB	51	Least Significant Bit (LSB) input for IF AGC amplifier gain setting from IF DSP
IFAGCMSB	52	Most Significant Bit (MSB) input for IF AGC amplifier gain setting from IF DSP
SWPORT2	53	software programmable port 2
V_{DDA5}	54	analog supply voltage 5 (8.5 V) for on-chip power supply
GND	55	ground
V_{DDA6}	56	analog supply voltage 6 (5 V) for on-chip power supply
XTAL1	57	crystal oscillator 1
XTAL2	58	crystal oscillator 2
XTALGND	59	crystal oscillator ground
VDAC	60	Digital-to-Analog Converter (DAC) output voltage for crystal oscillator frequency pulling
IREF	61	reference current for power supply
i.c.	62	internally connected; connect to ground
IFOUT1	63	IF AGC amplifier output 1
IFOUT2	64	IF AGC amplifier output 2

7. Functional description

7.1 FM in-phase/quadrature-phase mixer

The FM quadrature mixer converts FM RF (64 MHz to 108 MHz and 162.4 MHz to 162.55 MHz) to an IF of 10.7 MHz. It provides inherent image rejection and high dynamic range. The image rejection can be switched from low injection Local Oscillator (LO) to high injection LO via the I^2C-bus. The mixer conversion gain can be increased by 6 dB via the I^2C-bus. In this case the threshold of the FM keyed AGC has to be lowered by 6 dB to prevent the mixer from being overloaded.

7.2 Buffer output for weather band flag

The buffer output (pin WBFLAG) is HIGH for weather band mode.

7.3 VCO

The varactor tuned LC oscillator provides the local oscillator signal for both FM and AM mixers. It has a frequency range from 159.9 MHz to 248.2 MHz.

7.4 Crystal oscillator

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Timing signal for the Radio Data System (RDS) update algorithm.

7.5 PLL

The fast synthesizer PLL tuning system with local control is used for inaudible AF updating, combining fast PLL jumps with low reference frequency breakthrough.

It is capable of tuning the following FM and AM bands:

- US FM and US IBOC DAB from 87.9 MHz to 107.9 MHz
- US weather FM from 162.4 MHz to 162.55 MHz
- Europe FM from 87.5 MHz to 108 MHz
- Japan FM from 76 MHz to 91 MHz
- East Europe FM from 64 MHz to 74 MHz
- LW from 144 kHz to 288 kHz
- MW from 522 kHz to 1710 kHz (US AM band)
- SW from 5.73 MHz to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

7.6 DAA

To reduce the number of manual alignments in production, the following I^{2}C-bus controlled Digital Auto Alignment (DAA) functions are included:

- FM RF DAA
  - 7-bit DAC to control the conversion of the VCO tuning voltage to FM antenna tank tuning voltage
  - For cost reduction the diode at pin DAATD can be omitted from this application. In this case, pin DAATD must be connected to ground, which reduces the available alignment range (see Figure 9)
- Crystal frequency and general purpose DAA
  - 5-bit DAC for adjustment of the crystal oscillator frequency to align the actual IF frequency to the center frequency of IF selectivity inside the IF DSP. If the IF DSP can be aligned to the actual IF frequency, this DAA output can be used as general purpose DAC. Figure 3 shows the application of the crystal oscillator with frequency pulling.

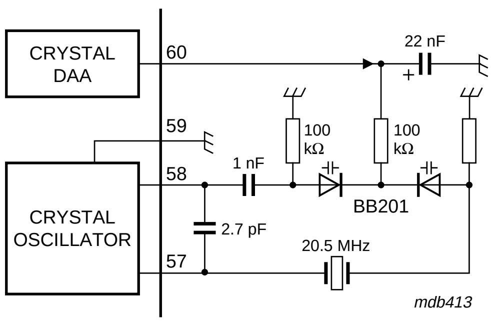


Fig 3. Crystal oscillator with frequency pulling

7.7 FM keyed AGC

The AGC detects at the FM mixer input and the IF AGC amplifier input. The AGC threshold for the FM mixer input is programmable via the I²C-bus. When the threshold is exceeded, the AGC sources a current to an external PIN diode circuit, keeping the RF signal level at the FM mixer input constant.

The keyed function shifts the threshold of the AGC if the in-band signal is small. This reduces desensitization by other strong transmitters. The amount of threshold shift is limited to 10 dB. The keyed function can be activated via the I²C-bus and is controlled by in-band level information delivered from IF DSP via pin KAGC.

The AGC can be activated via the I²C-bus to source a fixed current as a local function for search tuning. In AM mode the AGC can be activated to source a constant 10 mA current into the FM PIN diode.

7.8 AM mixer

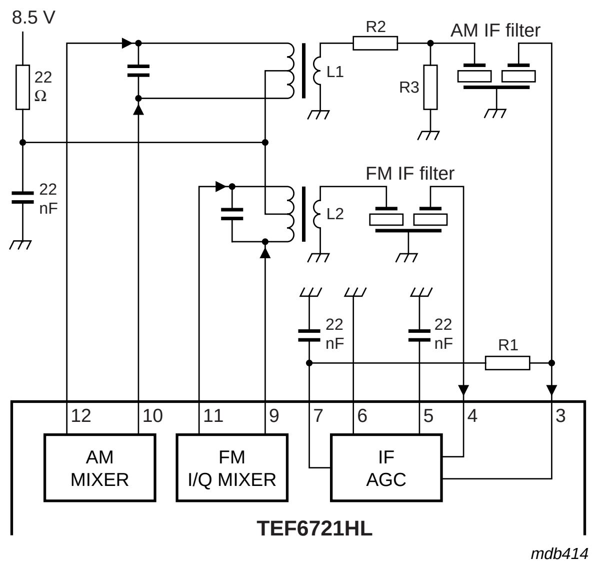


Fig 4. Separate IF paths for AM and FM mode

The AM mixer has a high dynamic range and converts AM RF to an IF frequency of 10.7 MHz.

The outputs of the AM and FM mixers can be separated to allow the use of different IF filters for AM and FM modes. Figure 4 shows this optional application. By adding the resistor R1 between pins AMIFIN and IFAGCBIAS the input impedance of the IF AGC amplifier is matched to the AM IF filter output impedance.

The input impedance of the AM IF filter is matched to 330 Ω with R2 and R3.

7.9 AM RF AGC

The AM wideband AGC in front of the AM mixer is realized first by a cascoded NPN transistor, which controls the transconductance of the RF amplifier JFET with 10 dB of AGC range. Second, an AM PIN diode stage with 30 dB of AGC range is available. The minimum JFET drain source voltage is controlled by a Direct Current (DC) feedback loop (pin VAMCASFB) in order to limit the cascode AGC range to 10 dB. If the cascode AGC is not required, a simple RF AGC loop is possible by using only a PIN diode. In some conditions, noise behavior will increase. In this case pins VAMCAS and VAMCASFB have to be left open-circuit. In FM mode, the cascode switches off the JFET bias current to reduce the total power consumption.

The AGC detection points for AM RF AGC are at the AM mixer input (threshold programmable via the I^2C-bus) and the AM and FM IF AGC amplifier input (fixed threshold).

In FM mode the AM AGC can be activated via the I^2C-bus to sink a constant current of 1 mA from the PIN diode.

7.10 FM/AM RF AGC buffer

This output current can be used to reduce the gain of active antennas before start of RF AGC.

The output (open-collector) sinks a current which in AM mode is proportional to the voltage at pin TRFAMAGC and in FM mode proportional to the RF level detector voltage (pin TFMAGC) inside the FM AGC.

8. I^2C-bus protocol

8.1 I^2C-bus specification

SDA and SCL HIGH and LOW levels are specified according to a 3.3 V I^2C-bus. The bus pins tolerate also thresholds of a 5 V bus.

The standard I^2C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2h: 1100001 R/$\overline{W}$
- 2nd IC address C0h: 1100000 R/$\overline{W}$
- 3rd IC address C4h: 1100010 R/$\overline{W}$.

Structure of the I^2C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

The second I^2C-bus address can be selected by connecting pin ADDRSEL via a 120 kΩ resistor to ground. The third I^2C-bus address can be selected by connecting pin ADDRSEL via a 33 kΩ resistor to ground.

The maximum bit rate for this device is 100 kbit/s.

The I^2C-bus interface is extended with an enable input (pin BUSENABLE). If pin BUSENABLE is HIGH the communication with the device is active; if pin BUSENABLE is LOW the signals on the I^2C-bus are ignored so that higher bit rates (> 100 kbit/s) can be used to communicate with other devices on the same I^2C-bus. The enable signal must not change while bus communication takes place.

No default settings at power-on reset. I^2C-bus transmission is required to program the IC.

8.1.1 Data transfer

Data sequence: address, byte 0, byte 1, byte 2, byte 3, byte 4 and byte 5.

The data transfer has to be in this order. The LSB of the address being logic 0 indicates a write operation.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

8.1.2 Frequency setting

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit PRESET to logic 1. To select a frequency, two I^2C-bus transmissions are necessary:

- First: bit PRESET = 1
- Second: bit PRESET = 0.

8.1.3 Restriction of the I^2C-bus characteristic

At –40 °C the start of the acknowledge bit after transmitting the slave address exceeds the general requirement of $t_{HD;DAT} < 3.45$ µs. The start of acknowledge is $t_{ST;ACK} < 4.1$ µs over the full temperature range from –40 °C to +85 °C. This will not influence the overall system performance, because the required set-up time $t_{SU;DAT} > 250$ ns is fulfilled at any condition.

8.2 I^2C-bus protocol

8.2.1 Data transfer mode and IC address

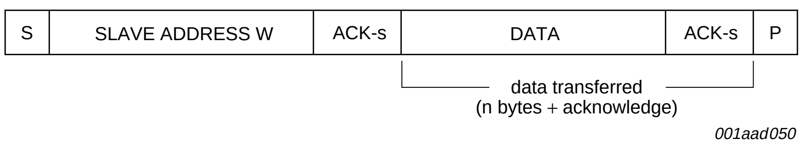


Fig 5. Write mode

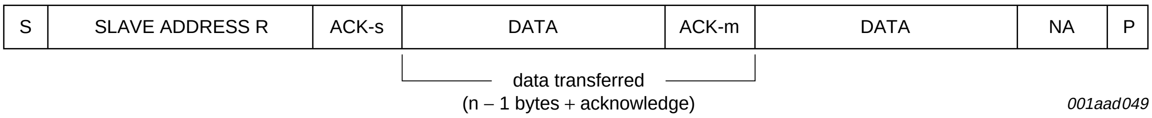


Fig 6. Read mode

Table 4: Description of I²C-bus format

Code	Description
S	START condition
Slave address W	see Table 5
Slave address R	see Table 5
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge generated by the master
Data	data byte
P	STOP condition

Table 5: IC address byte

Address	IC address [1]							Mode [2]
1	1	1	0	0	0	0	1	$R/\overline{W}$
2	1	1	0	0	0	0	0	$R/\overline{W}$
3	1	1	0	0	0	1	0	$R/\overline{W}$

[1] Pin ADDRSEL left open-circuit activates first IC address; R_{ext} = 120 kΩ at pin ADDRSEL to ground activates second IC address; R_{ext} = 33 kΩ at pin ADDRSEL to ground activates third IC address.

[2] Read or write bit:

0 = write operation to TEF6721HL

1 = read operation from TEF6721HL.

8.2.2 Write mode: data byte 0

Table 6: Format of data byte 0

7	6	5	4	3	2	1	0
AF	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 7: Description of data byte 0 bits

Bit	Symbol	Description
7	AF	**Alternative frequency.** If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode.
6 to 0	PLL[14:8]	**Setting of programmable counter of synthesizer PLL.** Upper byte of PLL divider word.

8.2.3 Write mode: data byte 1

Table 8: Format of data byte 1

7	6	5	4	3	2	1	0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 9: Description of data byte 1 bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	**Setting of programmable counter of synthesizer PLL.** Lower byte of PLL divider word.

8.2.4 Write mode: data byte 2

Table 10: Format of data byte 2

7	6	5	4	3	2	1	0
PRESET	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

Table 11: Description of data byte 2 bits

Bit	Symbol	Description
7	PRESET	**Preset.** If PRESET = 0, then programmable divider and antenna DAA locked. If PRESET = 1, then writing to programmable divider and antenna DAA enabled.
6 to 0	DAA[6:0]	**Setting of antenna digital auto alignment.**

8.2.5 Write mode: data byte 3

Table 12: Format of data byte 3

7	6	5	4	3	2	1	0
-	FREF2	FREF1	FREF0	-	BND1	BND0	AMFM

Table 13: Description of data byte 3 bits

Bit	Symbol	Description
7	-	This bit is not used and should be set to logic 0.
6 to 4	FREF[2:0]	**Reference frequency for synthesizer.** These 3 bits determine the reference frequency, see Table 14.
3	-	This bit is not used and should be set to logic 0.
2 and 1	BND[1:0]	**Band switch.** These 2 bits select the frequency in AM and FM mode, see Table 15 and Table 16.
0	AMFM	**AM or FM switch.** If AMFM = 0, then FM mode. If AMFM = 1, then AM mode.

Table 14: Reference frequency setting

FREF2	FREF1	FREF0	f_{ref} (kHz)
0	0	0	100
1	0	0	50
0	1	0	25
1	1	0	20
0	0	1	10
1	0	1	10
0	1	1	10
1	1	1	10

Table 15: FM band selection bits

BND1	BND0	Frequency band	VCO divider	Charge pump current
0	0	FM standard	2	130 µA + 3 mA
0	1	FM Japan	3	130 µA + 3 mA
1	0	FM East Europe	3	1 mA
1	1	FM weather	1	300 µA

Table 16: AM band selection bits [1]

BND1	BND0	Frequency band	VCO divider	Charge pump current
0	X	AM SW	10	1 mA
1	X	AM LW/MW	20	1 mA

[1] X = don't care.

8.2.6 Write mode: data byte 4

Table 17: Format of data byte 4

7	6	5	4	3	2	1	0
KAGC	AGC1	AGC0	LODX	FMINJ	-	AGCSW	MIXGAIN

Table 18: Description of data byte 4 bits

Bit	Symbol	Description
7	KAGC	**Keyed FM AGC.** If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on.
6 and 5	AGC[1:0]	**Wideband AGC.** These 2 bits set the start value of wideband AGC. For AM, see Table 19 and for FM, see Table 20.
4	LODX	**Local or distance.** If LODX = 0, then distance mode is on. If LODX = 1, then local mode is on.
3	FMINJ	**FM mixer image rejection.** If FMINJ = 0, then low injection. If FMINJ = 1, then high injection.
2	-	This bit is not used and should be set to logic 0.
1	AGCSW	**AGC switch.** If AGCSW = 0, then AM AGC in FM mode and FM AGC in AM mode is off. If AGCSW = 1, then AM AGC PIN diode drive is active in FM mode and FM AGC PIN diode drive is active in AM mode.
0	MIXGAIN	**FM mixer gain.** If MIXGAIN = 0, then the FM mixer gain is nominal. If MIXGAIN = 1, then the FM mixer gain is +6 dB.

Table 19: Setting of wideband AGC for AM (m = 0.3)

AGC1	AGC0	AM mixer input voltage (peak value) (mV)
0	0	275
0	1	375
1	0	500
1	1	625

Table 20: Setting of wideband AGC for FM

AGC1	AGC0	FM RF mixer input voltage (RMS value) (mV)
1	1	8
1	0	12
0	1	16
0	0	20

8.2.7 Write mode: data byte 5

Table 21: Format of data byte 5

7	6	5	4	3	2	1	0
SWPORT2	SWPORT1	-	DAC4	DAC3	DAC2	DAC1	DAC0

Table 22: Description of data byte 5 bits

Bit	Symbol	Description
7	SWPORT2	**Software programmable port 2.** If SWPORT2 = 0, then pin SWPORT2 is inactive (high-impedance). If SWPORT2 = 1, then pin SWPORT2 is active (pull down to ground).
6	SWPORT1	**Software programmable port 1.** If SWPORT1 = 0, then pin SWPORT1 is inactive (high-impedance). If SWPORT1 = 1, then pin SWPORT1 is active (pull down to ground).
5	-	This bit is not used and should be set to logic 0.
4 to 0	DAC[4:0]	**Setting of crystal frequency DAA.** These 5 bits determine the crystal frequency alignment output voltage.

8.2.8 Read mode: data byte 0

Table 23: Format of first data byte

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Table 24: Description of data byte 0 bits

Bit	Symbol	Description
7 to 0	ID[7:0]	**Chip ID.** These bits contain a constant value (0010 0001 = 21h) for chip identification purposes.

9. Internal circuitry

Table 25: Equivalent pin circuits

Symbol	Pin	Equivalent circuit
i.c.	1	
V_{DDA1}	2	

Table 25: Equivalent pin circuits *…continued*

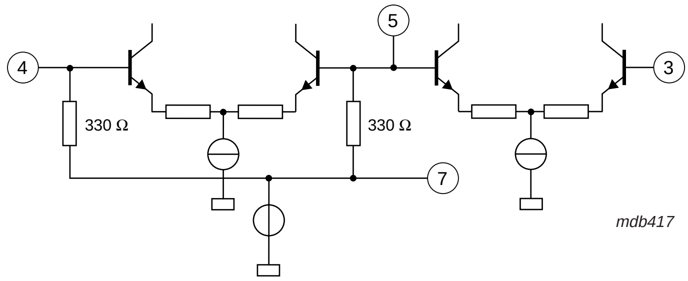
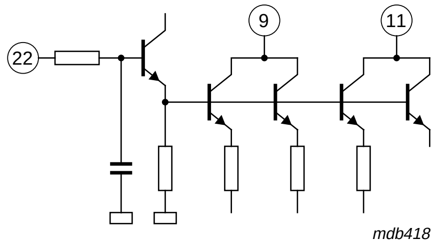
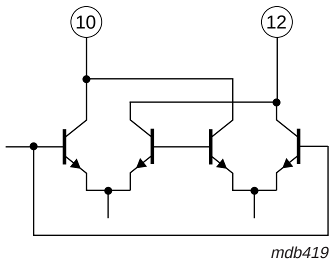
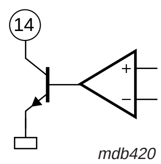
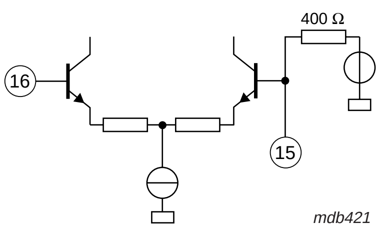
Symbol	Pin	Equivalent circuit
AMIFIN	3	
FMIFIN	4	
IFDEC	5	
IFAGCBIAS	7	
IFGND	6	
i.c.	8	
FMMIXOUT1	9	
FMMIXOUT2	11	
AMMIXOUT1	10	
AMMIXOUT2	12	
V_{DDA2}	13	
SWPORT1	14	
AMMIXDEC	15	
AMMIXIN	16	

Table 25: Equivalent pin circuits *…continued*

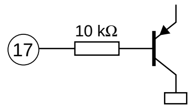
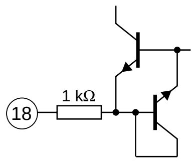
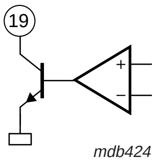
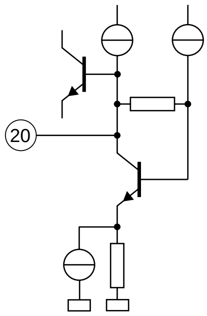
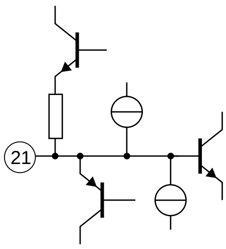
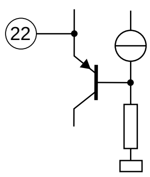
Symbol	Pin	Equivalent circuit
VAMCAS	17	 mdb422
VAMCASFB	18	 mdb423
IAMAGC	19	 mdb424
TAFAMAGC	20	 mdb425
TRFAMAGC	21	 mdb426
VREFFMMIX	22	 mdb427

Table 25: Equivalent pin circuits *…continued*

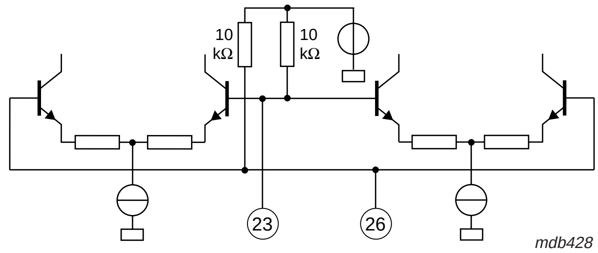
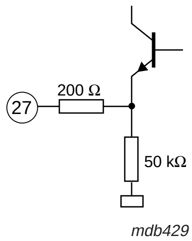
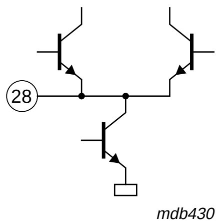
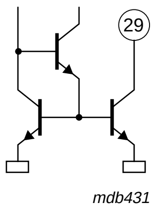
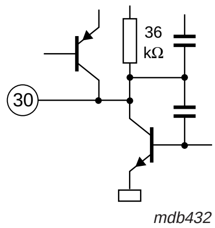
Symbol	Pin	Equivalent circuit
FMMIXIN1	23	
FMMIXIN2	26	
RFGND	24	
i.c.	25	
WBFLAG	27	
IFMAGC	28	
AGCBUF	29	
DAAOUT	30	

Table 25: Equivalent pin circuits *…continued*

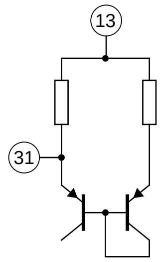
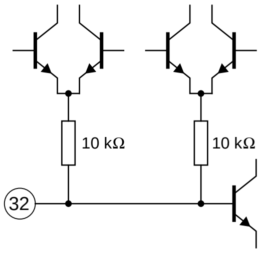
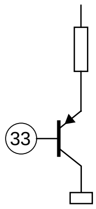
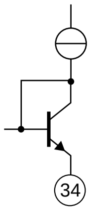
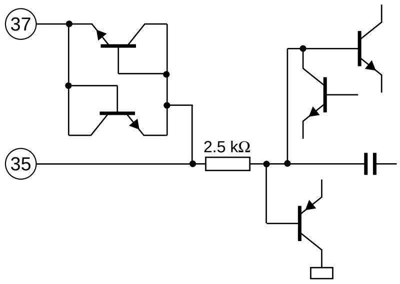
Symbol	Pin	Equivalent circuit
KAGCADJ	31	 mdb433
TFMAGC	32	 mdb434
KAGC	33	 mdb435
DAATD	34	 mdb436
DAAIN	35	 mdb437

Table 25: Equivalent pin circuits *…continued*

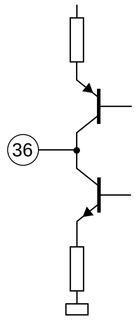
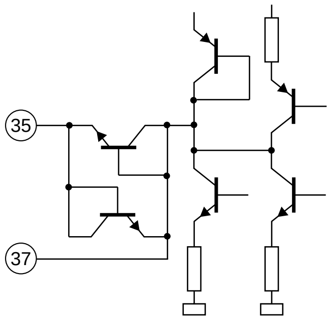
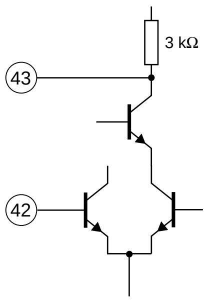
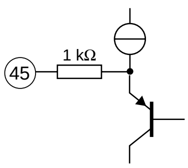
Symbol	Pin	Equivalent circuit
VTUNE	36	 *mdb438*
CPOUT	37	 *mdb439*
V_{DDA3}	38	
DGND	39	
V_{DDD}	40	
VCOGND	41	
OSCFDB	42	 *mdb440*
OSCTNK	43	
V_{DDA4}	44	
ADDRSEL	45	 *mdb441*

Table 25: Equivalent pin circuits *...continued*

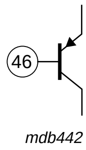
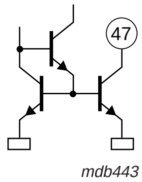
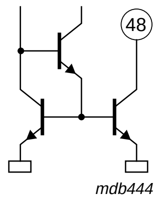
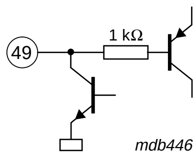
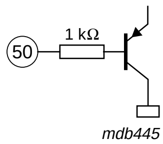
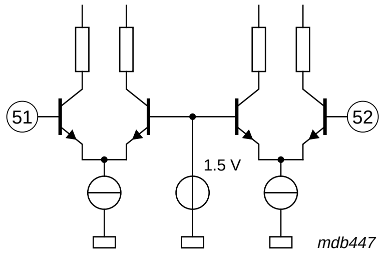
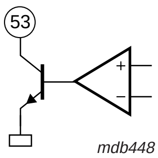
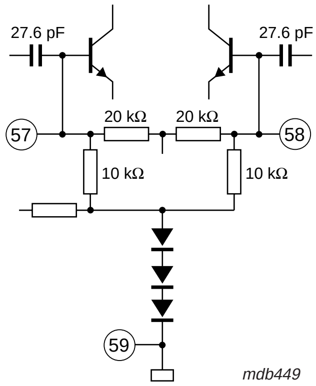
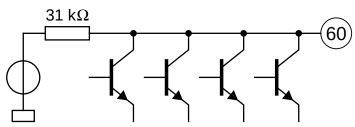
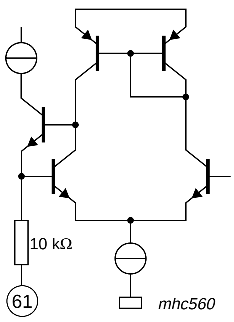
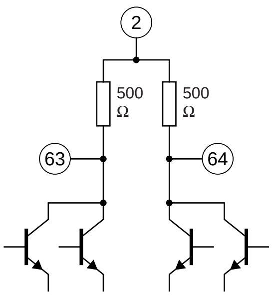
Symbol	Pin	Equivalent circuit
BUSENABLE	46	
AFSAMPLE	47	
AFHOLD	48	
SDA	49	
SCL	50	
IFAGCLSB	51	
IFAGCMSB	52	
SWPORT2	53	
V_{DDA5}	54	

Table 25: Equivalent pin circuits *…continued*

Symbol	Pin	Equivalent circuit
GND	55	
V_{DDA6}	56	
XTAL1	57	 *mdb449*
XTAL2	58	
XTALGND	59	
VDAC	60	 *mdb450*
IREF	61	 *mhc560*
i.c.	62	
IFOUT1	63	 *mdb451*
IFOUT2	64	

10. Limiting values

Table 26: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA1}	analog supply voltage 1 for IF AGC amplifier		[1]	–0.3	+10	V
V_{DDA2}	analog supply voltage 2 for FM and AM RF		[1]	–0.3	+10	V
V_{DDA3}	analog supply voltage 3 for tuning PLL		[1]	–0.3	+10	V
V_{DDA4}	analog supply voltage 4 for VCO		[1]	–0.3	+10	V
V_{DDA5}	analog supply voltage 5 for on-chip power supply		[1]	–0.3	+10	V
V_{DDA6}	analog supply voltage 6 for on-chip power supply			–0.3	+6.5	V
V_{DDD}	digital supply voltage			–0.3	+6.5	V
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{esd}	electrostatic discharge voltage		[2]	–200	+200	V
			[3]	–2000	+2000	V

[1] To avoid damages and wrong operation it is necessary to keep all 8.5 V supply voltages at a higher level than any 5 V supply voltage. This is also necessary during power-on and power-down sequences. Precautions have to be provided in such a way that interferences can not pull down the 8.5 V supply below the 5 V supply.

[2] Machine model (R = 0 Ω, C = 200 pF).

[3] Human body model (R = 1.5 kΩ, C = 100 pF).

11. Thermal characteristics

Table 27: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	58	K/W

12. Static characteristics

Table 28: Static characteristics

$V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DD5}$ = 8.5 V; V_{DDA6} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
$V_{DDA(n)}$	analog supply voltages 1 to 5		8	8.5	9	V
V_{DDA6}	analog supply voltage 6		4.75	5	5.25	V
V_{DDD}	digital supply voltage		4.75	5	5.25	V
Supply current in FM mode						
I_{DDA1}	analog supply current 1 for AM and FM IF AGC amplifier		-	20.5	-	mA
I_{DDA2}	analog supply current 2 for RF		-	5.5	-	mA
I_{DDA3}	analog supply current 3 for tuning PLL		-	4.3	-	mA
I_{DDA4}	analog supply current 4 for VCO		5.2	6.5	7.8	mA

Table 28: Static characteristics *…continued*

$V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DD5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA5}	analog supply current 5 for on-chip power supply		-	7.8	-	mA
$I_{DDA(n)}$	sum of analog supply currents 1 to 5	Japan band	35	44	55	mA
I_{DDA6}	analog supply current 6 for on-chip power supply	Europe/US band	2.0	3.0	4.1	mA
		Japan/East Europe band	2.2	3.2	4.3	mA
I_{DDD}	digital supply current	Europe/US band	-	23	-	mA
		Japan/East Europe band	23	30	39	mA
$I_{FMMIXOUT1}$	bias current of FM mixer output 1		4.8	6	7.2	mA
$I_{FMMIXOUT2}$	bias current of FM mixer output 2		4.8	6	7.2	mA
Supply current in AM mode						
I_{DDA1}	analog supply current 1 for AM and FM IF AGC amplifier		-	19.5	-	μA
I_{DDA2}	analog supply current 2 for RF		-	2	-	mA
I_{DDA3}	analog supply current 3 for tuning PLL		1.7	2.5	3.5	mA
I_{DDA4}	analog supply current 4 for VCO		5	6.5	8	mA
I_{DDA5}	analog supply current 5 for on-chip power supply		-	7.5	-	mA
$I_{DDA(n)}$	sum of analog supply currents 1 to 5		28	38	48	mA
I_{DDA6}	analog supply current 6 for on-chip power supply		10	14	18	mA
I_{DDD}	digital supply current		17	23	30	mA
$I_{AMMIXOUT1}$	bias current of AM mixer output 1		4.8	6	7.2	mA
$I_{AMMIXOUT2}$	bias current of AM mixer output 2		4.8	6	7.2	mA
On-chip power supply reference current generator: pin IREF						
$V_{o(ref)}$	output reference voltage		4	4.25	4.5	V
R_o	output resistance		-	10	-	kΩ
$I_{o(source)(max)}$	maximum output source current		–100	-	+100	nA

13. Dynamic characteristics

Table 29: Dynamic characteristics

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25\,°C$; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage controlled oscillator						
f_{osc}	oscillator frequency		159.9	-	248.2	MHz
C/N	carrier-to-noise ratio	$f_{osc} = 200$ MHz; $\Delta f = 10$ kHz; B = 1 Hz	-	97	-	dBc
RR	ripple rejection $\frac{\Delta f_{osc}}{f_{osc}}$	$f_{ripple} = 100$ Hz; $V_{DDA4(ripple)} = 100$ mV; $f_{osc} = 200$ MHz	92	99	-	dB
Crystal oscillator						
f_{xtal}	crystal frequency		-	20.5	-	MHz
C/N	carrier-to-noise ratio	$f_{xtal} = 20.5$ MHz; $\Delta f = 10$ kHz	-	112	-	$\frac{dBc}{\sqrt{Hz}}$
Circuit inputs: pins XTAL1, XTAL2 and XTALGND [1]						
$V_{o(xtal)}$	crystal oscillator output voltage	single tuner or master tuner; measured between pins XTAL1 and XTALGND or between pins XTAL2 and XTALGND; see Figure 10	100	-	250	mV
V_{XTAL1}, V_{XTAL2}	DC bias voltage		1.7	2.1	2.5	V
R_i	real part of input impedance	$V_{XTAL1} - V_{XTAL2} = 1$ mV	–250	-	-	Ω
C_i	input capacitance		8	10	12	pF
$V_{i(xtal)}$	crystal oscillator input voltage	slave tuner; minimum required input voltage between pins XTAL1 and XTALGND or between pins XTAL2 and XTALGND; see Figure 10	-	-	50	mV
Synthesizer						
$f_{AM(ant)}$	AM input frequency	LW	0.144	-	0.288	MHz
		MW	0.522	-	1.710	MHz
		SW	5.73	-	9.99	MHz
$f_{FM(ant)}$	FM input frequency		64	-	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	-	162.55	MHz
Programmable divider						
N_{prog}	programmable divider ratio		512	-	32767	
ΔN_{step}	programmable divider step size		-	1	-	

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Charge pump: pin CPOUT						
$I_{sink(cp1)l}$	low charge pump 1 peak sink current	FM weather band mode; 0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} > f_{ref} \times N_{prog}$	-	300	-	µA
$I_{source(cp1)l}$	low charge pump 1 peak source current	FM weather band mode; 0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} < f_{ref} \times N_{prog}$	-	–300	-	µA
$I_{sink(cp1)h}$	high charge pump 1 peak sink current	0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} > f_{ref} \times N_{prog}$				
		AM mode	-	1	-	mA
		FM East Europe band	-	1	-	mA
$I_{source(cp1)h}$	high charge pump 1 peak source current	0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} < f_{ref} \times N_{prog}$				
		AM mode	-	–1	-	mA
		FM East Europe band	-	–1	-	mA
$I_{sink(cp2)}$	charge pump 2 peak sink current	FM standard or FM Japan mode; $f_{VCO} > f_{ref} \times N_{prog}$; 0.3 V < V_{CPOUT} < 7.1 V	-	130	-	µA
$I_{source(cp2)}$	charge pump 2 peak source current	FM standard or FM Japan mode; $f_{VCO} < f_{ref} \times N_{prog}$; 0.3 V < V_{CPOUT} < 7.1 V	-	–130	-	µA
Charge pump: pin VTUNE						
$I_{sink(cp3)}$	charge pump 3 peak sink current	FM standard or FM Japan mode; $f_{VCO} > f_{ref} \times N_{prog}$; 0.4 V < V_{VTUNE} < 7.6 V	-	3	-	mA
$I_{source(cp3)}$	charge pump 3 peak source current	FM standard or FM Japan mode; $f_{VCO} < f_{ref} \times N_{prog}$; 0.4 V < V_{VTUNE} < 7.6 V	-	–3	-	mA
Antenna Digital Auto Alignment (DAA)						
DAA input: pin DAAIN						
$I_{bias(cp)}$	charge pump buffer input bias current	V_{DAAIN} = 0.4 V to 8 V	–10	-	+10	nA
$V_{i(cp)}$	charge pump buffer input voltage		0	-	8.5	V
DAA output: pin DAAOUT						
$V_{o(AM)}$	DAA output voltage in AM mode	I_{DAAOUT} < 100 µA	-	-	0.3	V

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5}$ = 8.5 V; V_{DDA6} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{o(FM)}$	DAA output voltage in FM mode	V_{DAATD} = 0.45 V					
		minimum value; data byte 2 = 1000 0000 (n = 0); V_{DAAIN} = 0.5 V		-	-	0.5	V
		data byte 2 = 1010 1010 (n = 42); V_{DAAIN} = 2 V		1.2	1.4	1.6	V
		data byte 2 = 1101 0101 (n = 85); V_{DAAIN} = 2 V	[2]	2.3	2.6	2.9	V
		data byte 2 = 1000 0000 (n = 0); V_{DAAIN} = 4 V	[2]	-	0.65	-	V
		data byte 2 = 1100 0000 (n = 64); V_{DAAIN} = 4 V		3.8	4	4.2	V
		maximum value; data byte 2 = 1111 1111 (n = 127); V_{DAAIN} = 4.7 V		8	-	8.5	V
$V_{o(n)}$	DAA output noise voltage	data byte 2 = 1100 0000 (n = 64); FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; B = 300 Hz to 22 kHz		-	30	100	µV
$\Delta V_{o(T)}$	DAA output voltage variation with temperature	T_{amb} = –40 °C to +85 °C; data byte 2 = 1100 0000 (n = 64)		–8	-	+8	mV
$\Delta V_{o(step)}$	DAA step accuracy	FM mode; n = 0 to 127; V_{DAAOUT} = 0.5 V to 8 V; V_{DAAIN} = 2 V; V_{DAATD} = 0.45 V	[3]	$0.5V_{LSB}$	V_{LSB}	$1.5V_{LSB}$	mV
$\Delta V_{o(sink)}$	DAA output voltage variation caused by sink current	V_{DAAIN} = 4 V; I_{DAAOUT} = 50 µA	[3]	$-V_{LSB}$	-	$+V_{LSB}$	mV
$\Delta V_{o(source)}$	DAA output voltage variation caused by source current	V_{DAAIN} = 4 V; I_{DAAOUT} = –50 µA	[3]	$-V_{LSB}$	-	$+V_{LSB}$	mV
t_{st}	DAA output settling time	V_{DAAOUT} = 0.2 V to 8.25 V; C_L = 270 pF		-	20	30	µs
RR	ripple rejection $\frac{V_{DAAOUT}}{V_{DDA3}}$	data byte 2 = 1010 1011 (n = 43); FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; f_{ripple} = 100 Hz; $V_{DDA3(ripple)}$ = 100 mV		-	65	-	dB
C_L	DAA output load capacitance			-	-	270	pF
DAA temperature compensation: pin DAATD							
I_{source}	compensation diode source current	V_{DAATD} = 0.2 V to 1.2 V		–50	–40	–30	µA

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TC_{source}	temperature coefficient of compensation diode source current	V_{DAATD} = 0.2 V to 1.2 V; T_{amb} = –40 °C to +85 °C	–300	-	+300	$\frac{10^{-6}}{K}$
I^2C-bus address select: pin ADDRSEL						
R_L	load resistance to ground	1st I^2C-bus address	1	-	-	MΩ
		2nd I^2C-bus address	108	120	132	kΩ
		3rd I^2C-bus address	29.7	33	36.3	kΩ
I^2C-bus enable: pin BUSENABLE						
V_{IL}	LOW-level input voltage		–0.3	-	+1	V
V_{IH}	HIGH-level input voltage		2	-	V_{DDD} + 0.3	V
Software programmable ports: pins SWPORT1 and SWPORT2						
$I_{sink(max)}$	maximum sink current	bit SWPORT1 = 1	1	-	1.6	mA
		bit SWPORT2 = 1	1	-	1.6	mA
Weather band flag: pin WBFLAG						
$I_{source(max)}$	maximum source current	R = 560 Ω	-	–5	-	mA
$R_{i(shunt)}$	internal shunt resistance to ground		-	50	-	kΩ
$V_{o(FM)(max)}$	maximum output voltage for FM mode	measured with respect to pin RFGND	0	-	0.2	V
$V_{o(WB)}$	output voltage for weather band mode	measured with respect to pin RFGND	4	-	5	V
AM signal channel						
AM RF AGC: pins AMMIXIN and AMMIXDEC						
$V_{i(RF)(p)}$	RF input voltage for wideband AGC start level (peak value)	m = 0.3; f_{AF} = 1 kHz				
		AGC[1:0] = 00	-	275	-	mV
		AGC[1:0] = 01	-	375	-	mV
		AGC[1:0] = 10	-	500	-	mV
		AGC[1:0] = 11	-	625	-	mV
AM RF AGC IF stage: pins AMIFIN and IFDEC						
$V_{i(IF)}$	IF input voltage	AGC start level				
		m = 0	42	60	85	mV
		m = 0.8	35	50	71	mV
AM RF AGC PIN diode drive: pin IAMAGC						
$I_{sink(max)}$	maximum AGC sink current	V_{IAMAGC} = 2.8 V	11	15	19	mA
I_{sink}	AGC sink current	FM mode; AGCSW = 1	0.8	-	-	mA
R_o	output resistance	I_{IAMAGC} = 1 µA	0.5	-	-	MΩ
C_o	output capacitance		-	5	7	pF
AM RF AGC cascode stage: pin VAMCAS						
V_{cas}	cascode voltage	$V_{AMMIXIN-AMMIXDEC}$ below threshold; maximum gain	-	5	-	V

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{cas}	cascode transistor base current capability		100	-	-	µA
$I_{cas(off)}$	AM cascode off current	FM mode	-	-	100	nA
AM RF AGC cascode stage: pin VAMCASFB						
$V_{cas(FB)}$	cascode voltage	$V_{AMMIXIN-AMMIXDEC}$ above threshold; minimum gain	-	0.26	-	V
$I_{cas(FB)}$	cascode feedback sense current		0	-	1	µA
AM RF AGC transconductance buffer: pin AGCBUF [4]						
$g_{m(buf)}$	buffer transconductance $\frac{\Delta I_{AGCBUF}}{\Delta V_{TRFAMAGC}}$	AM mode; $\Delta V_{TRFAMAGC}$ = 50 mV to 0.4 V	0.85	1.1	1.35	mS
$I_{sink(max)}$	maximum sink current	AM mode; open-collector; $\Delta V_{TRFAMAGC}$ = 0.8 V	450	500	560	µA
$I_{source(max)}$	maximum source current	AM mode; $\Delta V_{TRFAMAGC}$ < 50 mV	-	-	−30	µA
$V_{o(n)}$	buffer output noise voltage	AM mode; $V_{DDA2} - V_{AGCBUF}$ = 1 V (voltage across external pull-up resistor); B = 400 Hz to 20 kHz	-	10	15	µV
AM mixer (IF = 10.7 MHz)						
Mixer inputs: pins AMMIXIN and AMMIXDEC						
R_i	input resistance		15	25	40	kΩ
C_i	input capacitance		2.5	5	7.5	pF
V_I	DC input voltage		2.3	2.7	3.1	V
$V_{i(max)}$	maximum input voltage	1 dB compression point of AM mixer output; m = 0	500	-	-	mV
Mixer outputs: pins AMMIXOUT1 and AMMIXOUT2						
R_o	output resistance		100	-	-	kΩ
C_o	output capacitance		-	4	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		12	15	-	V
I_{bias}	mixer bias current	AM mode	4.8	6	7.2	mA
Mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{IF}}{V_{RF}}$		1.9	2.6	3.4	$\frac{mA}{V}$

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5}$ = 8.5 V; V_{DDA6} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		-	-9×10^{-4}	-	K^{-1}
IP3	3rd-order input intercept point	R_L = 2.6 kΩ (AC load between output pins); Δf = 300 kHz	135	138	-	dBμV
IP2	2nd-order input intercept point	R_L = 2.6 kΩ (AC load between output pins)	-	170	-	dBμV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 750 Ω; R_L = 2.6 kΩ (AC load between output pins)	-	5.8	8	$\frac{nV}{\sqrt{Hz}}$
F	noise figure of AM mixer		-	4.5	7.1	dB
FM signal channel						
FM RF AGC (FM distance mode; LODX = 0)						
RF input: pins FMMIXIN1 and FMMIXIN2; KAGC = 0						
$V_{i(RF)}$	RF input voltage for start of wideband AGC	AGC[1:0] = 11	-	8	-	mV
		AGC[1:0] = 10	-	12	-	mV
		AGC[1:0] = 01	-	16	-	mV
		AGC[1:0] = 00	-	20	-	mV
IF input: pins FMIFIN and IFDEC						
$V_{i(IF)}$	IF input voltage for start of wideband AGC		-	27.2	-	mV
FM RF AGC time constant: pin TFMAGC						
R_{source}	source resistance		4	5	6	kΩ
$V_{O(ref)}$	DC output reference voltage	AGC[1:0] = 00; KAGC = 0; $V_{FMMIXIN1-FMMIXIN2}$ = 0 V	3.9	4.4	4.9	V
FM RF AGC PIN diode drive output: pin IFMAGC						
$I_{sink(max)}$	maximum AGC sink current	V_{IFMAGC} = 2.5 V; $V_{TFMAGC} = V_{O(ref)}$ − 0.5 V; AGC[1:0] = 00; KAGC = 0	8	11.5	15	mA
$I_{source(max)}$	maximum AGC source current	V_{IFMAGC} = 2.5 V; $V_{TFMAGC} = V_{O(ref)}$ + 0.5 V; AGC[1:0] = 00; KAGC = 0	−15	−11.5	−8	mA
$I_{source(AGC)}$	AGC source current	AM mode; AGCSW = 1	−15	−11.5	−8	mA
		V_{IFMAGC} = 2.5 V; LODX = 1	−0.65	−0.5	−0.35	mA
FM keyed AGC: pin KAGC						
V_{th}	threshold voltage for narrow-band AGC	KAGC = 1; $V_{TFMAGC} = V_{O(ref)}$ + 0.3 V	0.5	0.95	1.4	V
FM RF AGC transconductance buffer: pin AGCBUF						
$g_{m(buf)}$	buffer transconductance	FM mode; $V_{TFMAGC} = V_{O(ref)}$ to $V_{O(ref)}$ + 80 mV	3.2	5.0	6.4	mS

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5}$ = 8.5 V; V_{DDA6} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{sink(max)}$	maximum sink current	FM mode; open-collector; $V_{TFMAGC} = V_{O(ref)}$ + 0.15 V	450	500	560	µA
$I_{source(max)}$	maximum source current	FM mode; $V_{TFMAGC} = V_{O(ref)}$	-	-	–30	µA
$V_{o(n)}$	buffer output noise voltage	FM mode; $V_{VDDA2\text{-}AGCBUF}$ = 1 V (voltage across external pull-up resistor); B = 400 Hz to 20 kHz	-	10	15	µV
FM RF mixer						
Reference voltage: pin VREFFMMIX						
V_{ref}	reference voltage	FM mode	6.6	7.3	8	V
		AM mode	2.7	3.1	3.4	V
Inputs: pins FMMIXIN1 and FMMIXIN2						
R_i	input resistance	MIXGAIN = 0	-	3.5	-	kΩ
		MIXGAIN = 1	-	1.8	-	kΩ
C_i	input capacitance		-	5	7	pF
V_{BIAS}	DC bias voltage	FM mode	2.2	2.7	3.2	V
$V_{i(RF)(p)}$	RF input voltage (peak value)	1 dB compression point of FM mixer output				
		MIXGAIN = 0	70	100	-	mV
		MIXGAIN = 1	35	50	-	mV
Outputs: pins FMMIXOUT1 and FMMIXOUT2						
R_o	output resistance		100	-	-	kΩ
C_o	output capacitance		2	3.5	5	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		3	-	-	V
I_{bias}	mixer bias current	FM mode	4.8	6	7.2	mA
FM mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{IF}}{V_{RF}}$	MIXGAIN = 0	8.5	12.5	18	$\frac{mA}{V}$
		MIXGAIN = 1	17	25	36	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$	MIXGAIN = 0	-	-1×10^{-3}	-	K^{-1}
F	noise figure	MIXGAIN = 0	-	3.5	4.6	dB
		MIXGAIN = 1	-	2.4	-	dB
IP3	3rd-order input intercept point	MIXGAIN = 0	113	117	-	dBµV
		MIXGAIN = 1	-	108	-	dBµV

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5}$ = 8.5 V; V_{DDA6} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IRR	image rejection ratio	FMINJ = 1 [5]				
		$f_{RFwanted}$ = 87.5 MHz; $f_{RFimage}$ = 108.9 MHz	25	30	-	dB
		data byte 3 = X010 X110; $f_{RFwanted}$ = 162.475 MHz; $f_{RFimage}$ = 183.875 MHz	22	30	-	dB
$V_{i(n)(eq)}$	equivalent input noise voltage (pin FMMIXIN1 to FMMIXIN2)	R_{gen} = 200 Ω; R_L = 2.6 kΩ				
		MIXGAIN = 0	-	2.9	3.1	$\frac{nV}{\sqrt{Hz}}$
		MIXGAIN = 1	-	2.6	-	$\frac{nV}{\sqrt{Hz}}$
$R_{gen(opt)}$	optimum generator resistance		-	200	-	Ω
IF AGC amplifier						
Outputs: pins IFOUT1 and IFOUT2						
$V_{o(max)(p)}$	maximum output voltage (peak value)		-	1.4	-	V
R_o	output resistance		-	500	-	Ω
FM mode						
Inputs: pins FMIFIN and IFDEC						
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		-	5	7	pF
G	gain	$V_{IFAGCMSB}$ = 0.2 V; $V_{IFAGCLSB}$ = 0.2 V; C_L = 0.5 pF	-	37.3	-	dB
		$V_{IFAGCMSB}$ = 0.2 V; $V_{IFAGCLSB}$ = 2.8 V; C_L = 0.5 pF	-	31.3	-	dB
		$V_{IFAGCMSB}$ = 2.8 V; $V_{IFAGCLSB}$ = 2.8 V; C_L = 0.5 pF	-	25.3	-	dB
		$V_{IFAGCMSB}$ = 2.8 V; $V_{IFAGCLSB}$ = 0.2 V; C_L = 0.5 pF	-	19.3	-	dB
F	noise figure	R_{gen} = 330 Ω	-	8.5	-	dB
IP3	3rd-order input intercept point		-	117	-	dBμV

Table 29: Dynamic characteristics *…continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF AGC amplifier output voltage				
		$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 0.2$ V	40	-	-	mV
		$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 2.8$ V	70	-	-	mV
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 2.8$ V	134	-	-	mV
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 0.2$ V	60	-	-	mV
AM mode						
Inputs: pins AMIFIN and IFDEC						
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		-	5	7	pF
G	gain	$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 0.2$ V; $C_L = 0.5$ pF	-	27.4	-	dB
		$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 2.8$ V; $C_L = 0.5$ pF	-	21.4	-	dB
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 2.8$ V; $C_L = 0.5$ pF	-	15.4	-	dB
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 0.2$ V; $C_L = 0.5$ pF	-	9.4	-	dB
F	noise figure	$R_{gen} = 330$ Ω	-	14.6	-	dB
IP3	3rd-order input intercept point	$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 0.2$ V	-	127	-	dBμV
		$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 2.8$ V	-	132	-	dBμV
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 2.8$ V	-	135	-	dBμV
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 0.2$ V	-	136	-	dBμV

Table 29: Dynamic characteristics *...continued*

$V_{FMMIXOUT1} = V_{AMMIXOUT1} = V_{FMMIXOUT2} = V_{AMMIXOUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA5} = 8.5$ V; $V_{DDA6} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 9; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF AGC amplifier output voltage				
		$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 0.2$ V	120	-	-	mV
		$V_{IFAGCMSB} = 0.2$ V; $V_{IFAGCLSB} = 2.8$ V	220	-	-	mV
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 2.8$ V	440	-	-	mV
		$V_{IFAGCMSB} = 2.8$ V; $V_{IFAGCLSB} = 0.2$ V	600	-	-	mV
Crystal frequency Digital Auto Alignment (DAA)						
Output: pin VDAC						
$V_{o(max)}$	maximum output voltage	data byte 5 = XXX0 0000 (n = 0)	7.4	-	-	V
$V_{o(min)}$	minimum output voltage	data byte 5 = XXX1 1111 (n = 31)	-	-	1.7	V
$\Delta V_{o(step)}$	DAA step accuracy	n = 0 to 31	100	200	300	mV
$V_{o(n)}$	DAA output noise voltage	B = 300 Hz to 22 kHz	-	100	130	µV

[1] Measured between pins XTAL1 and XTAL2.

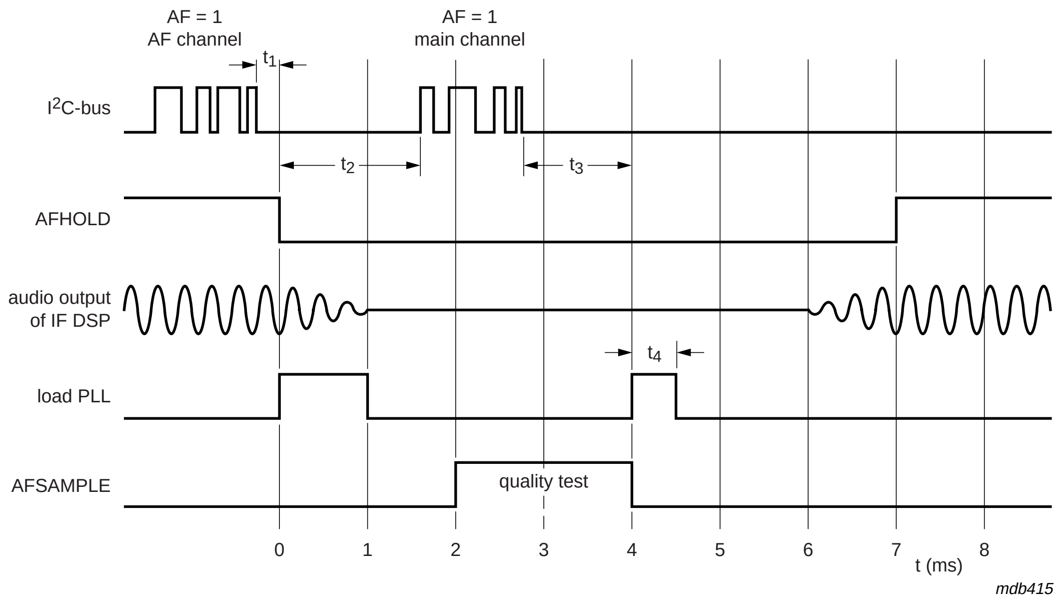
[2] DAA conversion gain formula: $V_{DAAOUT} = \left[2 \times \left(0.75 \times \frac{n}{128} + 0.125\right) \times (V_{DAAIN} + V_{DAATD})\right] - V_{DAATD}$; where n = 0 to 127.

[3] $V_{LSB} = V_{DAAOUT(n+1)} - V_{DAAOUT(n)}$

[4] The AM AGC transconductance buffer delivers a sink current which is proportional to the voltage change at pin TRFAMAGC.

$$\Delta V_{TRFAMAGC} = V_{TRFAMAGC} - V_{TRFAMAGC}\Big|_{(V_{AMMIXIN} - V_{AMMIXDEC}) < 10\ mV}$$

[5] Image rejection ratio: $IRR = \frac{V_{(FMMIXOUT1\text{-}FMMIXOUT2)wanted}}{V_{(FMMIXOUT1\text{-}FMMIXOUT2)image}}$



AFHOLD signal is used to hold the quality information for signal processing of the main channel during the alternative frequency jumps. PLL registers are loaded during load PLL = 1, but actual frequency jumps take place at the falling edge of this signal. IF counting is carried out during AFSAMPLE = 1. 10 µs after falling edge of AFSAMPLE result is valid for AF and remains valid until read by microcontroller. Quality tests in IF DSP should take place during the HIGH phase of AFSAMPLE.

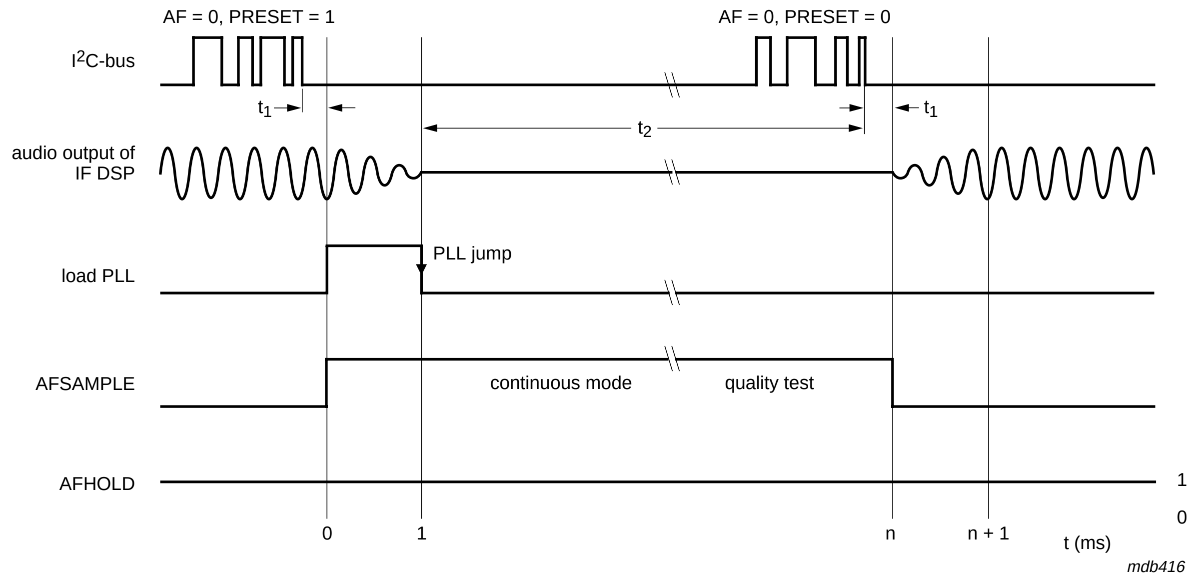
t_1 is the internal TEF6721HL clock related logic delay: 100 µs.

t_2 should be > 1.1 ms to ensure correct loading of PLL for the main channel.

t_3 should be > 0 to ensure inaudible update.

t_4 = 500 µs.

Fig 7. Inaudible AF update timing diagram



t_1 is the internal TEF6721HL clock related logic delay: 100 µs.

t_2 should be greater than the required PLL tuning time for the given band (FM: t_2 > 1 ms; AM: t_2 > 20 ms).

Fig 8. Preset mode timing diagram

14. Overall system parameters

Table 30: Overall system parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM overall system parameters (based on 15 pF/60 pF dummy aerial; m = 0.3; 2.5 kHz audio bandwidth in IF DSP; voltages in RMS value at input of dummy aerial); see Figure 9						
$V_{i(RF)(IFAGC)}$	RF input voltage for start of IF AGC	first step	-	5.5	-	mV
		second step	-	11	-	mV
		third step	-	22	-	mV
$V_{i(RF)(RFAGC)}$	RF input voltage for start of RF AGC	in-band; m = 0	-	31	-	mV
		wideband; m = 0				
		AGC[1:0] = 00	-	92	-	mV
		AGC[1:0] = 01	-	126	-	mV
		AGC[1:0] = 10	-	168	-	mV
		AGC[1:0] = 11	-	210	-	mV
α_{26dB}	sensitivity	f = 990 kHz	-	42	-	μV
IP3	3rd-order input intercept point	$\Delta f_{undesired}$ = 50 kHz	-	130	-	dBμV
		$\Delta f_{undesired}$ = 300 kHz	-	135	-	dBμV
IP2	2nd-order input intercept point		-	140	-	dBμV
FM overall system parameters (based on 75 Ω dummy aerial; Δf = 22.5 kHz; de-emphasis is 50 μs in IF DSP; voltages in RMS value at input of dummy aerial); see Figure 9						
$V_{i(RF)(IFAGC)}$	RF input voltage for start of IF AGC	first step	-	0.57	-	mV
		second step	-	1.1	-	mV
		third step	-	2.3	-	mV
$V_{i(RF)(RFAGC)}$	RF input voltage for start of wideband AGC	in-band	-	4.5	-	mV
		wideband				
		AGC[1:0] = 11	-	8	-	mV
		AGC[1:0] = 10	-	12	-	mV
		AGC[1:0] = 01	-	17	-	mV
		AGC[1:0] = 00	-	21	-	mV
α_{26dB}	sensitivity	f = 97 MHz	-	1.4	-	μV
IP3	3rd-order input intercept point	$\Delta f_{undesired}$ = 400 kHz	-	117	-	dBμV

15. Application information

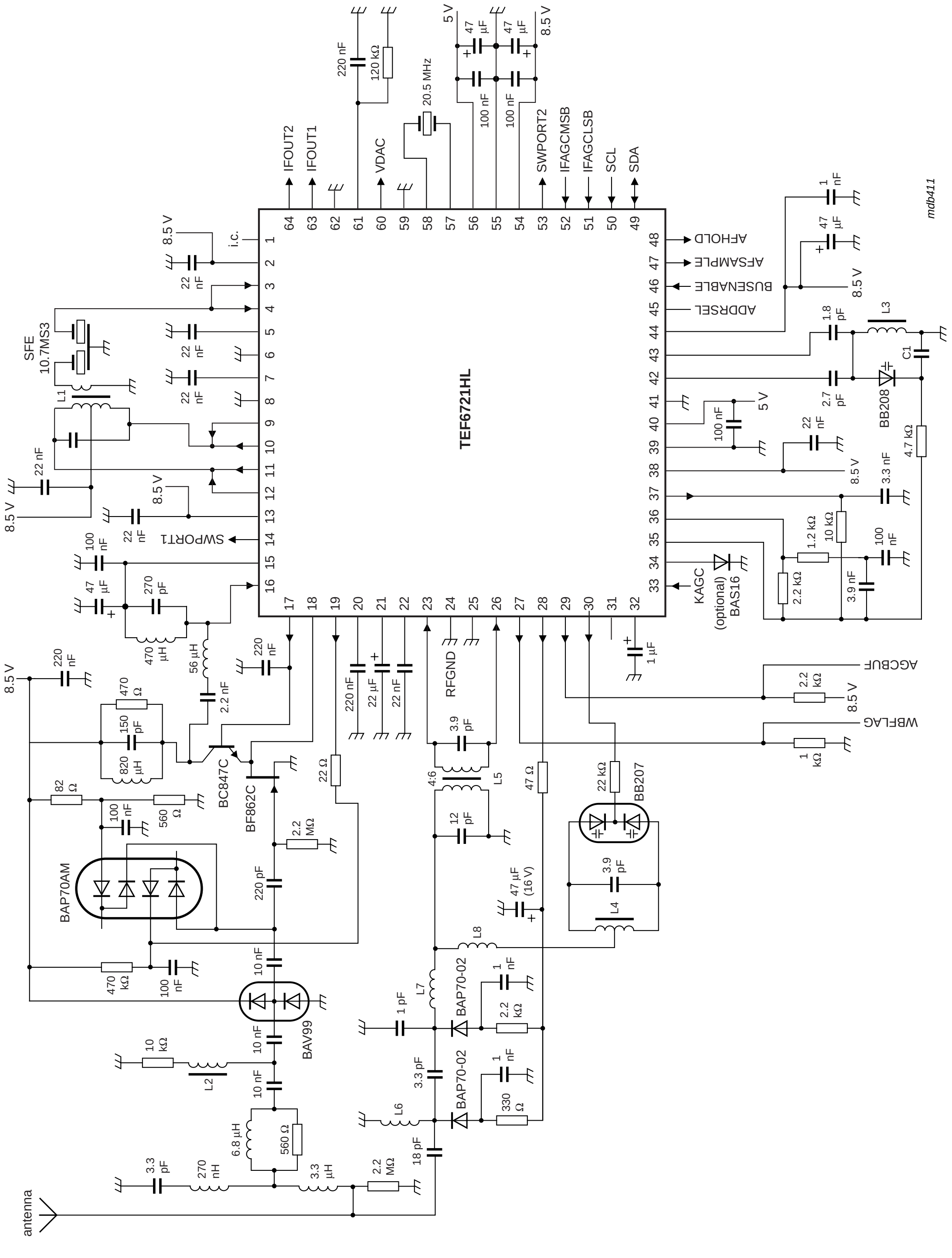


Fig 9. Application diagram of TEF6721HL

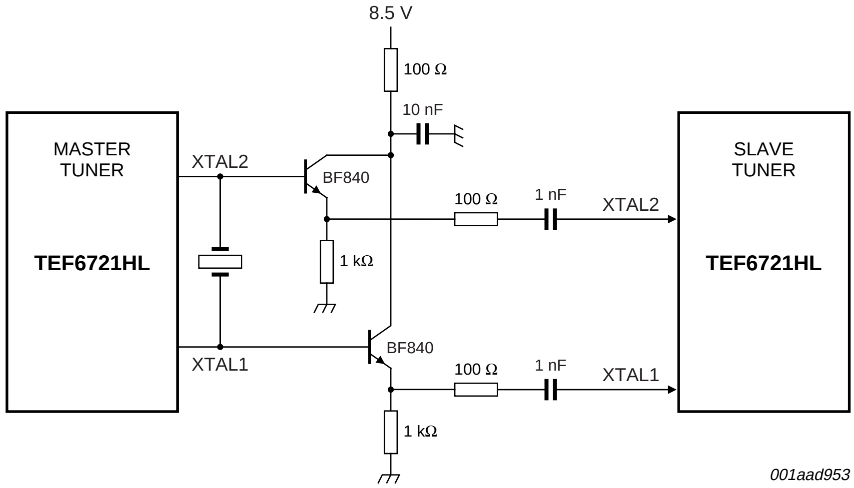


Fig 10. Driving two tuners with one crystal

Table 31: List of components

Symbol	Parameter	Type	Manufacturer
C1	capacitor for VCO tuning	270 pF; type NP0	
L1	10.7 MHz IF coil	P7 PSG P826RC 5134N=S	TOKO
L2	AM input	388BN-1211Z	TOKO
L3	oscillator coil	E543SNAS-02010	TOKO
L4	FM image rejection	611SNS-1066Y	TOKO
L5	FM input transformer	369INS-3076X	TOKO
L6	FM antenna coil	LQN1HR50; 215 nH	MURATA
L7	PIN diode bias	LQN1HR21; 500 nH	MURATA
L8	connection image reject	wire 10 mm/printed coil	
	crystal 20.5 MHz	LN-G102-587	NDK

16. Test information

Table 32: DC operating points

Symbol	Pin	Unloaded DC voltage (V) [1]					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
i.c.	1	-	5.6	-	-	5.6	-
V_{DDA1}	2	-	8.1	-	-	8.1	-
AMIFIN	3	-	2.1	-	-	2.1	-
FMIFIN	4	-	2.1	-	-	2.1	-
IFDEC	5	-	2.1	-	-	2.1	-
IFGND	6	external 0			external 0		
IFAGCBIAS	7	-	2.1	-	-	2.1	-
i.c.	8	external 0			external 0		
FMMIXOUT1	9	-	8.2	-	-	8.2	-
AMMIXOUT1	10	-	8.2	-	-	8.2	-
FMMIXOUT2	11	-	8.2	-	-	8.2	-
AMMIXOUT2	12	-	8.2	-	-	8.2	-
V_{DDA2}	13	-	8.4	-	-	8.2	-
SWPORT1	14	external biasing (open-collector)			external biasing (open-collector)		
AMMIXDEC	15	-	2.8	-	floating		
AMMIXIN	16	2.8 (external biasing)			floating		
VAMCAS	17	-	4.8	-	0	0.1	0.2
VAMCASFB	18	-	4.1	-	0	0.1	1
IAMAGC	19	6.9 (external biasing)			4.1 (external biasing)		
TAFAMAGC	20	-	0.3	-	0	0.3	0.5
TRFAMAGC	21	-	2.9	-	floating		
VREFFMMIX	22	-	3.2	-	-	7.3	-
FMMIXIN1	23	-	1.65	-	-	2.75	-
RFGND	24	external 0			external 0		
i.c.	25	external 0			external 0		
FMMIXIN2	26	-	1.65	-	-	2.75	-
WBFLAG	27	0			0	-	0.5
IFMAGC	28	4 (external biasing)			0.1 (external biasing)	-	4 (external biasing)
AGCBUF	29	8.5 (external biasing)			8.5 (external biasing)		
DAAOUT	30	-	0.2	0.3	0.2	-	8.25
KAGCADJ	31	-	8.4	-	-	8	-
TFMAGC	32	-	7.9	-	-	4.4	-
KAGC	33	0 to 3.3 (external biasing)			0 to 3.3 (external biasing)		
DAATD	34	floating		1.5	0.2	0.45	1.5
DAAIN	35	0	-	8.5	0	-	8.5
VTUNE	36	0	-	8.5	0	-	8.5

Table 32: DC operating points *...continued*

Symbol	Pin	Unloaded DC voltage (V) [1]					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
CPOUT	37	0	-	8.5	0	-	8.5
V_{DDA3}	38	-	8.44	-	-	8.4	-
DGND	39	external 0			external 0		
V_{DDD}	40	5 (external biasing)			5 (external biasing)		
VCOGND	41	external 0			external 0		
OSCFDB	42	2.2	2.8	3.4	2.2	2.8	3.4
OSCTNK	43	5	5.8	7.2	5	5.8	7.2
V_{DDA4}	44	-	8.35	-	-	8.35	-
ADDRSEL	45	-	3.7	-	-	3.7	-
BUSENABLE	46	3.3 (external biasing)			3.3 (external biasing)		
AFSAMPLE	47	open-collector			open-collector		
AFHOLD	48	open-collector			open-collector		
SDA	49	0 to 5 (external biasing)			0 to 5 (external biasing)		
SCL	50	0 to 5 (external biasing)			0 to 5 (external biasing)		
IFAGCLSB	51	0 to 3.3 (external biasing)			0 to 3.3 (external biasing)		
IFAGCMSB	52	0 to 3.3 (external biasing)			0 to 3.3 (external biasing)		
SWPORT2	53	-	-	0.3	-	-	0.3
V_{DDA5}	54	external 8.5			external 8.5		
GND	55	external 0			external 0		
V_{DDA6}	56	external 5			external 5		
XTAL1	57	1.7	2.1	2.5	1.7	2.1	2.5
XTAL2	58	1.7	2.1	2.5	1.7	2.1	2.5
XTALGND	59	external 0			external 0		
VDAC	60	2	4.8	7.8	2	4.64	7.8
IREF	61	4	4.25	4.5	4	4.25	4.5
i.c.	62	external 0			external 0		
IFOUT1	63	-	6.7	-	-	6.7	-
IFOUT2	64	-	6.7	-	-	6.7	-

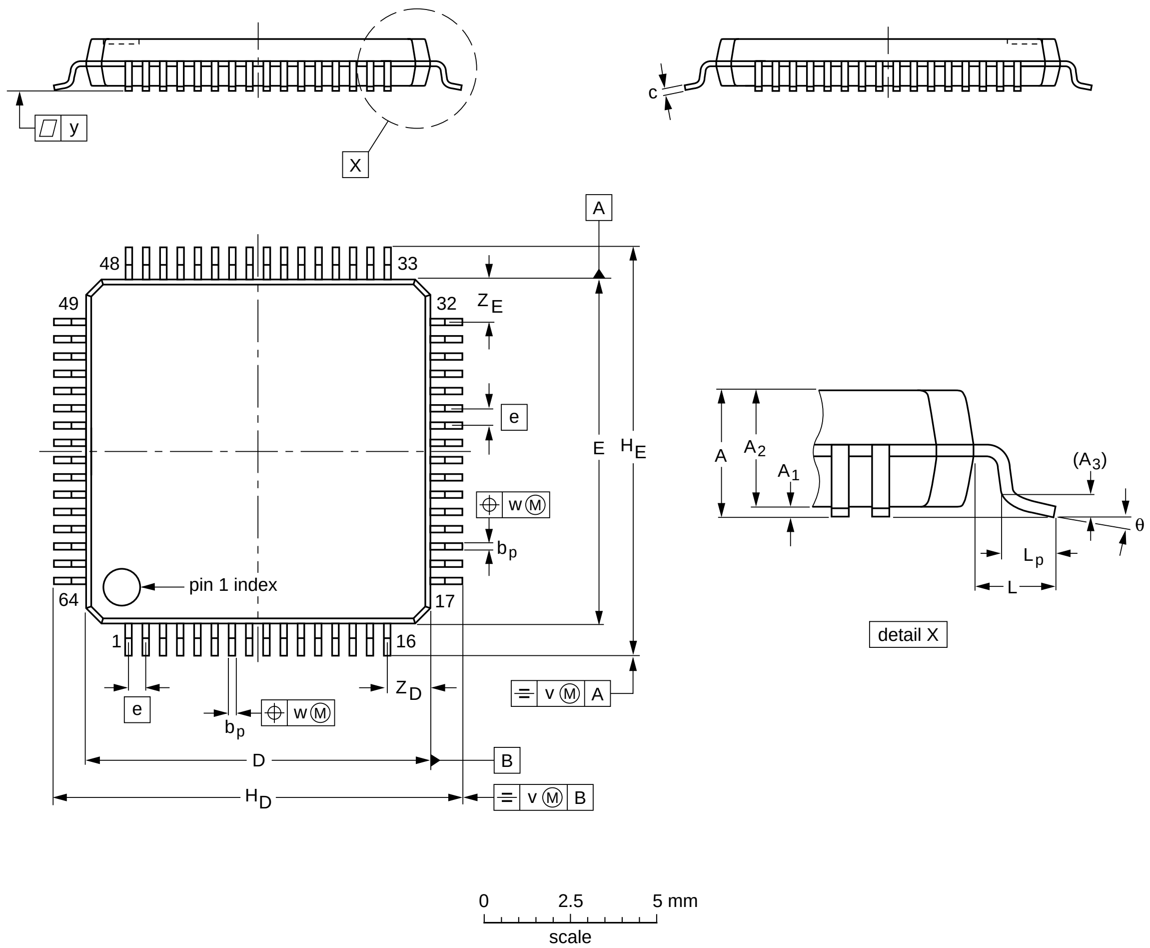
[1] After initialization via I^2C-bus using settings shown in Table 33.

Table 33: Default settings of I²C-bus transmission to 1st IC address (C2h) for AM and FM mode

Function	AM	FM
Alternative frequency	AF = 0 (no start of RDS update)	AF = 0 (no start of RDS update)
Programmable counter PLL	PLL[14:0] = 11700 (f_{RF} = 1 MHz)	PLL[14:0] = 3918 (f_{RF} = 76 MHz)
Preset	PRESET = 1 (writing to programmable divider and antenna DAA enabled)	PRESET = 1 (writing to programmable divider and antenna DAA enabled)
Setting antenna DAA	DAA[6:0] = 64	DAA[6:0] = 64
Reference frequency for synthesizer	FREF[2:0] = 110 (f_{ref} = 20 kHz; f_{VCO} = 234 MHz)	FREF[2:0] = 100 (f_{ref} = 50 kHz; f_{VCO} = 195.9 MHz)
Band select	BND[1:0] = 10; AMFM = 1 (VCO divider = 20; I_{cp} = 1 mA)	BND[1:0] = 01; AMFM = 0 (VCO divider = 3; I_{cp} = 130 µA + 3 mA)
Keyed FM AGC	KAGC = 0 (off)	KAGC = 1 (on)
Wideband AGC	AGC[1:0] = 01 (375 mV)	AGC[1:0] = 01 (16 mV)
Local or distance	LODX = 0 (distance)	LODX = 1 (local)
FM mixer image rejection	FMINJ = 0 (low injection)	FMINJ = 0 (low injection)
AGC switch	AGCSW = 1 (FM RF AGC PIN diode drive sources 10 mA)	AGCSW = 1 (FM RF AGC PIN diode drive sinks 1 mA)
FM mixer gain	MIXGAIN = 0 (nominal)	MIXGAIN = 0 (nominal)
Software programmable port 2	SWPORT2 = 1 (LOW)	SWPORT2 = 1 (LOW)
Software programmable port 1	SWPORT1 = 0 (open-collector)	SWPORT1 = 0 (open-collector)
Setting of crystal frequency DAA	DAC[4:0] = 15 (4.6 V)	DAC[4:0] = 16 (4.4 V)
I²C-bus transmission	C2 2D B4 C0 65 22 8F	C2 0F 4E C0 42 B2 90

17. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 11. Package outline SOT314-2 (LQFP64)

18. Soldering

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

18.5 Package related soldering information

Table 34: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	**Soldering method**	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

19. Revision history

Table 35: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TEF6721HL_4	20051220	Product data sheet	-	-	TEF6721HL_3
Modifications:	• Table 29: Changed the ‘Crystal oscillator’ section; the driving of two tuners with one crystal is shown in Figure 10.				
TEF6721HL_3	20050719	Product data sheet	-	9397 750 15042	TEF6721HL_2
TEF6721HL_2	20040629	Product specification	-	9397 750 13472	TEF6721HL_1
TEF6721HL_1	20031021	Preliminary specification	-	9397 750 11379	-

20. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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25. Contents

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