MF1ICS5005

Sawn bumped 120 µm wafer specification on UV tape

Rev. 3.2 — 23 June 2010
179132

Product data sheet addendum
PUBLIC

1. General description

The MF1ICS5005 is a contactless smart card IC designed for card IC coils following the "MIFARE card IC coil design guide" and is qualified to work properly in NXP Semiconductors´ reader environment, which is built according to NXP Semiconductors´ specification.

This specification describes electrical, physical and dimensional properties of sawn wafers delivered on UV-tape.

2. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MF1ICS5005W/U7DL	Wafer	Bumped die on sawn wafer	-

3. Mechanical specification

3.1 Wafer

- Diameter: 200 mm (8")
- Maximum diameter after foil expansion: 210 mm
- Thickness: 120 µm ± 15 µm
- Flatness: not applicable
- PGDW: 27720

3.2 Wafer backside

- Material: Si
- Treatment: ground and stress relieve
- Roughness: R_a max. 0.5 µm
  R_t max. 5 µm

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3.3 Chip dimensions

- Chip (step) size: 1.062 x 1.012 mm
- Scribe lines[1]: x-line: 48.4 μm
  y-line: 48.4 μm
- Gap between chips: typ. 27 μm
  min. 5 μm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride
- Thickness: 500 nm / 600 nm

3.5 Au bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 μm
- Bump height uniformity:
  - within a die: ± 2 μm
  - within a wafer: ± 3 μm
  - wafer to wafer: ± 4 μm
- Bump flatness: ± 1.5 μm
- Bump size:
  - LA, LB, VSS[2] 104 x 104 μm
  - TESTIO[2] 89 x 104 μm
- Bump size variation: ± 5 μm
- Under bump metallization: sputtered TiW

Remark: Substrate is connected to VSS.

3.6 Fail die identification

Electronic wafer mapping covers the electrical test results and additionally the results of mechanical / visual inspection.

No inkdots are applied.

1. typical scribe line width specified (measured from metal to metal), scribe line may vary due to changing foil expansion
2. Pads VSS and TESTIO are disconnected when wafer is sawn.

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4. Limiting values

Table 2. Limiting values[1][2][3]
In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
$I_{i(max)}$	maximum input current		-	30	mA
$P_{tot/pack}$	total power dissipation per package		-	200	mW
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	ambient temperature		−25	70	°C
I_{lu}	latch-up current		±100	-	mA
V_{ESD}	electrostatic discharge voltage	measured on pin LA-LB	[4]	2	kV

[1] Stresses above one or more of the limiting values may cause permanent damage to the device.

[2] These are stress ratings only. Operation of the device at these or any other conditions above those given in the Characteristics section of the specification is not implied.

[3] Exposure to limiting values for extended periods may affect device reliability.

[4] MIL Standard 883-C method 3015; Human body model: C = 100 pF, R = 1.5 kΩ.

5. Characteristics

Table 3. Electrical characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			-	13.56	-	MHz
C_i	input capacitance	T_{amb} = 22 °C, f_i = 13.56 MHz; 2 V_{RMS}	[1]	14.4	16.1	17.4	pF
EEPROM characteristics							
$t_{cy(ER_W)}$	erasure write cycle time			-	2.9	-	ms
t_{ret}	retention time	T_{amb} = 22 °C		10	-	-	year
$N_{endu(ER_W)}$	write or erase endurance	T_{amb} = 22 °C		100 000	-	-	cycle

[1] Measured with HP4285A, Precision LCR meter.

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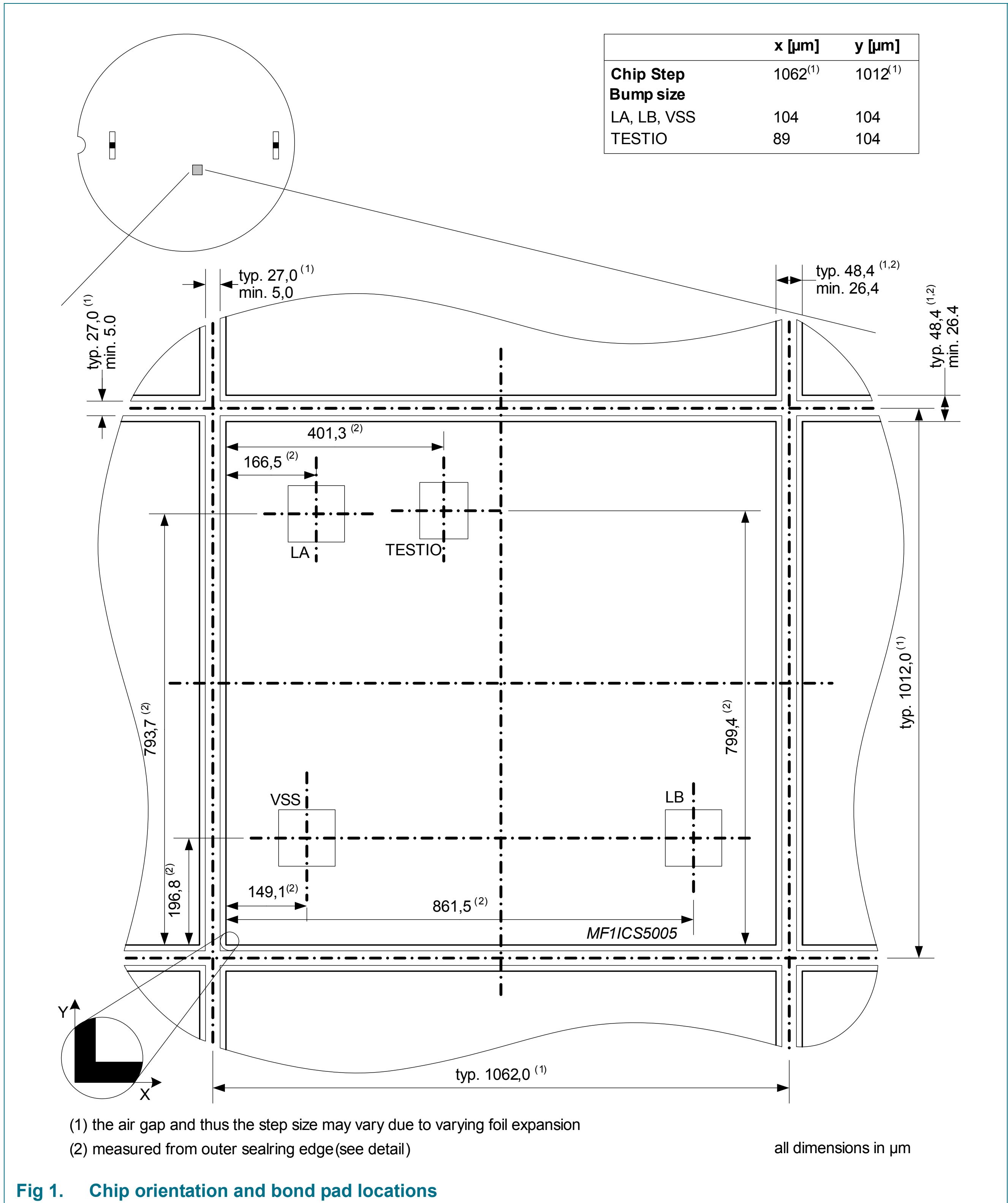
6. Chip orientation and bond pad locations



	x [µm]	y [µm]
Chip Step	1062[1]	1012[1]
Bump size		
LA, LB, VSS	104	104
TESTIO	89	104

(1) the air gap and thus the step size may vary due to varying foil expansion

(2) measured from outer sealring edge (see detail)

all dimensions in µm

Fig 1. Chip orientation and bond pad locations

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7. References

[1] **Data sheet** — General wafer specification for 8” wafers on UV-tape
BU ID Doc. No.: 1005**[3]

[2] **Data sheet** — Standard card IC MF1ICS50 memory contents after test
BU ID Doc. No.: 0061**

[3] **Data sheet** — Standard card IC MF1ICS50 functional specification
BU ID Doc. No.: 0010**

[4] **Product qualification package** — Standard card IC MF1ICS5005
BU ID Doc. No. 0809***

[5] **Application note** — MIFARE, card IC coil design guide
BU ID Doc. No. 0117**

8. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
179132	20100623	Product data sheet addendum	-	179131
Modifications:	• Section 3.3: Corrected step size and scribe line width • Figure 1: Added scribe line width dimension			
179131	20100210	Product data sheet addendum	-	179130
Modifications:	• Figure 1: chip drawing corrected • Section 9 “Legal information”: updated			
179130	20100121	Product data sheet addendum	-	-

3. ** ... document version number

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9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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