Freescale Semiconductor
Data Sheet: Technical Data

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Xtrinsic MMA52xxLW PSI5 Inertial Sensor

The MMA52xxLW family, a SafeAssure solution, includes the AKLV27 and PSI5 Version 1.3 compatible overdamped X-axis satellite accelerometers.

Features

- ±60g to ±480g Full-Scale Range
- Selectable 400 Hz, 3 Pole, or 4 pole Low-Pass Filter
- Single Pole High Pass Filter with Fast Startup and Output Rate Limiting
- PSI5 Version 1.3 Compatible
  - PSI5-P10P-500/3L Compatible
  - Programmable Time Slots with 0.5 µs Resolution
  - Selectable Baud Rate: 125 kBaud or 190.5 kBaud
  - Selectable Data Length: 8 or 10 bits
  - Selectable Error Detection: Even Parity, or 3-bit CRC
  - Optional Daisy Chain with External Low-Side Switch
  - Two-Wire Programming Mode
- 16 µs Internal Sample Rate, with Interpolation to 1 µs
- Pb-Free 16-Pin QFN, 6 x 6 Package
- Qualified AECQ100, Revision G, Grade 1 (-40°C to +125°C) (http://www.aecouncil.com/)

Typical Applications

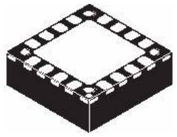
- Airbag Front and Side Crash Detection

ORDERING INFORMATION

Device	Axis	Range	Package	Shipping
MMA5206LW	X	60g	2086-01	Tubes
MMA5212LW	X	120g	2086-01	Tubes
MMA5224LW	X	240g	2086-01	Tubes
MMA5248LW	X	480g	2086-01	Tubes
MMA5206LWR2	X	60g	2086-01	Tape & Reel
MMA5212LWR2	X	120g	2086-01	Tape & Reel
MMA5224LWR2	X	240g	2086-01	Tape & Reel
MMA5248LWR2	X	480g	2086-01	Tape & Reel

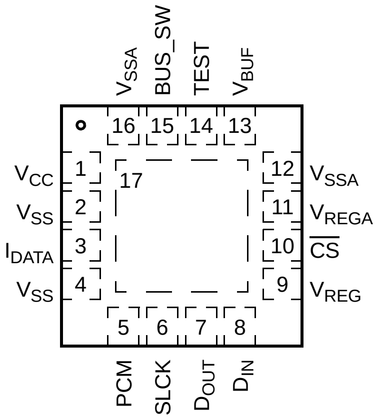
MMA52xxLW

Bottom View

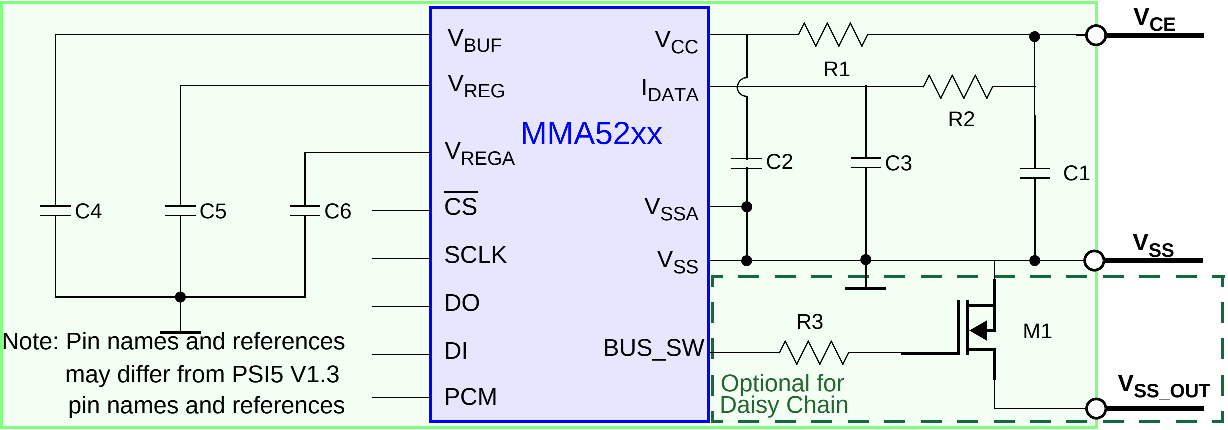


16-PIN QFN
CASE 2086-01

Top View



Pin Connections



Note: Pin names and references may differ from PSI5 V1.3 pin names and references

Figure 1. Application Diagram

Table 1. External Component Recommendations

Ref Des	Type	Description	Purpose
C1	Ceramic	2.2 nF, 10%, 50V minimum, X7R	V_{CC} Power Supply Decoupling and Signal Damping
C3	Ceramic	470 pF, 10%, 50V minimum, X7R	I_{DATA} Filtering and Signal Damping
C2	Ceramic	15 nF, 10%, 50V minimum, X7R	V_{CC} Power Supply Decoupling
C4, C5, C6	Ceramic	1 µF, 10%, 10V minimum, X7R	Voltage Regulator Output Capacitor(s)
R1	General Purpose	82Ω, 5%, 200 PPM	V_{CC} Filtering and Signal Damping
R2	General Purpose	27Ω, 5%, 200 PPM	I_{DATA} Filtering and Signal Damping
R3	General Purpose	20 kΩ, 5%, 200 PPM	Gate Resistor for External Low-Side Daisy Chain FET
M1	N-Channel MOSFET	—	Low-Side Daisy Chain Transistor

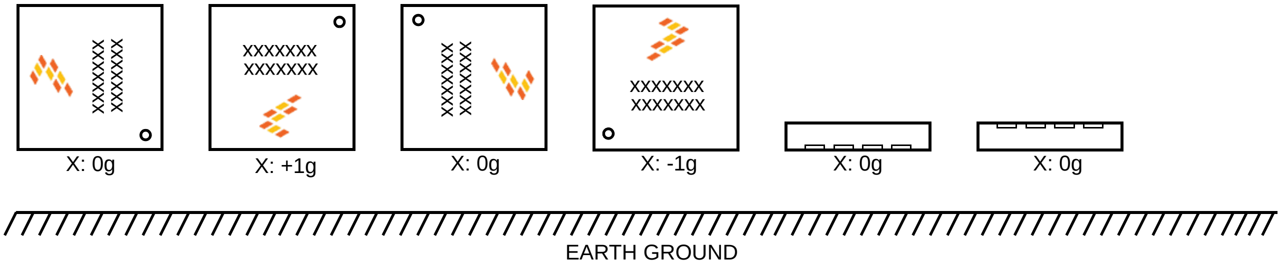


Figure 2. Device Orientation Diagram

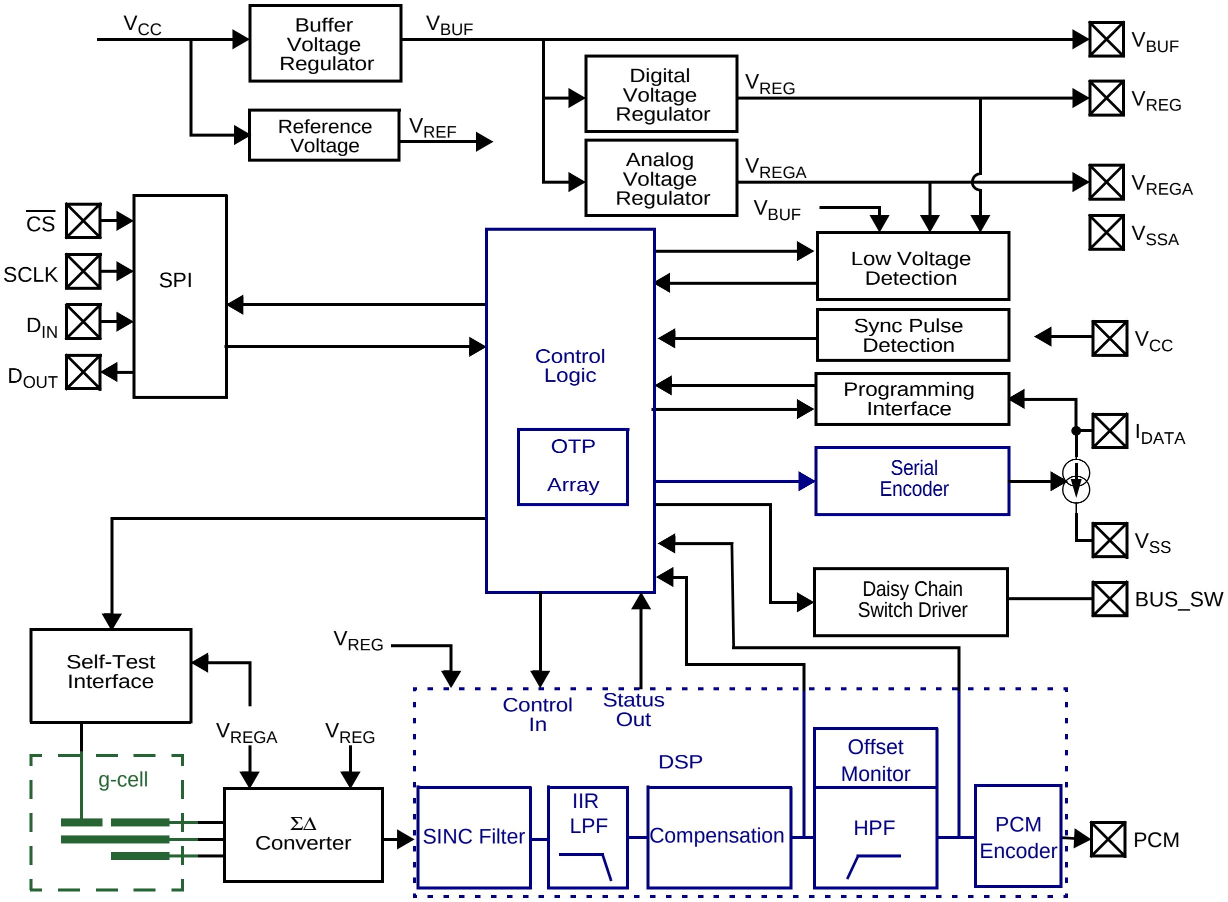


Figure 3. Internal Block Diagram

1 Pin Connections

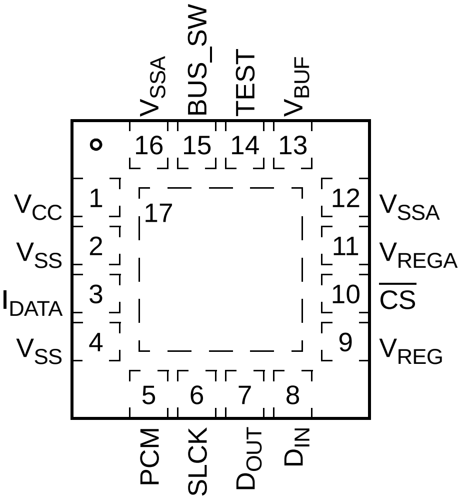


Figure 4. Top View, 16-Pin QFN Package

Table 2. Pin Description

Pin	Pin Name	Formal Name	Definition
1	V_{CC}	Supply	This pin is connected to the PSI5 power and data line through a resistor and supplies power to the device. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
2	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
3	I_{DATA}	Response Current	This pin is connected to the PSI5 power and data line through a resistor and modulates the response current for PSI5 communication. Reference Figure 1.
4	V_{SS}	Digital GND	This pin is the power supply return node for the digital circuitry.
5	PCM	PCM Output	This pin provides a 4 MHz PCM signal proportional to the acceleration data for test purposes. The output can be enabled via OTP. Reference Section 3.5.3.7. If unused, this pin must be left unconnected.
6	SCLK	SPI Clock	This input pin provides the serial clock to the SPI port for test purposes. An internal pulldown device is connected to this pin. This pin must be grounded or left unconnected in the application.
7	D_{OUT}	SPI Data Out	This pin functions as the serial data output from the SPI port for test purposes. This pin must be left unconnected in the application.
8	D_{IN}	SPI Data In	This pin functions as the serial data input to the SPI port for test purposes. An internal pulldown device is connected to this pin. This pin must be grounded or left unconnected in the application.
9	V_{REG}	Digital Supply	This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
10	CS	Chip Select	This input pin provides the chip select to the SPI port for test purposes. An internal pullup device is connected to this pin.This pin must be left unconnected in the application.
11	V_{REGA}	Analog Supply	This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V_{SSA}. Reference Figure 1.
12	VSSA	Analog GND	This pin is the power supply return node for the analog circuitry.
13	V_{BUF}	Power Supply	This pin is connected to a buffer regulator for the internal circuitry. The buffer regulator supplies both the analog (V_{REGA}) and digital (V_{REG}) supplies to provide immunity from EMC and supply dropouts on V_{CC}. An external capacitor must be connected between this pin and V_{SS}. Reference Figure 1.
14	TEST	Test Pin	This pin is must be grounded or left unconnected in the application.
15	BUS_SW	Bus Switch Gate Drive	This pin is the drive for a low-side daisy chain switch. When daisy chain mode is enabled, this pin is connected to the gate of an n-channel FET which connects V_{SS} to $V_{SS\_OUT.}$ Reference Figure 1. If unused, this pin must be left unconnected.
16	VSSA	Analog GND	This pin is the power supply return node for the analog circuitry.
17	PAD	Die Attach Pad	This pin is the die attach flag, and is internally connected to VSS. Reference Section 7 for die attach pad connection details.
	Corner Pads	Corner Pads	The corner pads are internally connected to V_{SS}.

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it.

#	Rating	Symbol	Value	Unit	
	Supply Voltage (V_{CC}, I_{DATA})				
1	Reverse Current ≤ 160 mA, t ≤ 80 ms	V_{CC_REV}	-0.7	V	(3)
2	Continuous	V_{CC_MAX}	+20.0	V	(3)
3	Transient (< 10 µs)	V_{CC_TRANS}	+25.0	V	(9)
4	$V_{BUF,}$ Test, BUS_SW		-0.3 to +4.2	V	(3)
5	V_{REG}, $V_{REGA,}$ SCLK, $\overline{CS}$, D_{IN}, D_{OUT}, PCM		-0.3 to +3.0	V	(3)
6	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±2000	g	(3)
7	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2500	g	(3)
8	Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation)	h_{DROP}	1.2	m	(5)
	Electrostatic Discharge (per AEC-Q100)				
9	External Pins (V_{CC}, I_{DATA}, V_{SS}, V_{SSA}), HBM (100 pF, 1.5 kΩ)	V_{ESD}	±4000	V	(5)
10	HBM (100 pF, 1.5 kΩ)	V_{ESD}	±2000	V	(5)
11	CDM (R = 0Ω)	V_{ESD}	±1500	V	(5)
12	MM (200 pF, 0Ω)	V_{ESD}	±200	V	(5)
	Temperature Range				
13	Storage	T_{stg}	-40 to +125	°C	(3)
14	Junction	T_J	-40 to +150	°C	(9)
15	Thermal Resistance	θ_{JC}	2.5	°C/W	(9, 14)

2.2 Operating Range

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
16	Supply Voltage	V_{CC}	V_L 4.2	—	V_H 17.0	V	(1)
17		V_{CC_UV}	$V_{VCC\_UV\_F}$	—	V_L	V	(9)
18	Programming Voltage (I_{DATA} ≤ 85 mA) Applied to $I_{DATA,}$ V_{CC}	V_{PP}	14.0	—	—	V	(3)
19	Operating Temperature Range	T_A	T_L -40	—	T_H +105	°C	(1)
20		T_A	-40	—	+125	°C	(3)

2.3 Electrical Characteristics - Supply and I/O

$V_L \le (V_{CC} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, $\Delta T \le 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
21	Quiescent Supply Current *	I_{IDLE}	4.0	—	8.0	mA	(1)
22	Modulation Supply Current *	I_{MOD}	I_{IDLE}+ 22.0	I_{IDLE}+ 26.0	I_{IDLE}+ 30.0	mA	(1)
23	Inrush Current (Power On until V_{BUF}, V_{REG}, V_{REGA} Stable)	I_{INRUSH}	—	—	30	mA	(3)
	Internally Regulated Voltages						
24	V_{BUF} *	V_{BUF}	3.60	3.80	4.00	V	(1)
25	V_{REG} *	V_{REG}	2.425	2.50	2.575	V	(1)
26	V_{REGA} *	V_{REGA}	2.425	2.50	2.575	V	(1)
	Low Voltage Detection Threshold						
27	V_{CC} Falling	$V_{VCC\_UV\_F}$	3.40	3.70	4.0	V	(3, 6)
28	V_{BUF} Falling	$V_{BUF\_UV\_F}$	2.95	3.15	3.35	V	(3, 6)
29	V_{REG} Falling	$V_{REG\_UV\_F}$	2.15	2.25	2.35	V	(3, 6)
30	V_{REGA} Falling	$V_{REGA\_UV\_F}$	2.15	2.25	2.35	V	(3, 6)
	Hysteresis						
31	V_{CC}	V_{CC_HYST}	0.10	0.25	0.40	V	(3)
32	V_{BUF}	V_{BUF_HYST}	0.05	0.10	0.15	V	(3)
33	V_{REG}	V_{REG_HYST}	0.05	0.10	0.15	V	(3)
34	V_{REGA}	V_{REGA_HYST}	0.05	0.10	0.15	V	(3)
	External Capacitor (V_{BUF}, V_{REG}, V_{REGA})						
35	Capacitance		500	1000	1500	nF	(9)
36	ESR (including interconnect resistance)	ESR	0	—	200	mΩ	(9)
	Synchronization Pulse (Figure 5)						
37	V_{IDLE} Voltage Range *	VIDLE	—	—	15.4	V	(3, 11)
38	DC Sync Pulse Detection Threshold *	ΔV_{SYNC}	V_{IDLE}+1.4	V_{IDLE}+2.0	V_{IDLE}+2.6	V	(3, 6)
39	Sync Pulse Pulldown Current	I_{SYNC_PD}	—	I_{MOD} - I_{IDLE}	—	mA	(3)
40	Output High Voltage (DO) I_{Load} = 100 µA	V_{OH}	V_{REG} - 0.1	—	—	V	(9)
41	Output Low Voltage (DO) I_{Load} = 100 µA	V_{OL}	—	—	0.1	V	(9)
42	Input High Voltage CS, SCLK, DI	V_{IH}	0.7 * V_{REG}	—	—	V	(9)
43	Input Low Voltage CS, SCLK, DI	V_{IL}	—	—	0.3 * V_{REG}	V	(9)
	Input Current						
44	High (at V_{IH}) (DI)	I_{IH}	-100	—	-10	µA	(9)
45	Low (at V_{IL}) (CS)	I_{IL}	10	—	100	µA	(9)
46	Pulldown Resistance (SCLK)	R_{PD}	20	æ	100	kΩ	(9)
47	BUS_SW Output High Voltage (BUS_SW) I_{Load} = 100 µA	$V_{BUS\_SW\_OH}$	3.15	—	V_{BUF}	V	(9)
48	Output Low Voltage (BUS_SW) I_{Load} = 100 µA	$V_{BUS\_SW\_OL}$	0.0	—	0.45	V	(9)
49	Daisy Chain Addressing Mode Sync Pulse Period		—	$t_{S-S\_PM\_L}$	—	s	(7)
50	Bus Switch Output Activation Time (C = 50 pF) From last bit of “SetAdr” Response to 80% of $V_{BUS\_SW\_OH}$	tBUS_SW	—	—	300	µs	(7)
51	Sync Pulse Blanking Time after “SetAdr” Command Received From last bit of “SetAdr” Response	$t_{DC\_BLANKING}$		200000 / f_{OSC}		s	(7)

2.4 Electrical Characteristics - Sensor And Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Sensitivity (10-bit output @ 100 Hz, referenced to 0 Hz)						
52	±60g Range *	SENS	—	8	—	LSB/g	(1)
53	±120g Range *	SENS	—	4	—	LSB/g	(1)
54	±240g Range *	SENS	—	2	—	LSB/g	(1)
55	±480g Range *	SENS	—	1	—	LSB/g	(1)
	Total Sensitivity Error (including non-linearity)						
56	$T_A = 25°C$, ≤ ±240g *	ΔSENS_240	-5	—	+5	%	(1)
57	$T_L \leq T_A \leq T_H$, ≤ ±240g *	ΔSENS_240	-7	—	+7	%	(1)
58	$T_L \leq T_A \leq T_H$, ≤ ±240g, $V_{VCC\_UV\_F} \leq V_{CC} \leq V_L$	ΔSENS_240	-7	—	+7	%	(9)
59	$T_A = 25°C$, > ±240g *	ΔSENS_480	-5	—	+5	%	(1)
60	$T_L \leq T_A \leq T_H$, > ±240g *	ΔSENS_480	-7	—	+7	%	(1)
61	$T_L \leq T_A \leq T_H$, > ±240g, $V_{VCC\_UV\_F} \leq V_{CC} \leq V_L$	ΔSENS_480	-7	—	+7	%	(9)
	Digital Offset Before Offset Cancellation						
62	10-bit *	OFF_{10Bit}	-52	0	+52	LSB	(1)
63	10-bit, $T_L \leq T_A \leq T_H$, $V_{VCC\_UV\_F} \leq V_{CC} \leq V_L$	OFF_{10Bit}	-52	0	+52	LSB	(9)
	Digital Offset After Offset Cancellation						
64	10-bit, 0.3 Hz HPF or 0.1 Hz HPF *	OFF_{10Bit}	-1	0	+1	LSB	(1)
65	10-bit, 0.04 Hz HPF *	OFF_{10Bit}	-2	0	+2	LSB	(9)
	Continuous Offset Monitor Limit						
66	10-bit output, before compensation	OFF_{MON}	-66	—	+66	LSB	(3)
	Range of Output (10-bit Mode)						
67	Acceleration	RANGE	-480	—	+480	LSB	(3)
	Cross-Axis Sensitivity						
68	Z-axis to X-axis *	V_{ZX}	-5	—	+5	%	(3)
69	Y-axis to X-axis *	V_{YX}	-5	—	+5	%	(3)
70	System Output Noise Peak (10-bit Mode, 1 Hz - 1 kHz, All Ranges) *	n_{Peak}	-4	—	+4	LSB	(3)
71	System Output Noise RMS (10-bit mode, 1 Hz - 1 kHz, All Ranges) *	n_{RMS}	—	—	+1.0	LSB	(3)
	Non-linearity						
72	10-bit output, ≤ ±240g	NL_{OUT_240g}	-2	—	+2	%	(3)
73	10-bit output, > ±240g	NL_{OUT_480g}	-2	—	+2	%	(3)

2.5 Electrical Characteristics - Self-Test and Overload

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

#	Characteristic	Symbol	Min	Typ	Max	Units	
	10-Bit Output During Active Self-Test ($T_L \leq T_A \leq T_H$)						
74	±60g Range *	g_{ST10_60X}	120	—	280	LSB	(3)
75	±120g Range *	g_{ST10_120X}	40	—	160	LSB	(3)
76	±240g Range *	g_{ST10_240X}	56	—	184	LSB	(3)
77	±480g Range *	g_{ST10_480X}	8	—	112	LSB	(3)
78	Acceleration (without hitting internal g-cell stops) ±60g Range Positive/Negative	$g_{g\text{-}cell\_Clip60X}$	400	456	500	g	(9)
79	Acceleration (without hitting internal g-cell stops) ±120g Range Positive/Negative	$g_{g\text{-}cell\_Clip120X}$	400	456	500	g	(9)
80	Acceleration (without hitting internal g-cell stops) ±240g Range Positive/Negative	$g_{g\text{-}cell\_Clip240X}$	1750	2065	2300	g	(9)
81	Acceleration (without hitting internal g-cell stops) ±480g Range Positive/Negative	$g_{g\text{-}cell\_Clip480X}$	1750	2065	2300	g	(9)
82	ΣΔ and Sinc Filter Clipping Limit ±60g Range Positive/Negative	$g_{ADC\_Clip60X}$	191	210	233	g	(9)
83	ΣΔ and Sinc Filter Clipping Limit ±120g Range Positive/Negative	$g_{ADC\_Clip120X}$	353	380	410	g	(9)
84	ΣΔ and Sinc Filter Clipping Limit ±240g Range Positive/Negative	$g_{ADC\_Clip240X}$	928	1055	1218	g	(9)
85	ΣΔ and Sinc Filter Clipping Limit ±480g Range Positive/Negative	$g_{ADC\_Clip480X}$	1690	1879	2106	g	(9)

2.6 Dynamic Electrical Characteristics - PSI5

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
	Initialization Timing						
86	Phase 1	t_{PSI5_INIT1}	—	532000 / f_{OSC}	—	s	(7)
87	Phase 2 (10-Bit, Synchronous Mode, k = 4)	$t_{PSI5\_INIT2\_10s}$	—	256 * $t_{S\text{-}S}$	—	s	(7)
88	Phase 2 (8-Bit, Synchronous Mode, k = 8)	$t_{PSI5\_INIT2\_8s}$	—	288 * $t_{S\text{-}S}$	—	s	(7)
89	Phase 2 (10-Bit, Asynchronous Mode 0, k = 8)	$t_{PSI5\_INIT2\_10a0}$	—	512 * t_{ASYNC}	—	s	(7)
90	Phase 2 (8-Bit, Asynchronous Mode 0, k = 16)	$t_{PSI5\_INIT2\_8a0}$	—	576 * t_{ASYNC}	—	s	(7)
91	Phase 3 (10-Bit, Synchronous Mode, ST_RPT = 0)	$t_{PSI5\_INIT3\_10s}$	—	2 * $t_{S\text{-}S}$	—	s	(7, 12)
92	Phase 3 (8-Bit, Synchronous Mode, ST_RPT = 0)	$t_{PSI5\_INIT3\_8s}$	—	2 * $t_{S\text{-}S}$	—	s	(7, 12)
93	Phase 3 (10-Bit, Asynchronous Mode 0, ST_RPT = 0)	$t_{PSI5\_INIT3\_10a0}$	—	19 * t_{ASYNC}	—	s	(7, 12)
94	Phase 3 (8-Bit, Asynchronous Mode 0, ST_RPT = 0)	$t_{PSI5\_INIT3\_8a0}$	—	2 * t_{ASYNC}	—	s	(7, 12)
95	Offset Cancellation Stage 1 Operating Time	t_{OC1}	—	320000 / f_{OSC}	—	s	(7)
96	Offset Cancellation Stage 2 Operating Time	t_{OC2}	—	280000 / f_{OSC}	—	s	(7)
97	Self-Test Stage 1 Operating Time	t_{ST1}	—	128000 / f_{OSC}	—	s	(7)
98	Self-Test Stage 2 Operating Time	t_{ST2}	—	128000 / f_{OSC}	—	s	(7)
99	Self-Test Stage 3 Operating Time	t_{ST3}	—	128000 / f_{OSC}	—	s	(7)
100	Self-Test Repetitions	ST_RPT	0	—	5		(7, 12)
101	Programming Mode Entry Window	t_{PME}	—	300000 / f_{OSC}	—	s	(7)
	Synchronization Pulse (Figure 5, Figure 28 and Figure 32)						
102	Reset to first sync pulse (Program Mode Entry)	t_{RS_PM}	58	—	—	ms	(7)
103	Reset to first sync pulse (Normal Mode)	t_{RS}	t_{PSI5_INIT1}	—	—	s	(7)
104	Sync Pulse Period	$t_{S\text{-}S}$	t_{SYNC_OFF}	—	—	µs	(7)
105	Sync Pulse Width	t_{SYNC}	9	—	—	µs	(7)
106	Sync Pulse Reference LPF time constant	t_{SYNC_LPF}	120	280	—	µs	(9)
107	Sync Pulse Reference Discharge Start Time	$t_{SYNC\_LPF\_RST\_ST}$	—	66 / f_{OSC}	—	s	(7)
108	Sync Pulse Reference Discharge Activation Time	$t_{SYNC\_LPF\_RST}$	—	616 / f_{OSC}	—	s	(7)
109	Sync Pulse Detection Disable Time (BLANKTIME = 0)	$t_{SYNC\_OFF\_500}$	—	1810 / f_{OSC}	—	s	(7)
110	Analog Delay of Sync Pulse Detection	$t_{A\_SYNC\_DLY}$	50		600	ns	(9)
111	Sync Pulse Pulldown Function Delay Time	t_{PD_DLY}	—	74 / f_{OSC}	—	s	(7)
112	Sync Pulse Pulldown Function Activate Time	t_{PD_ON}	—	64 / f_{OSC}	—	s	(7)
113	Sync Pulse Detection Jitter	t_{SYNC_JIT}	0	—	2 / f_{OSC}	s	(7)
114	Data Transmission Single Bit Time (PSI5 Low Bit Rate) *	t_{BIT_LOW}	7.6000	8.0000	8.4000	µs	(7)
115	Data Transmission Single Bit Time (PSI5 High Bit Rate) *	t_{BIT_HI}	4.9875	5.2500	5.5125	µs	(7)
	Modulation Current (20% to 80% of $I_{MOD} - I_{IDLE}$)						
116	Rise Time	t_{RISE}	324	463	602	ns	(3)
117	Fall Time	t_{FALL}	324	463	602	ns	(3)
118	Position of bit transition (PSI5 Low Baud Rate) *	$t_{Bittrans\_LowBaud}$	49	50	51	%	(7)
119	Position of bit transition (PSI5 High Baud Rate) *	$t_{Bittrans\_HighBaud}$	47	æ	53	%	(7)
120	Asynchronous Response Time *	t_{ASYNC}	—	912 / f_{OSC}	æ	s	(7)
	Time Slots						
121	Minimum Programmed Time Slot (TIMESLOTx = 0x001)	$t_{TIMESLOTx\_MIN}$	—	2 / f_{OSC}	—	s	(7, 9)
122	Maximum Programmed Time Slot (TIMESLOTx = 0x3FF)	$t_{TIMESLOTx\_MAX}$	—	2046 / f_{OSC}	—	s	(3, 7)
123	Default Time Slot (TIMESLOTx = 0x000)	$t_{TIMESLOT\_DFLT}$	—	186 / f_{OSC}	—	s	(3, 7)
124	Time Slot Resolution *	$t_{TIMESLOTx\_RES}$	—	2 / f_{OSC}	—	s/LSB	(7)
125	Sync Pulse to Daisy Chain Default Time Slot 1	$t_{TIMESLOT\_DC1}$	—	186 / f_{OSC}	—	s	(7)
126	Sync Pulse to Daisy Chain Default Time Slot 2	$t_{TIMESLOT\_DC2}$	—	768 / f_{OSC}	—	s	(7)
127	Sync Pulse to Daisy Chain Default Time Slot 3	$t_{TIMESLOT\_DC3}$	—	1400 / f_{OSC}	—	s	(7)
128	Sync Pulse to Daisy Chain Programming Time Slot	$t_{TIMESLOT\_DCP}$	—	186 / f_{OSC}	—	s	(7)
129	Data Interpolation Latency (Figure 35, Figure 36)	t_{LAT_INTERP}	64 / f_{OSC}	—	65 / f_{OSC}	s	(7)
130	Data Setup Time - Synchronous Mode (Figure 36)	$t_{DATASETUP\_synch}$	48 / f_{OSC}	—	56 / f_{OSC}	s	(7)
131	Data Setup Time - Double Sample Rate Mode (Figure 37)	$t_{DATASETUP\_double}$	48 / f_{OSC}	—	60 / f_{OSC}	s	(7)
132	Data Setup Time - 16-bit Resolution Mode (Figure 39)	$t_{DATASETUP\_16}$	48 / f_{OSC}	—	60 / f_{OSC}	s	(7)
	Programming Mode Timing						
133	Programming Mode Sync Pulse Period	$t_{S\text{-}S\_PM\_L}$	495	500	505	µs	(7)
134	Programming Mode Command Timeout	$t_{PM\_TIMEOUT}$	—	4 * $t_{S\text{-}S\_PM}$	—	µs	(7)
135	OTP Write Command to $V_{CC} = V_{PP}$	t_{PROG_HOLD}	—	—	20	µs	(7)
136	OTP Write CMD Response to OTP programming start	t_{PROG_DELAY}	—	—	40	ms	(7)
137	Time to program the OTP User Array	t_{PROG_ARRAY}	70	—	—	ms	(7)

2.7 Dynamic Electrical Characteristics - Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
138	Internal Oscillator Frequency *	f_{OSC}	3.80	4	4.20	MHz	(1)
	DSP Low-Pass Filter (Note15)						
139	Cutoff frequency LPF0 (referenced to 0 Hz) *	f_{C_LPF0}	—	400	—	Hz	(7)
140	Filter Order LPF0 *	O_{LPF0}	—	3	—	1	(7)
141	Cutoff frequency LPF1 (referenced to 0 Hz) *	f_{C_LPF1}	—	400	—	Hz	(7)
142	Filter Order LPF1 *	O_{LPF1}	—	4	—	1	(7)
	DSP Offset Cancellation Low-Pass Filter (Note 15)						
143	Offset Cancellation Low-Pass Filter Input Sample Rate	$t_{OC\_SampleRate}$	—	256	—	µs	(7)
144	Stage 1 Cutoff frequency, Startup Phase 1	f_{C_OC10}	—	10.0	—	Hz	(7)
145	Stage 1 Filter Order, Startup Phase 1	O_{OC10}	—	1	—	1	(7)
146	Stage 2 Cutoff frequency, Startup Phase 1	f_{C_OC03}	—	0.300	—	Hz	(7)
147	Stage 2 Filter Order, Startup Phase 1	O_{OC03}	—	1	—	1	(7)
148	Cutoff frequency, Option 0	f_{C_OC0}	—	0.100	—	Hz	(7)
149	Filter Order, Option 0	O_{OC0}	—	1	—	1	(7)
150	Offset Cancellation Output Update Rate (8-Bit Mode)	$t_{OffRate\_8}$	—	f_{OSC} / 2e6	—	s	(7)
151	Offset Cancellation Output Step Size (8-Bit Mode)	OFF_{Step_8}	—	0.125	—	LSB	(7)
152	Offset Cancellation Output Update Rate (10-Bit Mode)	$t_{OffRate\_10}$	—	f_{OSC} / 2e6	—	s	(7)
153	Offset Cancellation Output Step Size (10-Bit Mode)	OFF_{Step_10}	—	0.5	—	LSB	(7)
154	Offset Monitor Update Frequency	$OFFMON_{OSC}$	—	f_{OSC}/2000	—	Hz	(7)
155	Offset Monitor Count Limit	$OFFMON_{CNTLIMIT}$	—	4096	—	1	(7)
156	Offset Monitor Counter Size	$OFFMON_{CNTSIZE}$	—	8192	—	1	(7)
	Sensing Element Natural Frequency						
157	±60g	f_{gcell_X60}	12651	—	13871	Hz	(9)
158	±120g	f_{gcell_X120}	12651	—	13871	Hz	(9)
159	±240g	f_{gcell_X240}	26000	—	28700	Hz	(9)
160	±480g	f_{gcell_X480}	26000	—	28700	Hz	(9)
	Sensing Element Rolloff Frequency (-3 db)						
161	±60g	f_{gcell_X60}	938	—	2592	Hz	(9)
162	±120g	f_{gcell_X120}	938	—	2592	Hz	(9)
163	±240g	f_{gcell_X240}	3952	—	14370	Hz	(9)
164	±480g	f_{gcell_X480}	3952	—	14370	Hz	(9)
	Sensing Element Damping Ratio						
165	±60g	ζ_{gcell_X60}	2.760	—	6.770	—	(9)
166	±120g	ζ_{gcell_X120}	2.760	—	6.770	—	(9)
167	±240g	ζ_{gcell_X240}	1.260	—	3.602	—	(9)
168	±480g	ζ_{gcell_X480}	1.260	—	3.602	—	(9)
	Sensing Element Delay (@100 Hz)						
169	±60g	$f_{gcell\_delay\_X60}$	63	—	170	µs	(9)
170	±120g	$f_{gcell\_delay\_X120}$	63	—	170	µs	(9)
171	±240g	$f_{gcell\_delay\_X240}$	13	—	40	µs	(9)
172	±480g	$f_{gcell\_delay\_X480}$	13	—	40	µs	(9)
173	Package Resonance Frequency	$f_{Package}$	100	—	—	kHz	(9)

2.8 Dynamic Electrical Characteristics - Supply and SPI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

#	Characteristic	Symbol	Min	Typ	Max	Units	
174	Quiescent Current Settling Time (Power Applied to Iq = I_{IDLE} ± 2mA)	t_{SET}	—	—	5	ms	(3)
175	Reset Recovery Internal Delay (After internal POR)	t_{INT_INIT}	—	16000 / f_{OSC}	—	s	(7)
	V_{CC} Micro-cut ($C_{BUF}=C_{REG}=C_{REGA}=1\ \mu F$)						
176	Survival Time (V_{CC} disconnect without Reset, $C_{BUF}=C_{REG}=C_{REGA}=700$ nF)	$t_{VCC\_MICROCUTmin}$	30	—	—	µs	(3)
177	Survival Time (V_{CC} disconnect without Reset, $C_{BUF}=C_{REG}=C_{REGA}=1\ \mu F$)	$t_{VCC\_MICROCUT}$	50	—	—	µs	(3)
178	Reset Time (V_{CC} disconnect above which Reset is guaranteed)	t_{VCC_RESET}	—	—	1000	µs	(3)
	V_{BUF}, Capacitor Monitor Disconnect Time (Figure 10)						
179	POR to first Capacitor Test Disconnect	$t_{POR\_CAPTEST}$	—	12000 / f_{OSC}	—	s	(7)
180	Disconnect Time (Figure 10)	$t_{CAPTEST\_TIME}$	—	1.5	5.0	µs	(7)
181	Disconnect Delay, Asynchronous Mode (Figure 10)	$t_{CAPTEST\_ADLY}$	—	688 / f_{OSC}	—	s	(7)
182	Disconnect Delay, Synchronous Mode (Figure 11)	$t_{CAPTEST\_SDLY}$	—	72 / f_{OSC}	—	s	(7)
	V_{REG}, V_{REGA} Capacitor Monitor						
183	POR to first Capacitor Test Disconnect	$t_{POR\_CAPTEST}$	—	12000 / f_{OSC}	—	s	(7)
184	Disconnect Time	$t_{CAPTEST\_TIME}$	—	6 / f_{OSC}	—	s	(7)
185	Disconnect Rate	$t_{CAPTEST\_RATE}$	—	256 / f_{OSC}	—	s	(7)
	Serial Interface Timing (See Figure 7, $C_{DOUT} \leq 80$ pF, $R_{DOUT} \geq 10$ kΩ)						
186	Clock (SCLK) period (10% of V_{CC} to 10% of V_{CC})	t_{SCLK}	320	—	—	ns	(9)
187	Clock (SCLK) high time (90% of V_{CC} to 90% of V_{CC})	t_{SCLKH}	120	—	—	ns	(9)
188	Clock (SCLK) low time (10% of V_{CC} to 10% of V_{CC})	t_{SCLKL}	120	—	—	ns	(9)
189	Clock (SCLK) rise time (10% of V_{CC} to 90% of V_{CC})	t_{SCLKR}	—	15	40	ns	(9)
190	Clock (SCLK) fall time (90% of V_{CC} to 10% of V_{CC})	t_{SCLKF}	—	15	28	ns	(9)
191	$\overline{CS}$ asserted to SCLK high ($\overline{CS}$ = 10% of V_{CC} to SCLK = 10% of V_{CC})	t_{LEAD}	60	—	—	ns	(9)
192	$\overline{CS}$ asserted to D_{OUT} valid ($\overline{CS}$ = 10% of V_{CC} to D_{OUT} = 10/90% of V_{CC})	t_{ACCESS}	—	—	60	ns	(9)
193	Data setup time (D_{IN} = 10/90% of V_{CC} to SCLK = 10% of V_{CC})	t_{SETUP}	20	—	—	ns	(9)
194	D_{IN} Data hold time (SCLK = 90% of V_{CC} to D_{IN} = 10/90% of V_{CC})	t_{HOLD_IN}	10	—	—	ns	(9)
195	D_{OUT} Data hold time (SCLK = 90% of V_{CC} to D_{OUT} = 10/90% of V_{CC})	t_{HOLD_OUT}	0	—	—	ns	(9)
196	SCLK low to data valid (SCLK = 10% of V_{CC} to D_{OUT} = 10/90% of V_{CC})	t_{VALID}	—	—	50	ns	(9)
197	SCLK low to $\overline{CS}$ high (SCLK = 10% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	t_{LAG}	60	—	—	ns	(9)
198	$\overline{CS}$ high to D_{OUT} disable ($\overline{CS}$ = 90% of V_{CC} to D_{OUT} = Hi Z)	$t_{DISABLE}$	—	—	60	ns	(9)
199	$\overline{CS}$ high to $\overline{CS}$ low ($\overline{CS}$ = 90% of V_{CC} to $\overline{CS}$ = 90% of V_{CC})	t_{CSN}	1000	—	—	ns	(9)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at wafer probe.
3. Verified by characterization
4. * Indicates critical characteristic.
5. Verified by qualification testing.
6. Parameters verified by pass/fail testing in production.
7. Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
8. N/A.
9. Verified by simulation.
10. N/A.
11. Measured at V_{CC} pin; V_{SYNC} guaranteed across full V_{IDLE} range.
12. Self-Test repeats on failure up to a ST_RPT_{MAX} times before transmitting Sensor Error Message.
13. N/A.
14. Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
15. Filter cutoff frequencies are directly dependent upon the internal oscillator frequency.

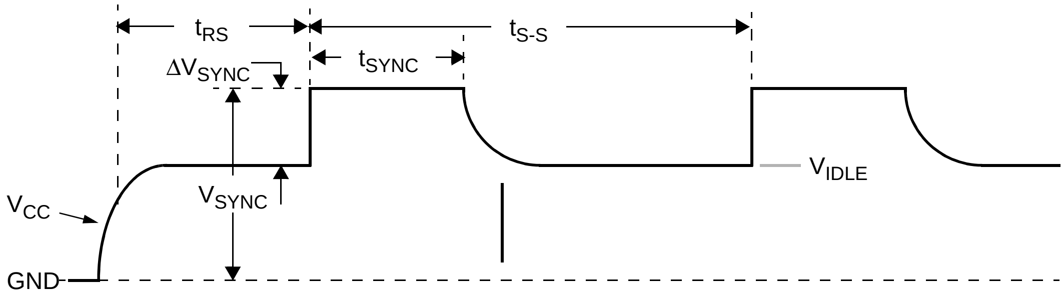


Figure 5. Sync Pulse Characteristics

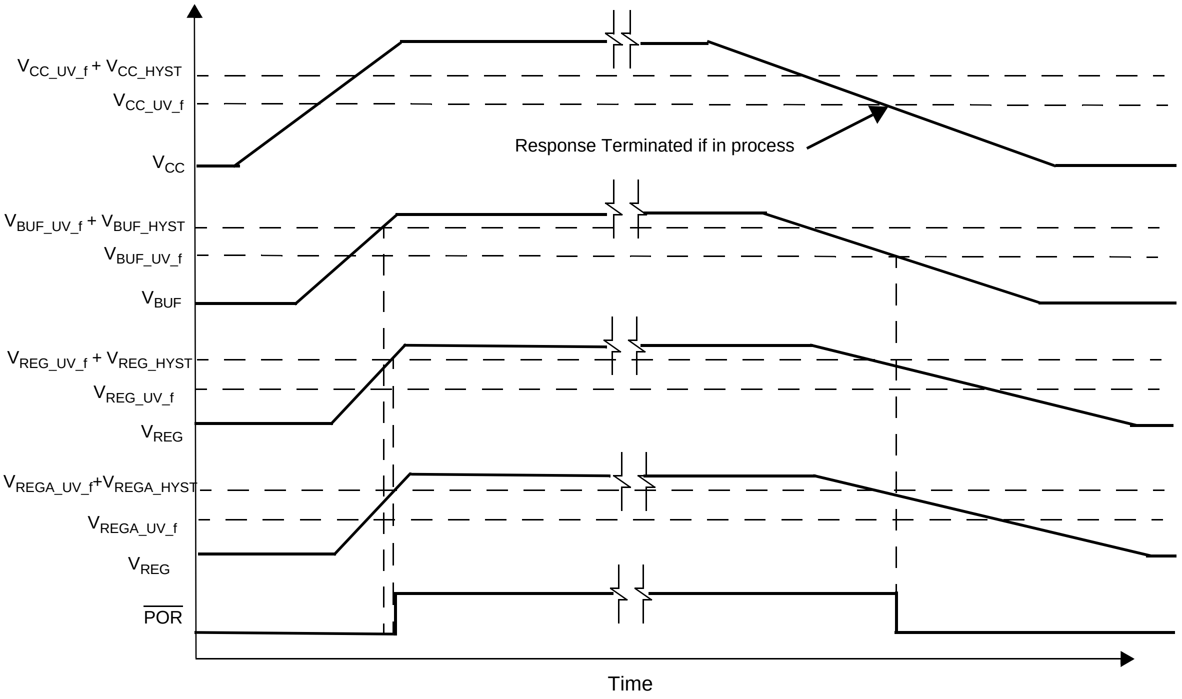


Figure 6. Powerup Timing

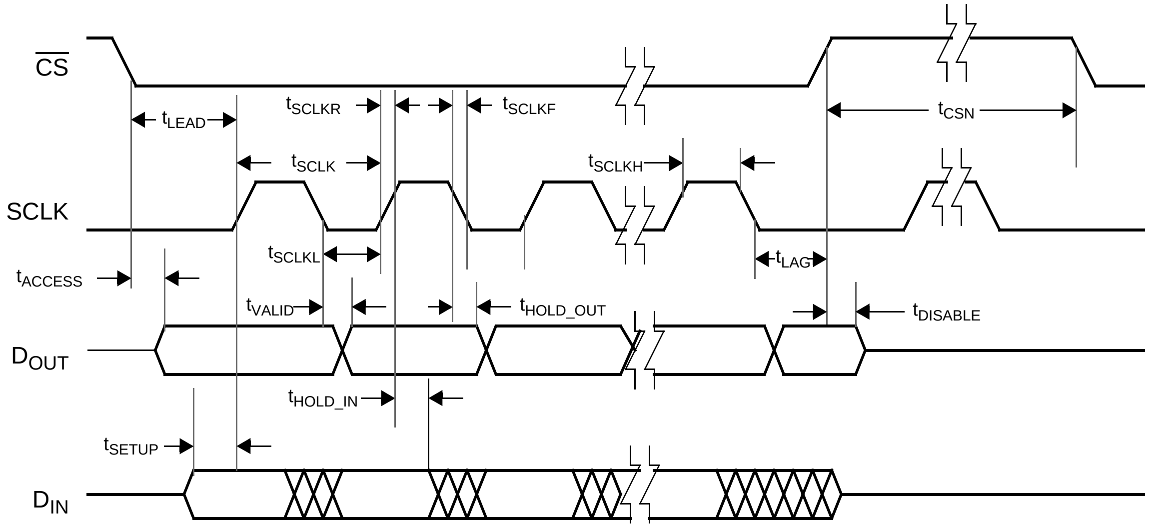


Figure 7. Serial Interface Timing

3 Functional Description

3.1 User Accessible Data Array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable block, an OTP user programmable block, and read only registers for device status. The OTP blocks incorporate independent error detection circuitry for fault detection (reference Section 3.2). Portions of the factory programmable array are reserved for factory-programmed trim values. The user accessible data is shown in Table 3.

Table 3. User Accessible Data

Byte Addr (XLong Msg)	Register	Nibble Addr (Long Msg)	Bit Function				Nibble Addr (Long Msg)	Bit Function				Type
			7	6	5	4		3	2	1	0	
$00	SN0	$01	SN[7]	SN[6]	SN[5]	SN[4]	$00	SN[3]	SN[2]	SN[1]	SN[0]	F, R
$01	SN1	$03	SN[15]	SN[14]	SN[13]	SN[12]	$02	SN[11]	SN[10]	SN[9]	SN[8]	
$02	SN2	$05	SN[23]	SN[22]	SN[21]	SN[20]	$04	SN[19]	SN[18]	SN[17]	SN[16]	
$03	SN3	$07	SN[31]	SN[30]	SN[29]	SN[28]	$06	SN[27]	SN[26]	SN[25]	SN[24]	
$04	DEVCFG1	$09	0	0	1	0	$08	AXIS	RNG[2]	RNG[1]	RNG[0]	
$05	DEVCFG2	$0B	LOCK_U	PCM	SYNC_PD	LATENCY	$0A	DATASIZE	BLANKTIME	P_CRC	BAUD	U, R
$06	DEVCFG3	$0D	TRANS_MD[1]	TRANS_MD[0]	LPF[1]	LPF[0]	$0C	TIMESLOTB[9]	TIMESLOTB[8]	TIMESLOTA[9]	TIMESLOTA[8]	
$07	DEVCFG4	$0F	TIMESLOTA[7]	TIMESLOTA[6]	TIMESLOTA[5]	TIMESLOTA[4]	$0E	TIMESLOTA[3]	TIMESLOTA[2]	TIMESLOTA[1]	TIMESLOTA[0]	
$08	DEVCFG5	$11	TIMESLOTB[7]	TIMESLOTB[6]	TIMESLOTB[5]	TIMESLOTB[4]	$10	TIMESLOTB[3]	TIMESLOTB[2]	TIMESLOTB[1]	TIMESLOTB[0]	
$09	DEVCFG6	$13	INIT2_EXT	ASYNC	U_DIR[1]	U_DIR[0]	$12	U_REV[3]	U_REV[2]	U_REV[1]	U_REV[0]	
$0A	DEVCFG7	$15	MONTH[3]	MONTH[2]	MONTH[1]	MONTH[0]	$14	YEAR[3]	YEAR[2]	YEAR[1]	YEAR[0]	
$0B	DEVCFG8	$17	UD[2]	UD[1]	UD[0]	DAY[4]	$16	DAY[3]	DAY[2]	DAY[1]	DAY[0]	
$0C	SC	$19	0	TM_B	RESERVED	IDEN_B	$18	OC_INIT_B	IDEF_B	OFF_B	0	R
$0D	MFG_ID	$1B	MFG_ID[7]	MFG_ID[6]	MFG_ID[5]	MFG_ID[4]	$1A	MFG_ID[3]	MFG_ID[2]	MFG_ID[1]	MFG_ID[0]	U, R

Type codes

F: Freescale programmed OTP location
U: User programmable OTP location via PSI5
R: Readable register via PSI5

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each device during manufacturing. The serial number is composed of the following information:

Bit Range	Content
SN[12:0]	Serial Number
SN[31:13]	Lot Number

Serial numbers begin at 1 for all produced devices in each lot and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the factory programmed OTP CRC verification. Reference Section 3.2.1 for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Factory Configuration Register (DEVCFG1)

The factory configuration register is a factory programmed, read only register which contains user specific device configuration information. The factory configuration register is included in the factory programmed OTP CRC verification.

Location		**Bit**							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$04	DEVCFG1	0	0	1	0	AXIS	RNG[2]	RNG[1]	RNG[0]
Factory Default		0	0	1	0	0	0	0	0

3.1.2.1 Axis Indication Bit (AXIS)

The axis indication bit indicates the axes of sensitivity as shown below. This bit is factory programmed.

AXIS	Sensitivity Axis
0	X
1	Z

3.1.2.2 Range Indication Bits (RNG[2:0])

The range indication bits are factory programmed and indicate the full-scale range of the device as shown below.

RNG[2]	RNG[1]	RNG[0]	Full-Scale Acceleration Range	g-Cell Design	PSI5 Init Data Transmission (D9) Reference Table 13
0	0	0	Reserved	N/A	0001
0	0	1	±60g	Medium-g	0111
0	1	0	Reserved	N/A	0010
0	1	1	±120 g	Medium-g	1000
1	0	0	Reserved	N/A	0011
1	0	1	±240 g	High-g	1001
1	1	0	Reserved	N/A	0100
1	1	1	±480 g	High-g	1010

3.1.3 Device Configuration 2 Register (DEVCFG2)

Device configuration register 2 is a user programmable OTP register that contains device configuration information.

Location		**Bit**							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$05	DEVCFG2	LOCK_U	PCM	SYNC_PD	LATENCY	DATASIZE	BLANKTIME	P_CRC	BAUD
Factory Default		0	0	0	0	0	0	0	0

3.1.3.1 User Configuration Lock Bit (LOCK_U)

The LOCK_U bit allows the user to prevent writes to the user configuration array once programming is completed.

If the LOCK_U bit is written to ‘1’ when a PSI5 “Execute Programming of NVM” command is executed, the LOCK_U OTP bit will be programmed. Upon completion of the OTP programming, an OTP readout will be executed, locking the array from future OTP writes. The User Programmable OTP Array Error Detection Verification is also activated (Reference Section 3.2.2).

3.1.3.2 PCM Enable Bit (PCM)

The PCM bit enables the PCM output pin. When the PCM bit is set, the PCM output pin is active and outputs a Pulse Code Modulated signal proportional to the acceleration response. Reference Section 3.5.3.7 for more information regarding the PCM output. When the PCM bit is cleared, the PCM output pin is actively pulled low.

PCM	PCM Output
0	Actively Pulled Low
1	PCM Signal Enabled

3.1.3.3 Sync Pulse Pulldown Enable Bit (SYNC_PD)

The sync pulse pulldown enable bit selects if the sync pulse pulldown is enabled once a sync pulse is detected. Reference Section 4.2.1.2 for more information regarding the sync pulse pulldown.

SYNC_PD	Sync Pulse Pulldown
0	Disabled
1	Enabled

If Daisy Chain Mode is enabled, the Sync Pulse Pulldown is enabled as listed below:

SYNC_PD	Daisy Chain Address Programmed	“Run Mode” Command Received	Daisy Chain Address = ‘001’	Sync Pulse Pulldown
0	x	x	x	Disabled
1	No	x	x	Enabled
1	Yes	No	x	Disabled
1	Yes	Yes	No	Disabled
1	Yes	Yes	Yes	Enabled

3.1.3.4 Latency Selection Bit (LATENCY)

The latency selection bit selects between one of two data latency methods to accommodate synchronized sampling or simultaneous sampling. Reference Section 4.5 for more information regarding latency and data synchronization.

Latency	Data Latency
0	Simultaneous Sampling Mode (Latency relative to Sync Pulse)
1	Synchronous Sampling Mode (Latency relative to Time Slot)

3.1.3.5 Data Size Selection Bit (DATASIZE)

The data size selection bit selects one of two data lengths for the PSI5 response message as shown below.

DATASIZE	Data Length
0	10 Bits
1	8 Bits

3.1.3.6 PSI5 Sync Pulse Blanking Time Selection Bit (BLANKTIME)

The PSI5 sync pulse blanking time selection bit selects the timing for ignoring sync pulses after successful reception of a sync pulse. Reference Section 4.2.1.1 for details regarding sync pulse detection and blanking.

BLANKTIME	Blanking Time Method
0	Maximum of $t_{SYNC\_OFF\_500}$ or Response Transmission Complete
1	Blanking Time determined by end of response transmission for programmed time slot

3.1.3.7 PSI5 Response Message Error Detection Selection Bit (P_CRC)

The PSI5 response message error detection selection bit selects either even parity, or a 3-Bit CRC for error detection of the PSI5 response message. Reference Section 4.3.3 for details regarding response message error detection.

P_CRC	Parity or CRC
0	Parity
1	CRC

Note: The PSI5 specification recommends parity for data lengths of 10 bits or less.

3.1.3.8 Baud Rate Selection Bit (BAUD)

The baud rate selection bit selects one of two PSI5 baud rates as shown below. Reference Section 2.6 for baud rate timing specifications.

BAUD	Baud Rate
0	Low Baud Rate (125 kBaud)
1	High Baud Rate (190.5 kBaud)

3.1.4 Device Configuration Registers (DEVCFG3, DEVCFG4, DEVCFG5)

Device configuration registers 3, 4, and 5 are user programmable OTP registers which contain device configuration information.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$06	DEVCFG3	TRANS_MD[1]	TRANS_MD[0]	LPF[1]	LPF[0]	TIMESLOTB[9]	TIMESLOTB[8]	TIMESLOTA[9]	TIMESLOTA[8]
$07	DEVCFG4	TIMESLOTA[7]	TIMESLOTA[6]	TIMESLOTA[5]	TIMESLOTA[4]	TIMESLOTA[3]	TIMESLOTA[2]	TIMESLOTA[1]	TIMESLOTA[0]
$08	DEVCFG5	TIMESLOTB[7]	TIMESLOTB[6]	TIMESLOTB[5]	TIMESLOTB[4]	TIMESLOTB[3]	TIMESLOTB[2]	TIMESLOTB[1]	TIMESLOTB[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.4.1 PSI5 Transmission Mode Selection Bits (TRANS_MD[1:0])

The PSI5 transmission mode selection bits select the PSI5 transmission mode as shown below.

TRANS_MD[1]	TRANS_MD[0]	Operating Mode	Reference
0	0	Normal Mode (Asynchronous or Parallel, Synchronous)	Section 4.5.1
0	1	Synchronous Double Sample Rate Mode	Section 4.5.1.3
1	0	16-bit Resolution Mode (2 10-bit Responses)	Section 4.5.2
1	1	Daisy Chain Mode	Section 4.5.4

3.1.4.2 Low-Pass Filter Selection Bit (LPF[1:0])

The low-pass filter selection bits select the low-pass filter for the acceleration signal as described below:

LPF[1]	LPF[0]	Low-Pass Filter Selected
0	0	400 Hz, 3-Pole
0	1	400 Hz, 4-Pole
1	0	Reserved
1	1	Reserved

3.1.4.3 TimeSlot Selection Bits (TIMESLOTx[9:0])

The timeslot selection bits select the time slot(s) to be used for data transmission. Reference Section 4.5 for details regarding PSI5 transmission modes and time slots. Accepted time slot values are 0.5 µs to 511.5 µs in 0.5 µs increments. Care must be taken to prevent from programming time slots which violate the PSI5 Version 1.3 specification, or time slots which will cause data contention.

TIMESLOTx[9:0]	ASYNC Bit	Time Slot	Reference
00 0000 0000	0	Default Time Slot ($t_{TIMESLOT\_DFLT}$) from start of Sync Pulse (t_{TRIG})	Section 4.5
	1	Asynchronous Mode	Section 4.5.1.1
Non-Zero	N/A	TimeSlot Definition from start of Sync Pulse (t_{TRIG}) in 0.5µs Increments	Section 4.5

Note: TIMESLOTB is only used for Synchronous Double Sample Rate Mode and 16-Bit Resolution Mode.

3.1.5 Device Configuration Registers 6, 7, and 8 (DEVCFG6, DEVCFG7, DEVCFG8)

Device configuration registers 6, 7 and 8 are user programmable OTP registers which contain device configuration and user specific manufacturing information. The user specific manufacturing information bits have no impact on the performance, but are transmitted during the PSI5 initialization phase 2 in 10-bit mode.

Location		Bit							
Address	Register	7	6	5	4	3	2	1	0
$09	DEVCFG6	INIT2_EXT	ASYNC	U_DIR[1]	U_DIR[0]	U_REV[3]	U_REV[2]	U_REV[1]	U_REV[0]
$0A	DEVCFG7	MONTH[3]	MONTH[2]	MONTH[1]	MONTH[0]	YEAR[3]	YEAR[2]	YEAR[1]	YEAR[0]
$0B	DEVCFG8	UD[2]	UD[1]	UD[0]	DAY[4]	DAY[3]	DAY[2]	DAY[1]	DAY[0]
Factory Default		0	0	0	0	0	0	0	0

3.1.5.1 Initialization Phase 2 Data Extension Bit (INIT2_EXT)

The initialization phase 2 data extension bit enables or disables data transmission in data fields D27 through D32 of PSI5 Initialization Phase 2 as shown below.

INIT2_EXT	Description
0	D27 through D32 are set to “0000”
1	D27 through D32 are transmitted as defined in Section 4.4.2.1

3.1.5.2 Asynchronous Mode Bit (ASYNC)

The asynchronous mode bit enables asynchronous data transmission as described in Section 3.1.4.3.

3.1.5.3 User Sensing Direction (U_DIR[1:0])

The user sensing direction registers are user programmable OTP registers which contain the module level sensing direction. This data is transmitted to the main ECU during PSI5 initialization phase 2 in 10-bit mode, as described in Section 4.4.2.1.

U_DIR[1]	U_DIR[0]	Module Sensing Direction As Defined in AKLV27	PSI5 Init Data Transmission (D8) Reference Table 11
0	0	Connector Direction (β)	0000
0	1	Bushing Direction (α)	0100
1	0	Perpendicular to α and β (γ)	1000
1	1	Not used	1100

3.1.5.4 User Product Revision (U_REV[3:0])

The user product revision registers are user programmable OTP registers which contain the module production revision. The device supports up to 16 product revisions. This data is transmitted to the main ECU during PSI5 initialization phase 2 in 10-bit mode, as described in Section 4.4.2.1.

3.1.5.5 User Production Date Information (YEAR[3:0], MONTH[3:0], DAY[4:0)

The user production date information registers are user programmable OTP registers which contain the module production date. The table below shows the relationship between the stored values and the production date.

Programmed Value	Decoded Value	Julian Date Value
YEAR[3:0]	Year	JY[6:0]
0000	2009	0001001
• • •	• • •	• • •
1111	2024	0011000
MONTH[3:0]	Month	JM[3:0]
0000	N/A	0000
0001	January	0001
• • •	• • •	• • •
1100	December	1100
• • •	• • •	• • •
1111	N/A	N/A
DAY[4:0]	Day	JD[4:0]
00000	N/A	00000
00001	Day 1	00001
• • •	• • •	• • •
11111	Day 31	11111

The Julian date value is transmitted to the main ECU during PSI5 initialization phase 2 in 10-bit mode, as described in Section 4.4.2.2.

3.1.5.6 User Specific Data (UD[2:0])

The user specific data bits are user programmable OTP bits. These bits have no impact on device operation or performance.

3.1.6 Status Check Register (SC)

The status check register is a read-only register containing device status information.

Location		Bit							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0C	SC	0	TM_B	RESERVED	IDEN_B	OC_INIT_B	IDEF_B	OFF_B	0

3.1.6.1 Test Mode Flag (TM_B)

The test mode bit is cleared if the device is in test mode.

TM_B	Operating Mode
0	Test Mode is active
1	Test Mode is not active

3.1.6.2 Internal Data Error Flag (IDEN_B)

The internal data error bit is cleared if a register data error detection mismatch is detected in the user accessible OTP array. A device reset is required to clear the error.

IDEN_B	Error Condition
0	Error detection mismatch in user programmable OTP array
1	No error detected

3.1.6.3 Offset Cancellation Init Status Flag (OC_INIT_B)

The offset cancellation initialization status bit is set once the offset cancellation initialization process is complete, and the filter has switched to normal mode.

OC_INIT_B	Error Condition
0	Offset Cancellation in initialization
1	Offset Cancellation initialization complete (t_{OC1} and t_{OC2} expired)

3.1.6.4 Internal Factory Data Error Flag (IDEF_B)

The internal factory data error bit is cleared if a register data CRC fault is detected in the factory programmable OTP array. A device reset is required to clear the error.

IDEF_B	Error Condition
0	CRC error in factory programmable OTP array
1	No error detected

3.1.6.5 Offset Error Flag (OFF_B)

The offset error flag is cleared if the acceleration signal reaches the offset limit.

OFF_B	Error Condition
0	Offset error detected
1	No error detected

3.1.7 Manufacturer ID (MFG_ID)

The manufacturer ID register is a user programmable OTP register that contains the PSI5 manufacturer ID. The manufacturer ID register has no impact on the performance, but is transmitted during the PSI5 initialization phase 2 in 10-bit mode.

Location		**Bit**							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0D	MFG_ID	MFG_ID[7]	MFG_ID[6]	MFG_ID[5]	MFG_ID[5]	MFG_ID[3]	MFG_ID[2]	MFG_ID[1]	MFG_ID[0]
Factory Default		0	0	0	0	0	0	0	0

3.2 OTP Array Error Detection

3.2.1 Factory Programmed OTP Array CRC Verification

The Factory programmed OTP array is verified for errors with a 3-bit CRC. The CRC verification is enabled only when the factory programmed array is locked. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = ‘111’.

Once the CRC verification is enabled, the CRC is continuously calculated on all bits in registers $00, $01, $02, $03, and $04 and on the factory programmable device configuration bits with the exception of the factory lock bit. Bits are fed in from right to left (LSB first), and top to bottom (lower addresses first) in the register map. The calculated CRC is then compared against the stored 3 bit CRC. If a CRC error is detected in the OTP array, the IDEF_B bit is cleared in the SC register.

The CRC verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.2.2 User Programmable OTP Array Error Detection

The user programmable OTP array is independently verified for errors. The Error Detection is enabled only when the LOCK_U bit in the user data register array is set.

When a PSI5 Programming Mode “Execute Programming of NVM” command is received and the LOCK_U bit is set, the device calculates the error detection code and writes the code to NVM, enabling the Error Detection.

Once the error detection is enabled, the error detection code is continuously calculated on all bits in registers $05, $06, $07, $08, $09, $0A, $0B and $0D with the exception of the LOCK_U bit. The calculated code is then compared against the stored error code. If a mismatch is detected, the IDEN_B bit is cleared in the SC register.

The error detection is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.3 Voltage Regulators

The device derives its internal supply voltage from the V_{CC} and V_{SS} pins. Separate internal voltage regulators are used for the analog (V_{REGA}) and digital circuitry (V_{REG}). The analog and digital regulators are supplied by a buffer regulator (V_{BUF}) to provide immunity from EMC and supply dropouts on V_{CC}. External filter capacitors are required, as shown in Figure 1.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the internal voltages have increased above the undervoltage detection thresholds. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below the undervoltage detection thresholds. A reference generator provides a reference voltage for the ΣΔ converter.

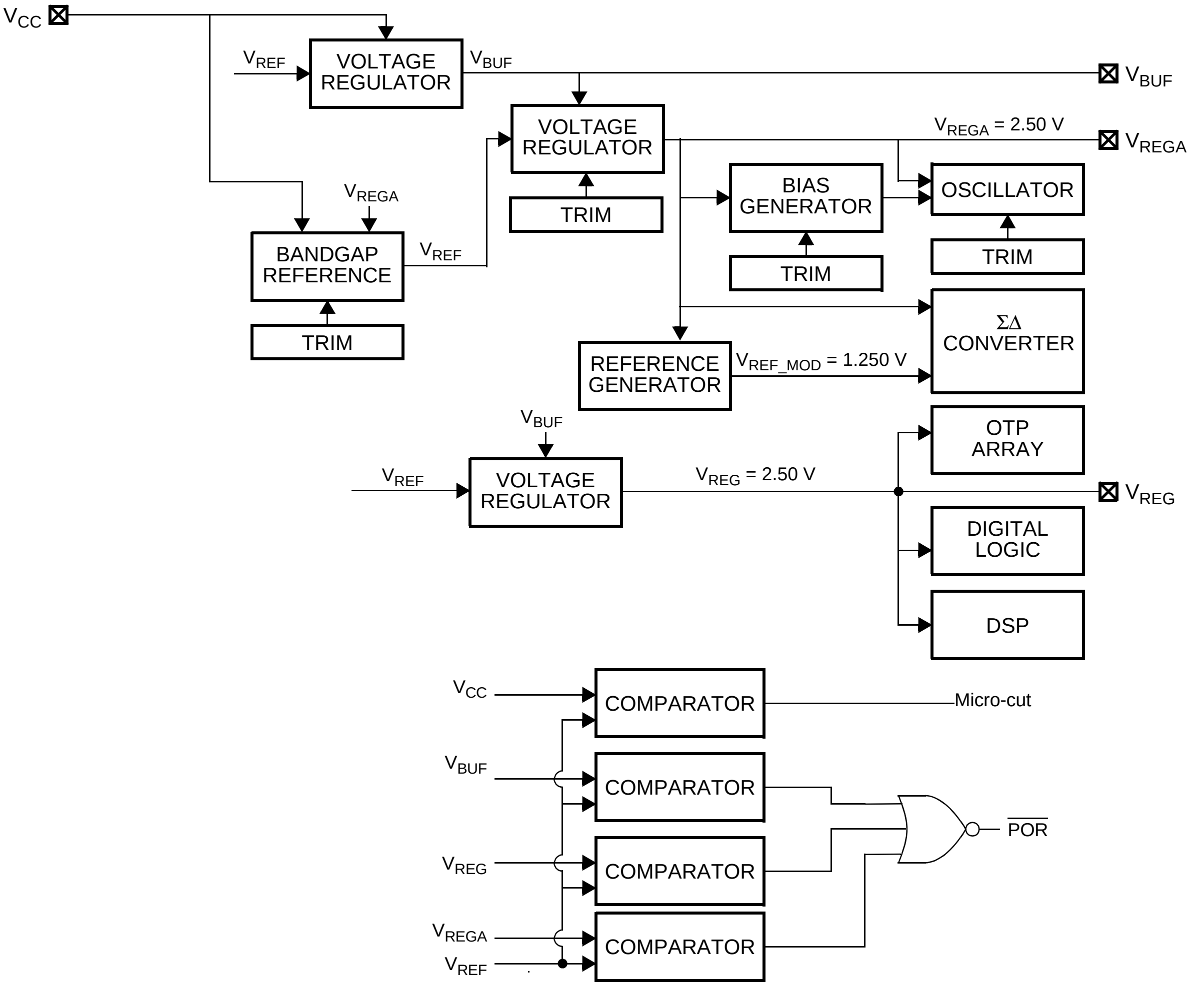


Figure 8. Voltage Regulation and Monitoring

3.3.1 V_{BUF}, V_{REG}, and V_{REGA} Regulator Capacitor

The internal regulators require an external capacitor between each of the regulator pins (V_{BUF}, V_{REG}, or V_{REGA}) and the associated the V_{SS} / V_{SSA} pin for stability. Figure 1 shows the recommended types and values for each of these capacitors.

3.3.2 V_{CC}, V_{BUF}, V_{REG}, and V_{REGA} Undervoltage Monitor

A circuit is incorporated to monitor the supply voltage (V_{CC}) and all internally regulated voltages (V_{BUF}, V_{REG}, and V_{REGA}). If any of internal regulator voltages fall below the specified undervoltage thresholds in Section 2, the device will be reset. If V_{CC} falls below the specified threshold, PSI5 transmissions are terminated for the present response. Once the supply returns above the threshold, the device will respond to the next detected sync pulse. Reference Figure 9.

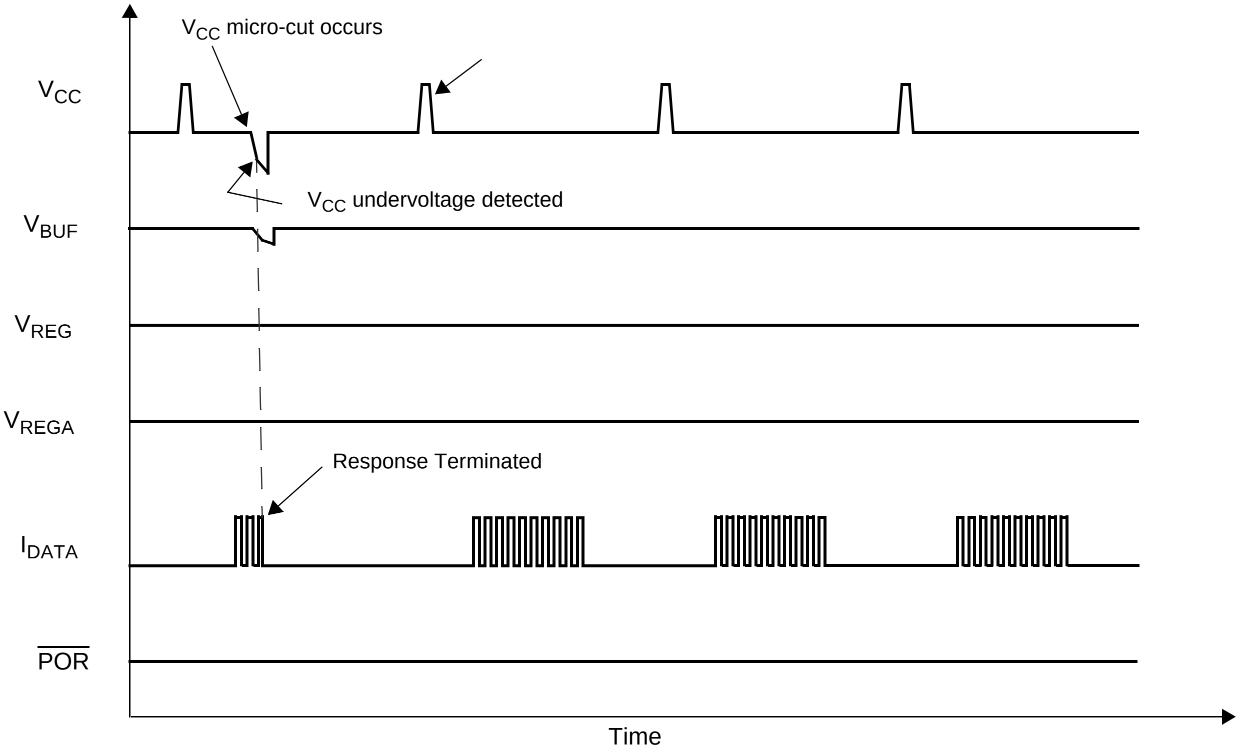


Figure 9. V_{CC} Micro-Cut Response

3.3.3 V_{BUF}, V_{REG}, and V_{REGA} Capacitance Monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external V_{BUF}, V_{REG}, or V_{REGA}, capacitor becomes open.

In asynchronous mode, the V_{BUF} regulator is disabled $t_{CAPTEST\_ADLY}$ seconds after each data transmission for a duration of $t_{CAPTEST\_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

In synchronous mode, the V_{BUF} regulator is disabled $t_{CAPTEST\_SDLY}$ seconds after each sync pulse for a duration of $t_{CAPTEST\_TIME}$ seconds. If the external capacitor is not present, the regulator voltage will fall below the internal reset threshold, forcing a device reset.

The V_{REG} and V_{REGA} regulators are disabled at a continuous rate ($t_{CAPTEST\_RATE}$), for a duration of $t_{CAPTEST\_TIME}$ seconds. If either external capacitor is not present, the associated regulator voltage will fall below the internal reset threshold, forcing a device reset.

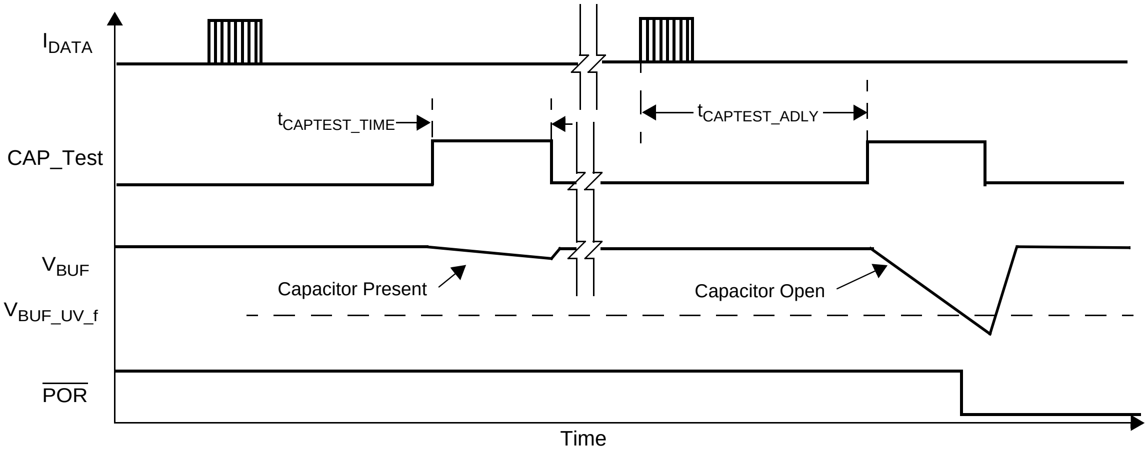


Figure 10. V_{BUF} Capacitor Monitor - Asynchronous Mode

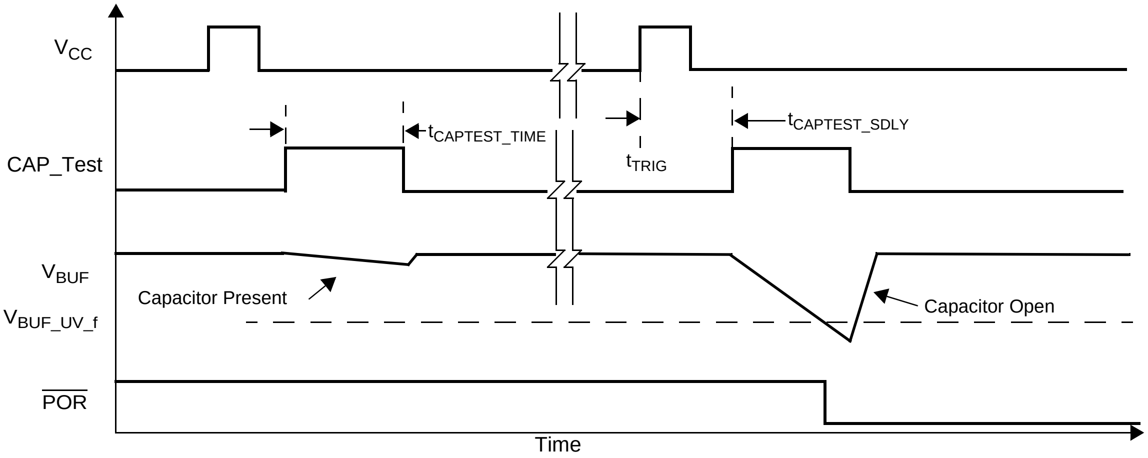


Figure 11. V_{BUF} Capacitor Monitor - Synchronous Mode

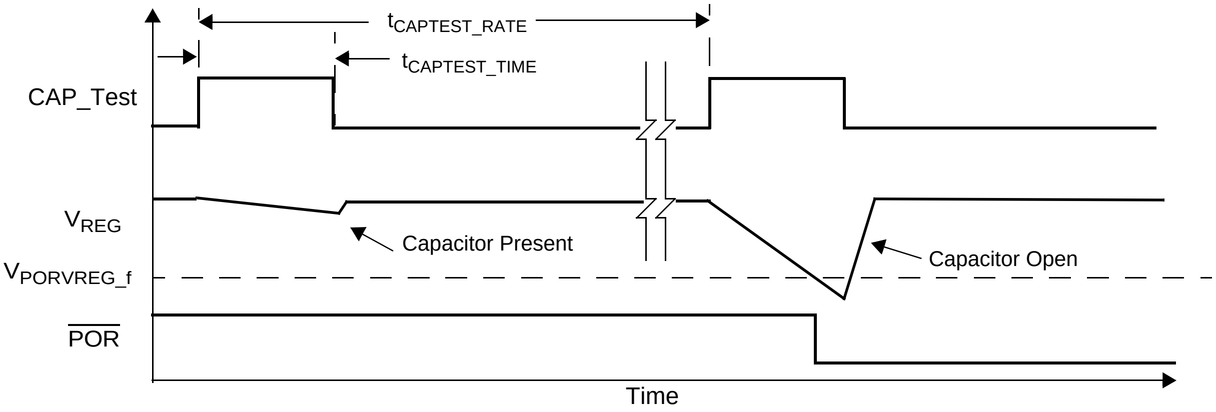


Figure 12. V_{REG} Capacitor Monitor

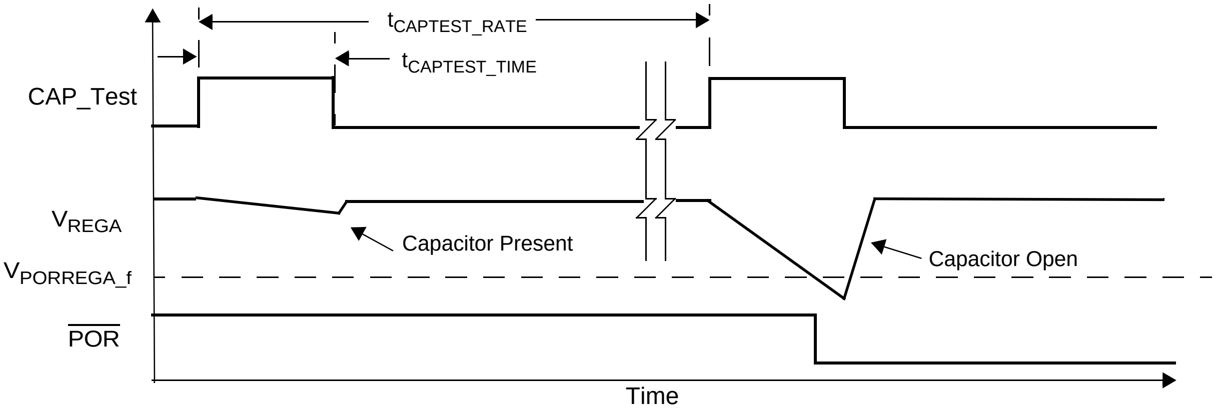


Figure 13. V_{REGA} Capacitor Monitor

3.4 Internal Oscillator

A factory trimmed oscillator is included as specified in Section 2.

3.5 Acceleration Signal Path

3.5.1 Transducer

The transducer is an overdamped mass-spring-damper system defined by the following transfer function:

where:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

ζ = Damping Ratio

ω_n = Natural Frequency = $2 * \Pi * f_n$

Reference Section 2.7 for transducer parameters.

3.5.2 ΣΔ Converter

A sigma delta modulator converts the differential capacitance of the transducer to a 1 MHz data stream that is input to the DSP block.

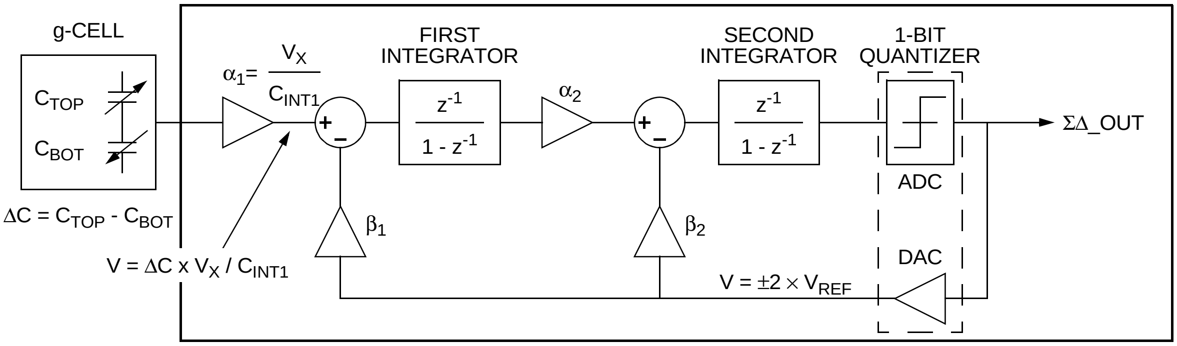


Figure 14. ΣΔ Converter Block Diagram

3.5.3 Digital Signal Processing Block

A Digital Signal Processing (DSP) block is used to perform signal filtering and compensation. A diagram illustrating the signal processing flow within the DSP block is shown in Figure 15.

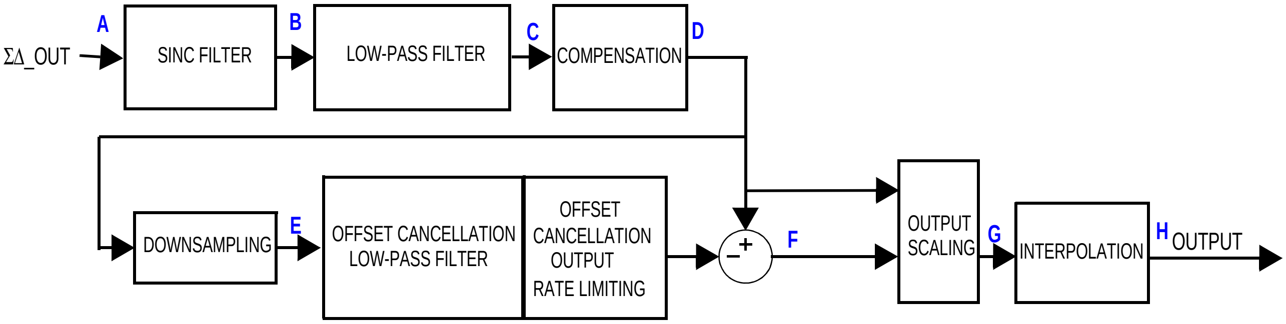


Figure 15. Signal Chain Diagram

Table 4. Signal Chain Characteristics

	Description	Sample Time (µs)	Data Width (Bits)	Over Range (Bits	Signal Width (Bits)	Signal Noise (Bits)	Signal Margin (Bits)	Typical Block Latency	Reference
A	SD	1	1		1			$203/f_{osc}$	Section 3.5.2
B	SINC Filter	16	20		13				Section 3.5.3.2
C	Low-Pass Filter	16	26	4	10	3	9	Reference Section 3.5.3.2	Section 3.5.3.2
D	Compensation	16	26	4	10	3	9	$68/f_{osc}$	
E	Down Sampling	16	26	4	10	3	9		
F	High Pass Filter	16	26	4	10	3	9	Reference Section 3.5.3.3	Section 3.5.3.3
G	DSP Sampling 10-Bit Output Scaling	16			10			$4/f_{osc}$	Section 3.5.3.5
H	Interpolation	1			10			$64/f_{osc}$	Section 3.5.3.5

3.5.3.1 Decimation Sinc Filter

The serial data stream produced by the ΣΔ converter is decimated and converted to parallel values by a 3rd order 16:1 sinc filter with a decimation factor of 16.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})}\right]^3$$

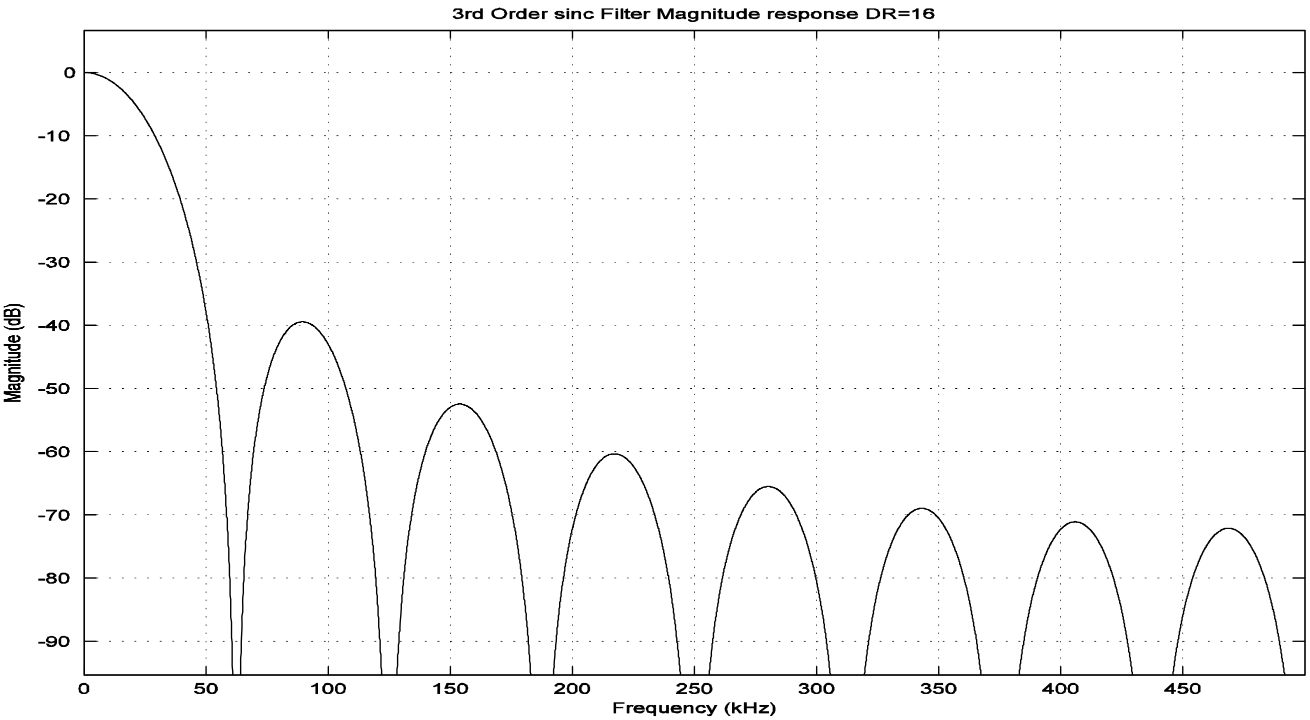


Figure 16. Sinc Filter Response, $t_S = 16\ \mu s$

3.5.3.2 Low-Pass Filter

Data from the Sinc filter is processed by an infinite impulse response (IIR) low-pass filter.

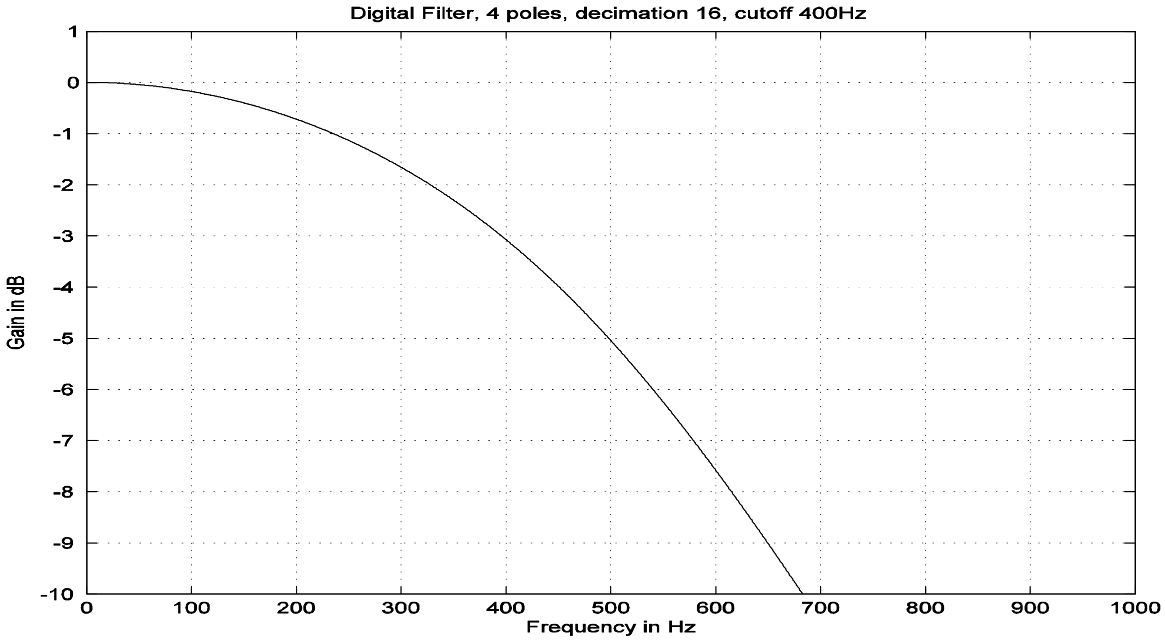
$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^{0}) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^{0}) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^{0}) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{11} \cdot z^{0}) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})}$$

The device provides the option for one of two low-pass filters. The filter is selected with the LPF[1:0] bits in the DEVCFG3 register. The filter selection options are listed in Section 3.1.4.2. Response parameters for the low-pass filter are specified in Section 2.7. Filter characteristics are illustrated in Figure 17 and Figure 18.

Table 5. Low-Pass Filter Coefficients

Description	Filter Coefficients				Group Delay
400 Hz, 3-Pole LPF	a_0	5.189235225042199e-02			2816/f_{osc}
	n_{11}	1.629077582099646e-03	d_{11}	1.0	
	n_{12}	1.630351547919014e-03	d_{12}	-9.481076477495780e-01	
	n_{13}	0	d_{13}	0	
	n_{21}	2.500977520825902e-01	d_{21}	1.0	
	n_{22}	4.999999235890745e-01	d_{22}	-1.915847097557409e+00	
	n_{23}	2.499023243303036e-01	d_{23}	9.191065266874253e-01	
400 Hz, 4-Pole LPF	a_0	3.143225986084408e-03			3392/f_{osc}
	n_{11}	9.951105668343345e-04	d_{11}	1.0	
	n_{12}	2.003487780064749e-03	d_{12}	-1.892328151433503e+00	
	n_{13}	1.008466113720278e-03	d_{13}	8.954713774195870e-01	
	n_{21}	2.516720624825626e-01	d_{21}	1.0	
	n_{22}	4.999888752940916e-01	d_{22}	-1.918978239761011e+00	
	n_{23}	2.483390622233452e-01	d_{23}	9.229853042218408e-01	

Note: Low-Pass Filter values do not include g-cell frequency response.



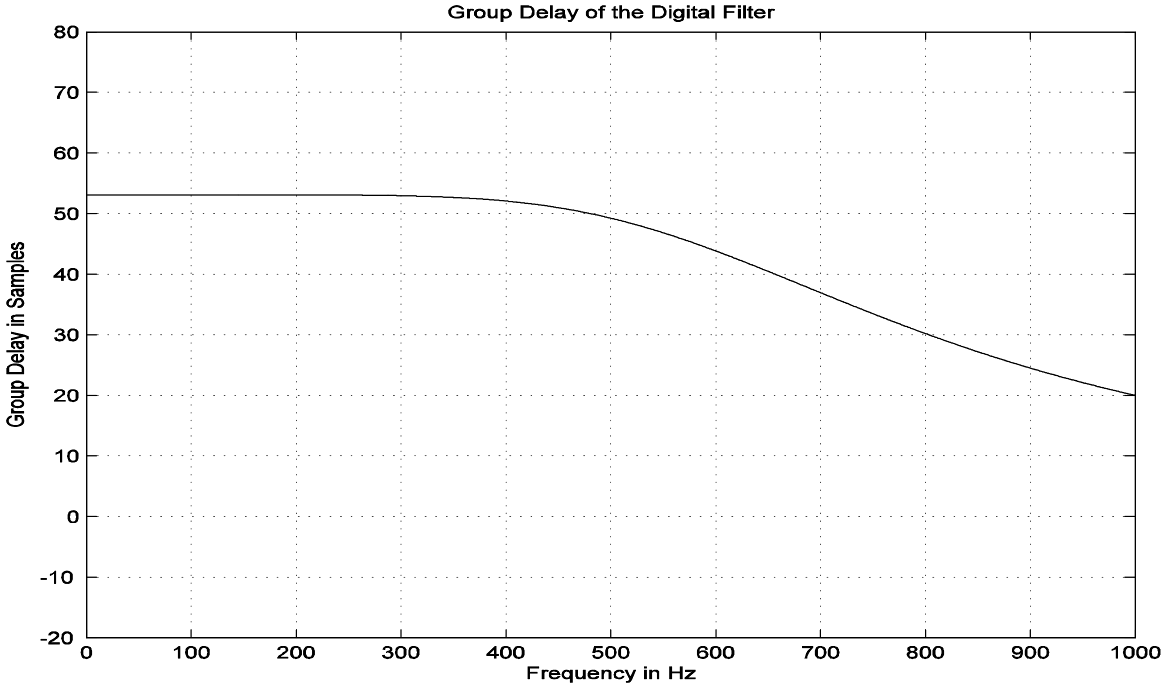


Figure 17. Low-Pass Filter Characteristics: f_C = 400 Hz, 4-Pole, t_S = 16 µs

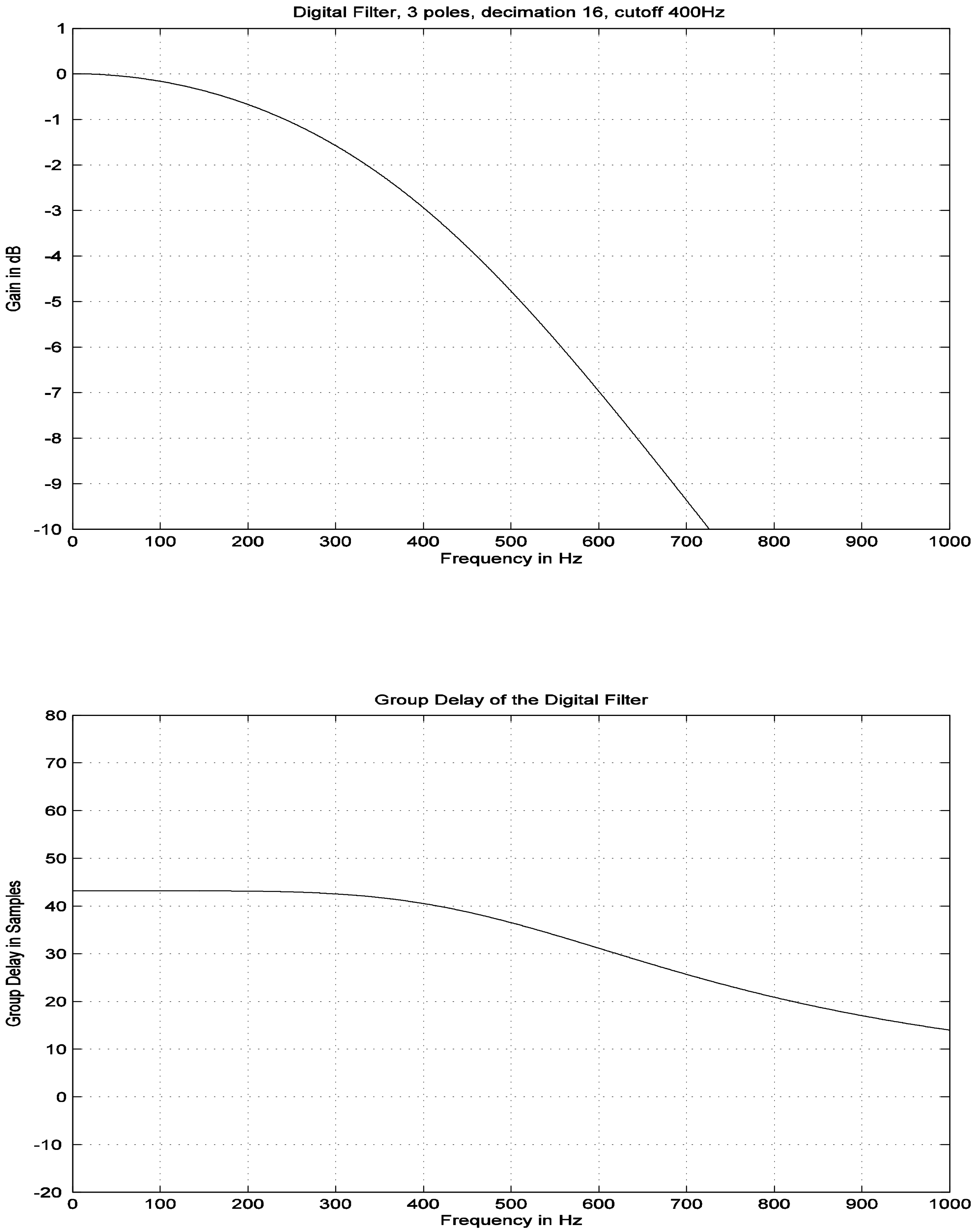


Figure 18. Low-Pass Filter Characteristics: f_C = 400 Hz, 3-Pole, t_S = 16 µs

3.5.3.3 Offset Cancellation

The device provides an optional offset cancellation circuit to remove internal offset error. A block diagram of the offset cancellation is shown in Figure 19.

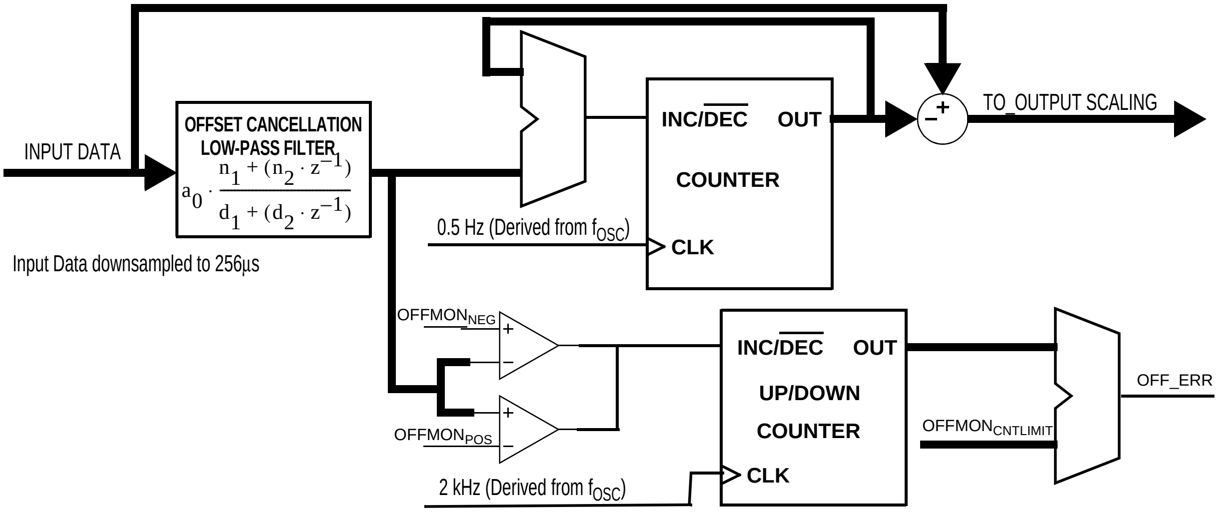


Figure 19. Offset Cancellation Block Diagram

The transfer function for the offset LPF is:

$$H(z) = ao_0 \cdot \frac{no_1 + (no_2 \cdot z^{-1})}{do_1 + (do_2 \cdot z^{-1})}$$

Response parameters are specified in Section 2 and the offset LPF coefficients are specified in Table 7.

During startup, two phases of the offset LPF are used to allow for fast convergence of the internal offset error during initialization. The timing and characteristics of each phase are shown in Table 6 and Table 7 and specified in Section 2. For more information regarding the startup timing, reference the PSI5 initialization information in Section 4.4. The offset low-pass filter used in normal operation is selected by the OC_FILT bit as shown in Table 6.

During the Initialization Self-Test phase, the offset cancellation circuit output value is frozen.

During normal operation, output rate limiting is applied to the output of the high pass filter. Rate limiting updates the offset cancellation output by OFF_{Step_xx} LSB every $t_{OffRate\_xx}$ seconds.

Table 6. Offset Cancellation Startup Characteristics and Timing

Offset Cancellation Startup Phase	Offset LPF	Output Rate Limiting	Total Time for Phase
1	10 Hz	Bypassed	80 ms
2	0.3 Hz	Bypassed	70 ms
Self-Test	0.3 Hz	Bypassed (Frozen during ST2)	96 ms per Self-Test Sequence (up to 6 repeats)
Complete	0.1 Hz	Enabled	N/A

Table 7. High Pass Filter Coefficients

Description	Coefficients				Group Delay
10 Hz HPF	ao_0	0.015956938266754			16.384 ms
	no_1	0.499998132328277	do_1	1.0	
	no_2	0.499998132328277	do_2	-0.984043061733246	
0.3 Hz HPF	ao_0	0.000482380390167			537.6 ms
	no_1	0.499938218213271	do_1	1.0	
	no_2	0.499938218213271	do_2	-0.999517619609833	
0.1 Hz HPF	ao_0	0.0001608133316040			1591ms
	no_1	0.4999999403953552	do_1	1.0	
	no_2	0.4999999403953552	do_2	-0.9998391270637512	

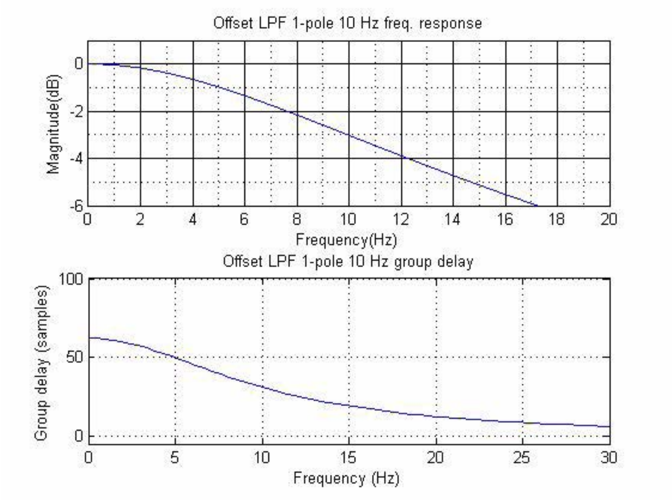


Figure 20. 10 Hz Offset Cancellation Low-Pass Filter Characteristics

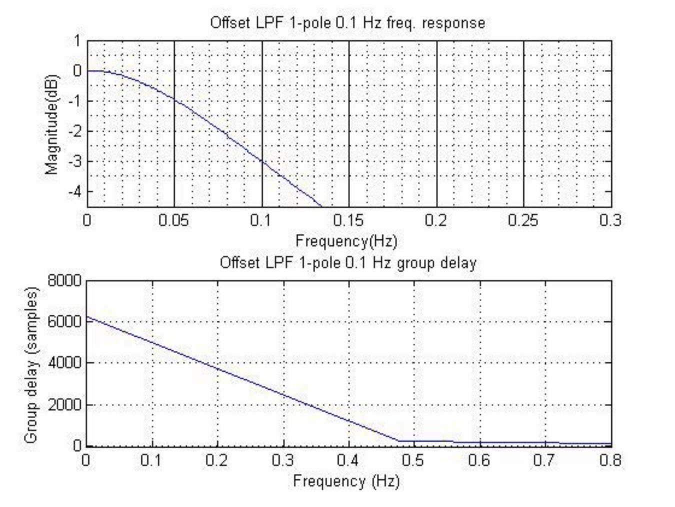


Figure 21. 0.1 Hz Offset Cancellation Low-Pass Filter Characteristics

3.5.3.4 Offset Monitor

The device includes an offset monitor circuit. The output of the single pole low-pass filter in the offset cancellation block is continuously monitored against the offset limits specified in Section 2.4. An up/down counter is employed to count up If the output exceeds the limits, and to count down if the output is within the limits. The output of the counter is compared against the count limit $OFFMON_{CNTLIMIT}$. If the counter exceeds the limit, the OFF_B flag in the SC register is cleared. The counter rails once the max counter value is reached ($OFFMON_{CNTSIZE}$). The offset monitor is disabled during Initialization Phase 1, Phase 2, and Phase 3.

3.5.3.5 Data Interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. On detection of a sync pulse the transmitted data is interpolated from the two previous samples, resulting in a latency of one sample time, and a maximum signal jitter of ±1/16 of a sample time. Reference Section 4.5 for more information regarding interpolation and data latency.

3.5.3.6 Output Scaling

The 26-bit digital output from the DSP is clipped and scaled to a 10-bit or 8-bit word which spans the acceleration range of the device. Figure 22 shows the method used to establish the output acceleration data word from the 26-bit DSP output.

Over Range			**Signal**										**Noise**				**Margin**				
D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	...	D2	D1	D0
8-bit Data Word				D21	D20	D19	D18	D17	D16	D15	D14	Using Rounding									
10-bit Data Word				D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	Using Rounding							

Figure 22. 10-Bit Output Scaling Diagram

3.5.3.7 PCM Output Function

The device provides the option for a PCM output function. The PCM output is activated if the PCM bit is set in the DEVCFG2 register. When the PCM function is enabled, a 4 MHz Pulse Code Modulated signal proportional to the upper 9 bits of the 10-bit acceleration response is output onto the PCM pin. The PCM output is intended for test use only.

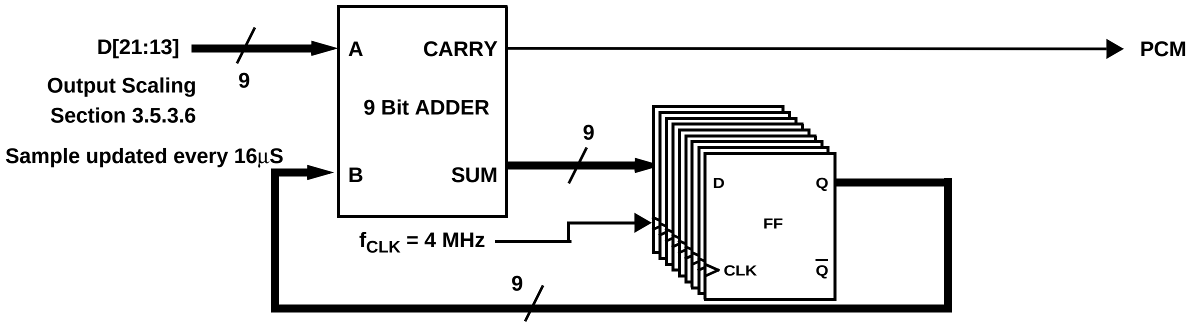


Figure 23. PCM Output Function Block Diagram

3.6 Overload Response

3.6.1 Overload Performance

The device is designed to operate within a specified range. Acceleration beyond that range (overload) impacts the output of the sensor. Acceleration beyond the range of the device can generate a DC shift at the output of the device that is dependent upon the overload frequency and amplitude. The g-cell is overdamped, providing the optimal design for overload performance. However, the performance of the device during an overload condition is affected by many other parameters, including:

- g-cell damping
- Non-linearity
- Clipping limits
- Symmetry

Figure 24 shows the g-cell, ADC and output clipping of The device over frequency. The relevant parameters are specified in Section 2.

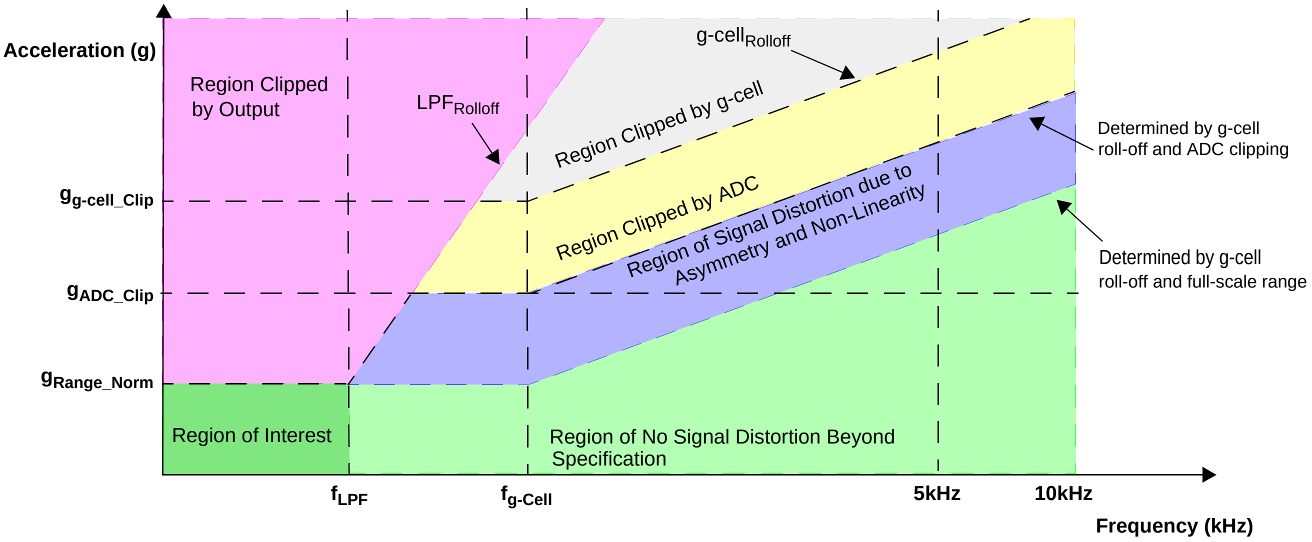


Figure 24. Output Clipping vs. Frequency

3.6.2 Sigma Delta Modulator Over Range Response

Over Range conditions exist when the signal level is beyond the full-scale range of the device but within the computational limits of the DSP. The ΣΔ converter can saturate at levels above those specified in Section 2 (G_{ADC_CLIP}). The DSP operates predictably under all cases of over range, although the signal may include residual high frequency components for some time after returning to the normal range of operation due to non-linear effects of the sensor.

4 PSI5 Layer and Protocol

4.1 Communication Interface Overview

The communication interface between a master device and the MMA52xxLW is established via a PSI5 compatible 2-wire interface, with parallel or serial (daisy-chain) connections to the satellite modules. Figure 25 shows one possible system configuration for multiple satellite modules in parallel.

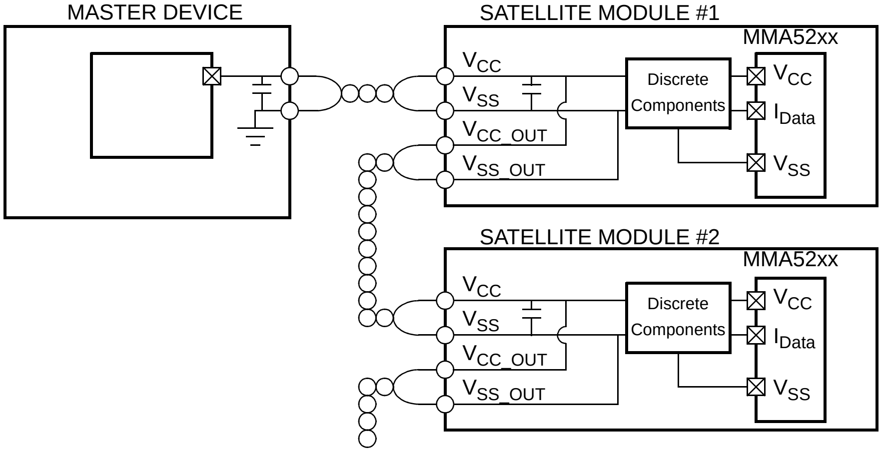


Figure 25. PSI5 Satellite Interface Diagram

4.2 Data Transmission Physical Layer

The device uses a two wire interface for both its power supply (V_{CC}), and data transmission. The PSI5 master supplies a pre-regulated voltage. Data transmissions and synchronization control from the PSI5 master to the device are accomplished via modulation of the supply voltage. Data transmissions from the device to the PSI5 master are accomplished via modulation of the current on the power supply line.

4.2.1 Synchronization Pulse

The PSI5 master modulates the supply voltage in the positive direction to provide synchronization of the satellite sensor data. Upon reception of a synchronization pulse, the device delays a specified period of time, called a time slot, before transmitting acceleration data. For more details regarding time slots, refer to Section 3.1.4, and Section 4.5.

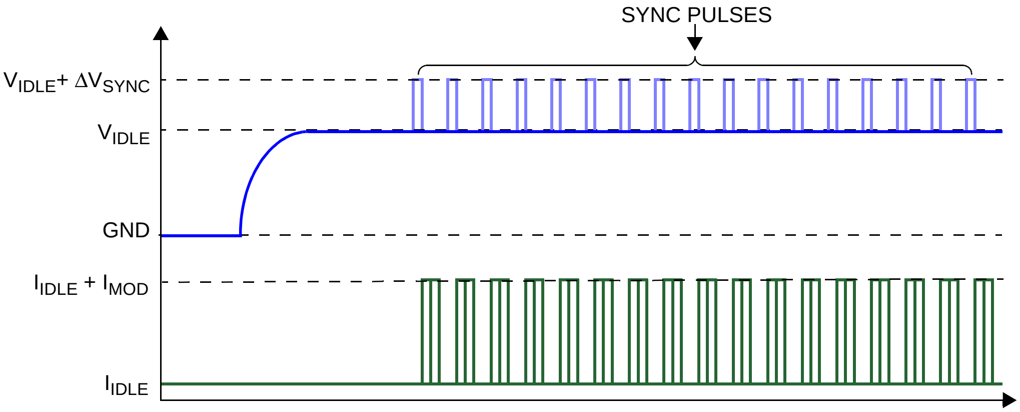


Figure 26. Synchronous Communication Overview

4.2.1.1 Synchronization Pulse Detection

The Synchronization (Sync) pulse detection block generates a valid synchronization pulse signal following the detection of an externally generated Sync pulse. This signal resets the Sync pulse time reference (t_{TRIG}), and initiates the timers associated with response messages.

The supply voltage can vary throughout the specified range, so the external Sync pulses may have different absolute voltage levels. Thus, the Sync pulse detection threshold (V_{CC_SYNC}) is dependent not only on the Sync pulse absolute voltage, but also on the supply voltage. Figure 27 shows a block diagram of the Sync pulse detection circuit.

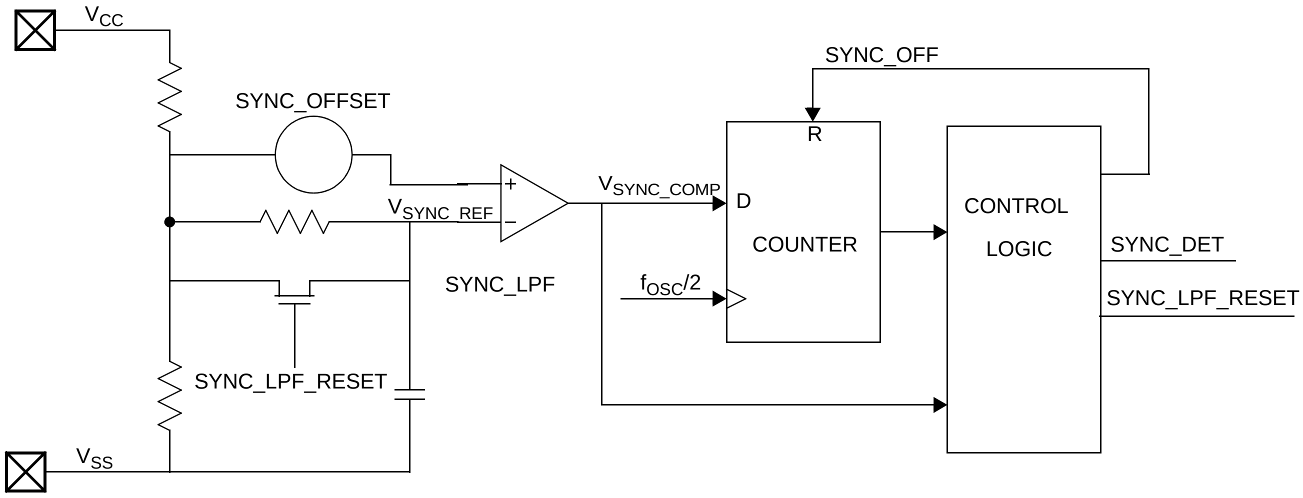


Figure 27. Synchronization Pulse Detection Circuit

The start of a Sync pulse is detected when the comparator output is set (V_{SYNC} exceeds V_{SYNC_REF}). The comparator output is input into a counter, and the counter is updated at a fixed frequency of $f_{OSC}/2$. At a fixed time after the initial sync pulse detection ($t_{SYNC\_LPF\_RST\_ST}$), the counter is compared against a limit (the minimum value of t_{SYNC}). If the counter is above the limit, a valid sync pulse is detected.

If the Sync pulse is valid, the following occur:

1. The valid Sync pulse detection signal is set.
2. The detection counter is reset and disabled for t_{SYNC_OFF} (referenced from t_{TRIG}). t_{SYNC_OFF} is a user programmable option. Reference Section 3.1.3.6 for details on the selectable option, and Section 2.6 for timing specifications for each option.
    a. If BLANKTIME = ‘0’, $t_{SYNC\_OFF} = t_{SYNC\_OFF\_500}$
    b. If BLANKTIME = ‘1’, $t_{SYNC\_OFF}=t_{SYNC\_OFF\_VAR}= t_{TIMESLOT\_DLYx}$ + (2+DATASIZE+(P_CRC?3:1)) *t_{BIT_x}
3. The Sync pulse detection low-pass filter is reset for a specified time ($t_{SYNC\_LPF\_RESET}$).

If the Sync pulse is invalid, all timers are reset, and the detector becomes sensitive for the very next f_{SYNC_DET} sample.

The output of the comparator is monitored at the $f_{OSC}/2$ frequency. Once the comparator output goes high, all of the internal timers are started, so that the t_{TRIG} jitter is minimized.

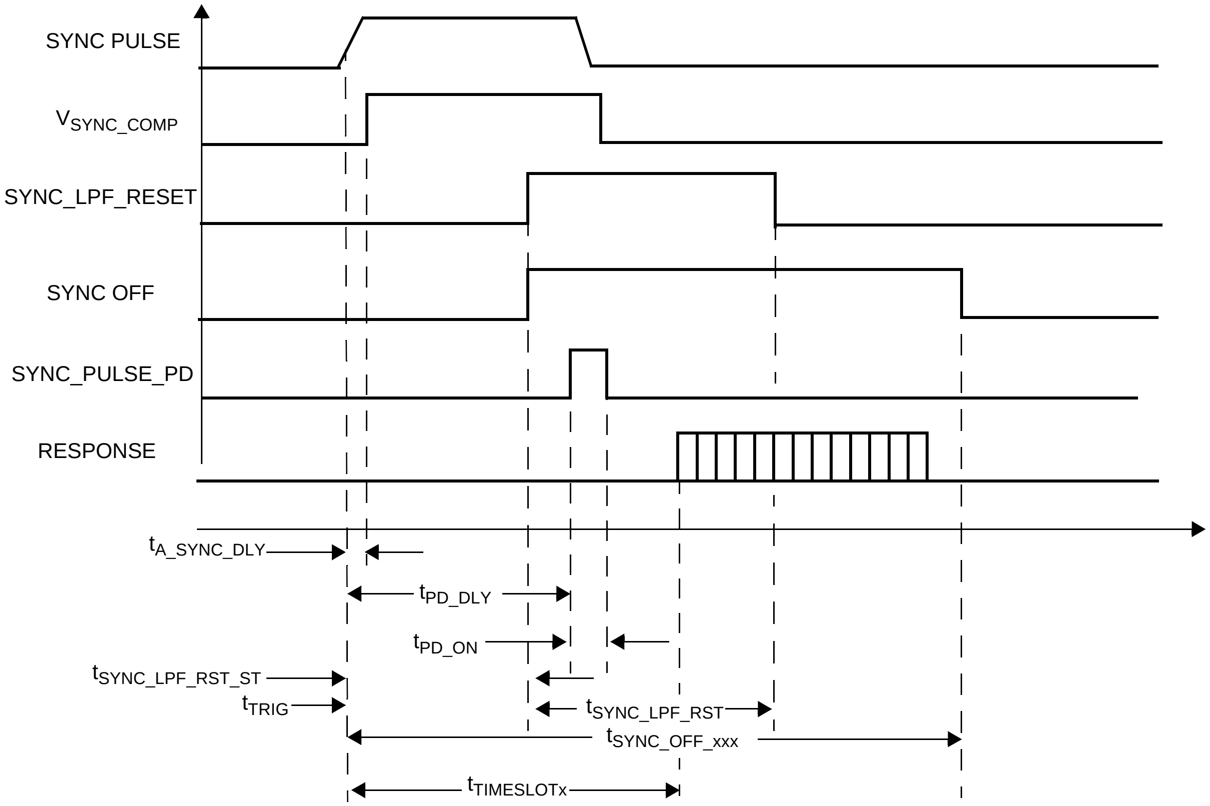


Figure 28. Synchronization Pulse Detection Timing

4.2.1.2 Synchronization Pulse Pulldown Function

The device includes an optional Sync pulse pulldown function for systems in which the master device does not include an active pulldown function. The modulation current pulldown circuit is used, which sinks I_{MOD}-I_{IDLE} additional current from the I_{DATA} pin. The pulldown current is activated after t_{PD_DLY} (referenced to t_{TRIG}), and is activated for t_{PD_ON}.

4.3 Data Transmission Data Link Layer

4.3.1 Bit Encoding

The device outputs data by modulation of the V_{CC} current using Manchester 2 Encoding. Data is stored in a transition occurring in the middle of the bit time. The signal idles at the normal quiescent supply current. A logic low is defined as an increase in current at the middle of a bit time. A logic high is defined as a decrease in current at the middle of a bit time. There is always a transition in the middle of the bit time. If consecutive “1” or “0” data are transmitted, There will also be a transition at the start of a bit time.

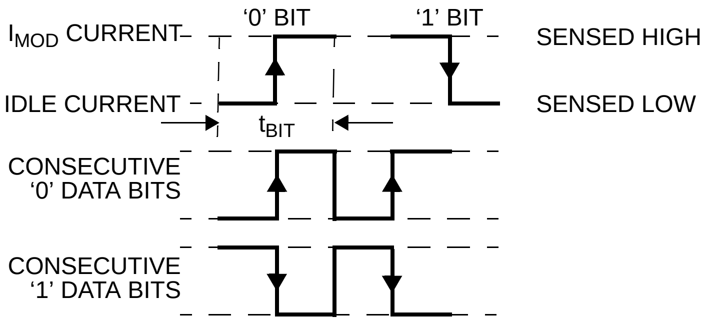


Figure 29. Manchester 2 Data Bit Encoding

4.3.2 Data Transmission

Transmission frames are composed of two start bits, an 8-Bit or 10-bit data word, and error detection bit(s). Data words are transmitted least-significant bit (LSB) first. A typical Manchester-encoded transmission frame is illustrated in Figure 30.

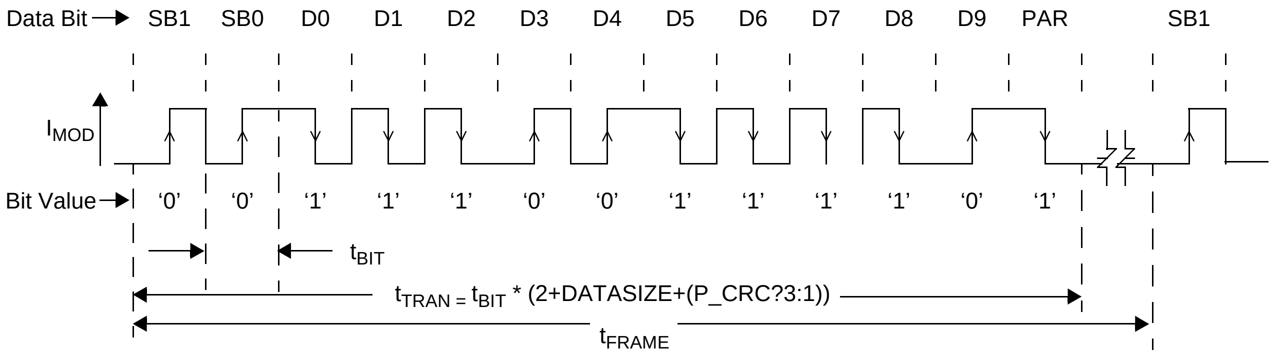


Figure 30. Example Manchester Encoded Data Transfer - PSI5-x10P

4.3.3 Error Detection

Error detection of the transmitted data is accomplished via either a parity bit, or a 3-Bit CRC. The type of error detection used is selected by the P_CRC bit in the DEVCFG register.

4.3.3.1 Parity Error Detection

When parity error detection is selected, even parity is employed. The number of logic '1' bits in the transmitted message must be an even number.

4.3.3.2 3-Bit CRC Error Detection

When CRC error detection is selected, a 3-bit CRC is appended to each response message. The 3-bit CRC uses a generator polynomial of $g(x) = X^3+X+1$, with a seed value = '111'. Data from the transmitted message is read into the CRC calculator LSB first, and the data is augmented with three '0's. Start bits are not used in the CRC calculation. Table 8 shows some example CRC calculation values for 10-bit data transmissions.

Table 8. PSI5 3-Bit CRC Calculation Examples

Data Transmitted											CRC		
HEX	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**C2**	**C1**	**C0**
0x000	0	0	0	0	0	0	0	0	0	0	1	1	0
0x0CC	0	0	1	1	0	0	1	1	0	0	0	1	1
0x151	0	1	0	1	0	1	0	0	0	1	0	0	0
0x1E0	0	1	1	1	1	0	0	0	0	0	0	1	1
0x1F4	0	1	1	1	1	1	0	1	0	0	0	1	0
0x220	1	0	0	0	1	0	0	0	0	0	1	0	0
0x275	1	0	0	1	1	1	0	1	0	1	1	1	1
0x333	1	1	0	0	1	1	0	0	1	1	0	0	1
0x3FF	1	1	1	1	1	1	1	1	1	1	1	0	0

4.3.4 Data Range Values

Table 10 shows the details for each data range.

Table 9. PSI5 Data Values

8-Bit Data Value		10-Bit Data Value		Description
Decimal	Hex	Decimal	Hex	
+127	$7F	+511	$1FF	Reserved
		• • •	• • •	
		+502	$1F6	
+126	$7E	+501	$1F5	
+125	$7D	+500	$1F4	Sensor Defect Error Message
N/A	N/A	+499	$1F3	Reserved
		• • •	• • •	
		+489	$1E9	
+124	$7C	+488	$1E8	Sensor Busy
+123	$7B	+487	$1E7	Sensor Ready
+122	$7A	+486	$1E6	Sensor Ready, but Unlocked
N/A	N/A	+485	$1E5	Reserved
		• • •	• • •	
+121	$79	+481	$1E1	
+120	$78	+480	$1E0	Maximum positive acceleration value
• • •	• • •	• • •	• • •	Positive acceleration values
+3	$03	+3	$03	
+2	$02	+2	$02	
+1	$01	+1	$01	
0	0	0	0	0g level
-1	$FF	-1	$3FF	Negative acceleration values
-2	$FE	-2	$3FE	
-3	$FD	-3	$3FD	
• • •	• • •	• • •	• • •	
-120	$88	-480	$220	Maximum negative acceleration value
-121	$87	-481	$21F	Initialization Data Codes 10-Bit Status Data Nibble 1 - 16 (0000 - 1111) (Dx) 8-Bit Status Data Nibble 1 - 4 (00 - 11) (Dx)
• • •	• • •	• • •	• • •	
-124	$84	-496	$210	
-125	$83	-497	$20F	Initialization Data IDs Block ID 1 - 16 (10-bit Mode) (IDx) Block ID 1 - 4 (8-Bit Mode) (IDx)
• • •	• • •	• • •	• • •	
-128	$80	-512	$200	

4.4 Initialization

Following powerup, the device proceeds through an initialization process which is divided into 3 phases:

- Initialization Phase 1: No Data transmissions occur
- Initialization Phase 2: Sensor self-test and transmission of configuration information
- Initialization Phase 3: Transmission of “Sensor Busy”, and “Sensor Ready” / “Sensor Defect” message

Once initialization is completed the device begins normal mode operation, which continues as long as the supply voltage remains within the specified limits.

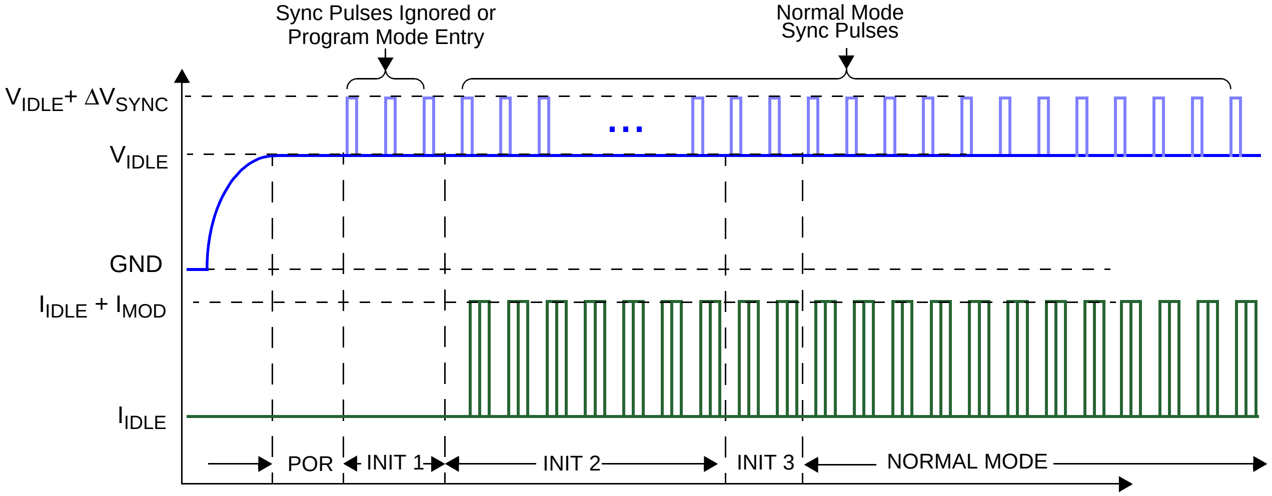


Figure 31. PSI5 Sensor 10-Bit Initialization

During PSI5 initialization, the device completes an internal initialization process consisting of the following:

- Power-on Reset
- Device Initialization
- Program Mode Entry Verification
- Offset Cancellation Initialization (2 Stages)
- Self-Test

Figure 32 shows the timing for internal and external initialization.

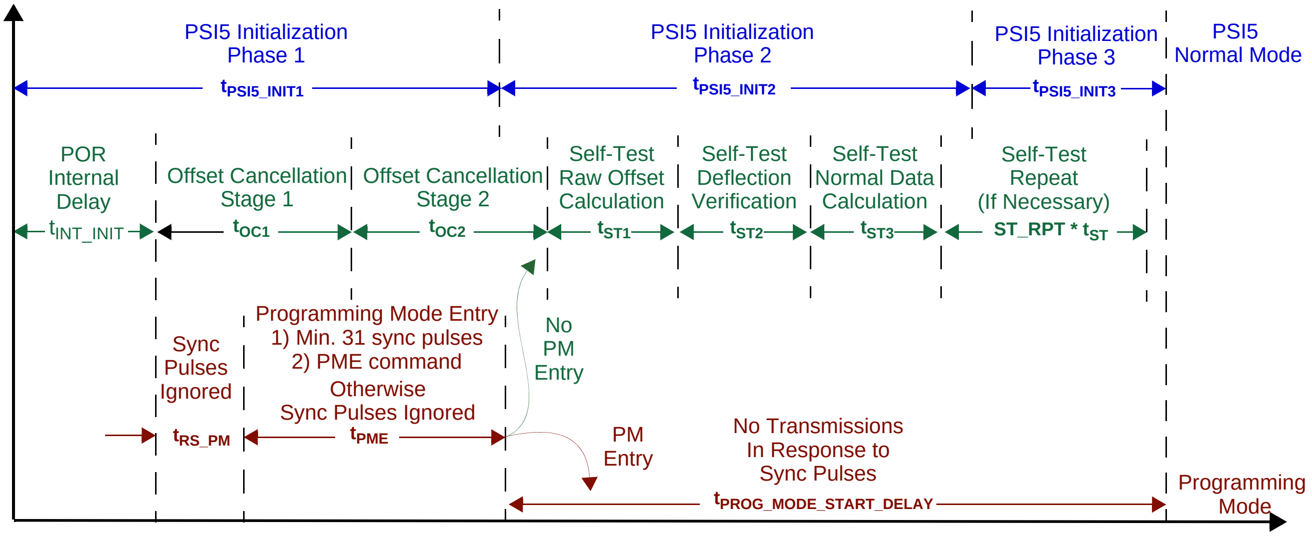


Figure 32. Initialization Timing

4.4.1 PSI5 Initialization Phase 1

During PSI5 initialization phase 1, the device begins internal initialization and self checks, but transmits no data. Initialization begins with the sequence below and shown in Figure 32:

- Internal Delay to ensure analog circuitry has stabilized (t_{INT_INIT})
- Offset Cancellation phase 1 Initialization (t_{OC1})
- Monitor for the Programming Mode Entry Sequence (t_{PME})
  - A sequence of sync pulses received during the program mode entry window in PSI5 initialization phase 1 will allow the device to enter into a PSI5 programming mode if the LOCK_U bit is not set. Reference Section 5.2 for details.
- Offset Cancellation phase 2 Initialization (t_{OC2})
- If the Programming Mode Entry Sequence is not detected, the device enters Initialization Phase 2 (t_{PSI5_INIT2})

4.4.2 PSI5 Initialization Phase 2

During PSI5 initialization phase 2, the device continues it's internal self checks and transmits the PSI5 initialization phase 2 data. The PSI5 initialization data transmission format varies depending on whether the device is programmed for 8-bit or 10-bit data. Initialization is transmitted using the initialization data codes and IDs specified in Table 13, and in the order shown in Figure 33 and Figure 34.

D1								D2								...	D32							
ID1$_1$	D1$_1$	ID1$_2$	D1$_2$	...	ID1$_k$	D1$_k$		ID2$_1$	D2$_1$	ID2$_2$	D2$_2$	...	ID2$_k$	D2$_k$		...	ID32$_1$	D32$_1$	ID32$_2$	D32$_2$	...	ID32$_k$	D32$_k$	
Repeat k times								Repeat k times								...	Repeat k times							

Figure 33. PSI5 Initialization Phase 2 Data Transmission Order (10-bit Mode)

D1							D2							...	D9						
ID1H$_1$	D1H$_1$	ID1H$_2$	D1H$_2$	...	ID1H$_k$	D1H$_k$	ID1L$_1$	D1L$_1$	ID1L$_2$	D1L$_2$	...	ID1L$_k$	D1L$_k$	...	ID9L$_1$	D9L$_1$	ID9L$_2$	D9L$_2$	...	ID9L$_k$	D9L$_k$
Repeat k times							Repeat k times							...	Repeat k times						

Figure 34. PSI5 Initialization Phase 2 Data Transmission Order (8-bit Mode)

The Initialization phase 2 time is calculated with the following equation:

$$t_{PHASE2} = TRANS_{NIBBLE} \times k \times (DataFields) \times t_{S-S}$$

where:

- $TRANS_{NIBBLE}$ = # of Transmissions per Data Nibble
  2 for 10-bit Data: 1 for ID, and 1 for Data
  4 for 8-bit Data: 2 for ID, and 2 for Data
- k = the repetition rate for the data fields
- Data Fields = 32 data fields for 10-bit data, 9 data fields for 8-bit data
- t_{S-S} = Sync Pulse Period

4.4.2.1 PSI5 Initialization Phase 2 (10-Bit Mode)

In PSI5 initialization phase 2, 10-bit mode, the device transmits a sequence of sensor specific configuration and serial number information. The transmission data is in conformance with the PSI5 specification, Revision 1.3 and AKLV27, Revision 1.10. The data content and transmission format is shown in Table 10 and Table 11. Table 10 shows the 10-bit phase 2 timing for different operating modes. Times are calculated using the equation in Section 4.4.2.

Table 10. Initialization Phase 2 Time (10-Bit Mode)

Operating Mode	Repetition Rate (k)	# of Transmissions	Nominal Phase 2 Time
Asynchronous Mode (228 µs)	8	512	116.7 ms
Synchronous Mode (500 µs)	4	256	128.0 ms

Table 11. PSI5 Initialization Phase 2 Data (10-Bit Mode)

PSI5 V1.2 Field ID #	PSI5 V1.2 Nibble ID #	Page Address	PSI5 Nibble Address	Register Address	Description	Value
F1	D1	0	0000	Hard-coded	Protocol Revision = V1.3	0100
F2	D2, D3		0001, 0010	Hard-coded	Number of Data Blocks = 32	0010 0000
F3	D4		0011	MFG_ID[7:4]	Manufacturer ID	User
	D5		0100	MFG_ID[3:0]		
F4	D6, D7		0101, 0110	Hard-coded	Sensor Type = Acceleration (high-g)	0000 0001
F5	D8		0111	U_DIR[1:0] = 00: 0000 U_DIR[1:0] = 01: 0100 U_DIR[1:0] = 10: 1000 U_DIR[1:0] = 11: 1100 (not used)	Axis	User
	D9		1000	±60g: 0111 ±120g: 1000 ±240g: 1001 ±480g: 1010	Range	Varies
F6	D10		1001	DEVCFG2[7:4]	Sensor Specific Information	User
	D11		1010	DEVCFG2[3:0]	Sensor Specific Information	User
F7	D12		1011	Hard-coded	Product Revision	Factory
	D13		1100	Hard-coded	Product Revision	Factory
	D14		1101	DEVCFG6[3:0]	Product Revision	User
F8	D15		1110	DEVCFG7[7:0], DEVCFG8[4:0] converted to Binary coded Julian Date Reference Section 3.1.5.5	JY[6:3]	User
	D16		1111		JY[2:0], JM[3]	User
	D17	1	0000		JM[2:0], JD[1]	User
	D18		0001		JD[3:0]	User
F9	D19		0010	SN0 (High Nibble)	MMA52xx Serial Number	Factory
	D20		0011	SN0 (Low Nibble)	MMA52xx Serial Number	Factory
	D21		0100	SN1 (High Nibble)	MMA52xx Serial Number	Factory
	D22		0101	SN1 (Low Nibble)	MMA52xx Serial Number	Factory
	D23		0110	SN2 (High Nibble)	MMA52xx Serial Number	Factory
	D24		0111	SN2 (Low Nibble)	MMA52xx Serial Number	Factory
	D25		1000	SN3 (High Nibble)	MMA52xx Serial Number	Factory
	D26		1001	SN3 (Low Nibble)	MMA52xx Serial Number	Factory
	D27		1010	Initial Raw Offset (Offset[3:0])	Raw Offset[1] (If INIT2_EXT=1, '0000' otherwise)	Varies
	D28		1011	Initial Raw Offset (Offset7:4])	Raw Offset[1] (If INIT2_EXT=1, '0000' otherwise)	Varies
	D29		1100	([AvgSelfTest[1:0],Offset[9:8]])	Raw Off/Avg ST[1] (If INIT2_EXT=1, '0000' otherwise)	Varies
	D30		1101	Average Self-Test (AvgSelfTest[5:2])	Avg Self-Test[1] (If INIT2_EXT=1, '0000' otherwise)	Varies
	D31		1110	Average Self-Test (AvgSelfTest[9:6])	Avg Self-Test[1] (If INIT2_EXT=1, '0000' otherwise)	Varies
	D32		1111	DEVCFG1 [7:4]	Sensor Specific (If INIT2_EXT=1, '0000' otherwise)	0010

[1] Offset and average self-test data will only be transmitted with sync pulse periods that guarantee the self-test phase1 and phase 2 will be complete prior to required transmission. If sync pulse periods faster than this are used, '0's will be transmitted instead of offset and/or average self-test data.

4.4.2.2 Initialization Phase 2 (8-Bit Mode)

In PSI5 initialization phase 2, 8-bit mode, the device transmits a sequence of sensor specific configuration and serial number information. The transmission data uses a format similar to the PSI5 specification, Revision 1.3 10-Bit format modified for 8-bit transmission. The data content and transmission format is shown in Table 12 and Table 13. Table 12 shows the 8-bit phase 2 timing for different operating modes. Times are calculated using the equation in Section 4.4.2.

Table 12. Initialization Phase 2 Time (8-Bit Mode)

Operating Mode	Repetition Rate (k)	# of Transmissions	Nominal Phase 2 Time
Asynchronous Mode 0 (228 µs)	16	576	131.3 ms
Synchronous Mode (500 µs)	8	288	144.0 ms

Table 13. PSI5 Initialization Phase 2 Data (8-Bit Mode)

PSI5 V1.2 Field ID #	PSI5 V1.2 Nibble ID #	Page Address	PSI5 Half-Nibble Address	Register Address	Description	Value
F1	D1 H	0	00	Hard-coded	Protocol Revision = V1.3	01
F1	D1 L	0	01	Hard-coded	Protocol Revision = V1.3	00
F2	D2 H	0	10	Hard-coded	Number of Data Blocks = 9	00
F2	D2 L	0	11	Hard-coded	Number of Data Blocks = 9	10
F2	D3 H	1	00	Hard-coded	Number of Data Blocks = 9	00
F2	D3 L	1	01	Hard-coded	Number of Data Blocks = 9	00
F3	D4 H	1	10	Hard-coded, MFG_ID[7:6]	Manufacturer ID	User
F3	D4 L	1	11	Hard-coded, MFG_ID[5:4]	Manufacturer ID	
F3	D5 H	2	00	Hard-coded, MFG_ID[3:2]	Manufacturer ID	
F3	D5 L	2	01	Hard-coded, MFG_ID[1:0]	Manufacturer ID	
F4	D6 H	2	10	Hard-coded	Sensor Type = Acceleration (high-g)	00
F4	D6 L	2	11	Hard-coded	Sensor Type = Acceleration (high-g)	00
F4	D7 H	3	00	Hard-coded	Sensor Type = Acceleration (high-g)	00
F4	D7 L	3	01	Hard-coded	Sensor Type = Acceleration (high-g)	01
F5	D8 H	3	10	U_DIR[1:0] = 00: 0000 U_DIR[1:0] = 01: 0100 U_DIR[1:0] = 10: 1000 U_DIR[1:0] = 11: 1100 (not used)	Axis	User
F5	D8 L	3	11			User
F5	D9 H	4	00	±60g: 0111 ±120g: 1000 ±240g: 1001 ±480g: 1010	Range	Varies
F5	D9 L	4	01			Varies

4.4.3 Internal Self-Test

During PSI5 Initialization Phase 2 and Phase 3, the device completes it's internal self-test as described below and shown in Figure 32.

- Self-Test Phase 1 - Raw Offset Calculation
  - The average offset is calculated for t_{ST1} (Self-Test Disabled).
  - If the INIT2_EXT bit is set, this 10-bit value is transmitted in Initialization Phase 2 (reference Section 4.4.2).
- Self-Test Phase 2 - Self-Test Deflection Verification
  - The offset cancellation value is frozen for t_{ST2} + 2ms
  - Self-Test is enabled
  - After $t_{ST2}/2$, the acceleration output value is averaged for $t_{ST2}/2$ to determine the self-test value
  - If the INIT2_EXT bit is set, this10-bit value is transmitted in Initialization Phase 2 (reference Section 4.4.2).
  - The self-test value is compared against the limits specified in Section 2.5
  - Self-Test is disabled
- Self-Test Phase 3 - Self-Test Normal Data Calculation
  - The average offset is calculated for t_{ST3}
  - If Self-Test passed, the device advances to normal mode
  - If Self-Test failed, the device repeats Self-Test Phases 1 through 3 up to ST_RPT times.

4.4.4 Initialization Phase 3

During PSI5 initialization phase 3, the device completes it's internal self checks, and transmits a combination of "Sensor Busy", "Sensor Ready", or "Sensor Defect" messages as defined in Table 9. The number of messages transmitted in initialization phase 3 varies depending on the mode of operation, and the number of self-test repetitions. Self-Test is repeated on failure up to ST_RPT times to provide immunity to misuse inputs during initialization. Self-Test terminates successfully after one successful self-test sequence.

Table 14 shows the nominal Initialization Phase 3 times for different operating modes and self-test repeats. Times are calculated using the following equation.

$$t_{PSI5INIT3} = \mathrm{ROUNDUP}\left(\frac{(t_{INTINIT} + t_{OC1} + t_{OC2} + (t_{ST1} + t_{ST2} + t_{ST3}) \times (STRPT + 1)) - (t_{PSI5INIT1} + t_{PSI5INIT2xx})}{t_{S-S}} + 2\right) \times t_{S-S}$$

Table 14. Initialization Phase 3 Time

Operating Mode	Self-Test Repetitions	# of Sensor Busy Messages	# of Sensor Ready or Sensor Defect Messages	Nominal Phase 3 Time (ms)
8-Bit Asynchronous Mode 0 (228 µs)	0	0	2	0.46
	1	359		82.31
	2	780		178.30
	3	1201		274.28
	4	1622		370.27
	5	2043		466.26
10-Bit Asynchronous Mode 0 (228 µs)	0	2		0.91
	1	423		96.90
	2	844		192.89
	3	1265		288.88
	4	1686		384.86
	5	2107		480.85
8-Bit Synchronous Mode (500 µs)	0	0		1.00
	1	138		70.00
	2	330		166.00
	3	522		262.00
	4	714		358.00
	5	906		454.00
10-Bit Synchronous Mode (500 µs)	0	0		1.00
	1	170		86.00
	2	362		182.00
	3	554		278.00
	4	746		374.00
	5	938		470.00

4.5 PSI5 Transmission Modes

4.5.1 Normal Mode

4.5.1.1 Asynchronous Mode

The device can be programmed to respond in asynchronous mode with the following settings:

- TRANS_MD[1:0] = ‘00’ (“Normal Mode”)
- ASYNC = ‘1’ in the DEVCFG6 Register
- TIMESLOTA[9:0] = 0x000 in the DEVCFG3 and DEVCFG4 registers

In asynchronous mode, the device transmits data at a fixed rate (t_{ASYNC}) and will not respond to normal sync pulses. However, during initialization phase 1, sync pulses are monitored to decode the Programming Mode Entry Command and allow entry into Programming Mode if the LOCK_U bit is not set.

4.5.1.2 Simultaneous Sampling Mode

The device can be programmed to respond in Simultaneous Sampling Mode by setting the TRANS_MD[1:0] bits to “Normal Mode”, and by programming the LATENCY bit to “Simultaneous Sampling Mode”.

In Simultaneous Sampling Mode, the most recent interpolated acceleration data sample is latched at t_{TRIG} (rising edge of Sync Pulse) and transmitted starting at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG}.

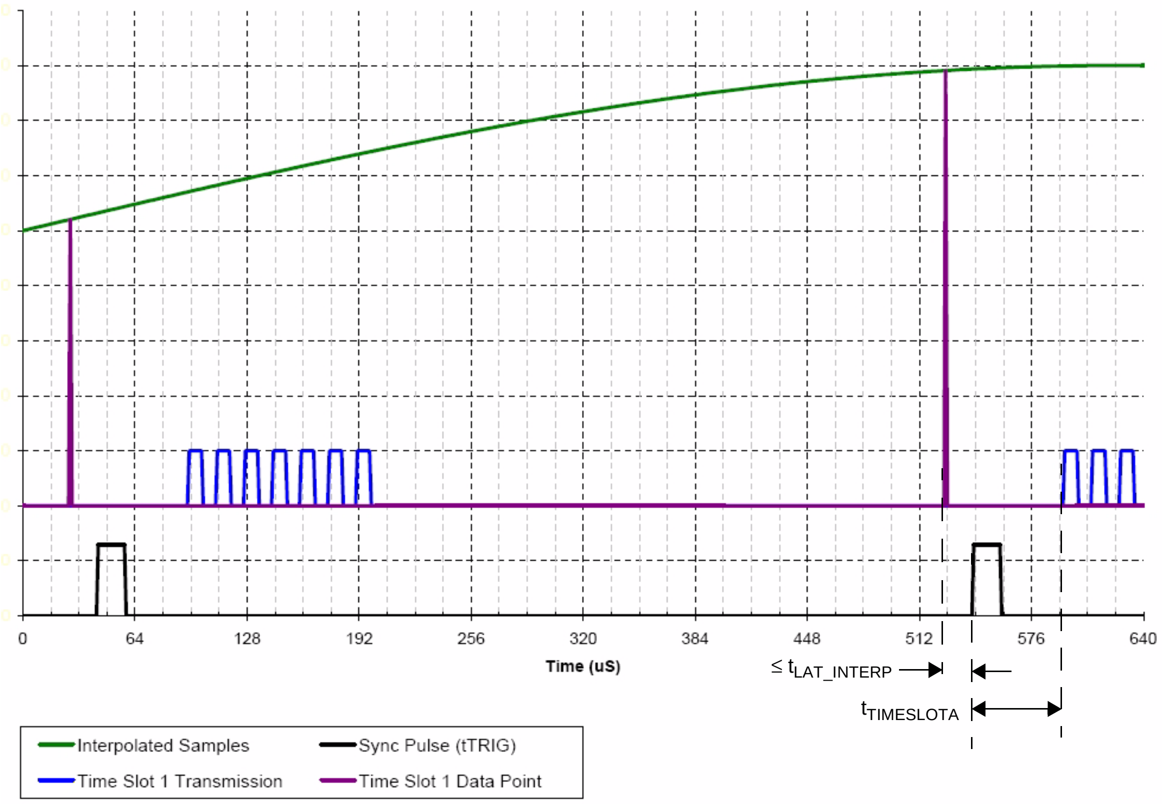


Figure 35. Simultaneous Sampling Mode

4.5.1.3 Synchronous Sampling Mode with Minimum Latency

The device can be programmed to respond in Synchronous Sampling Mode with minimum latency by setting the TRANS_MD[1:0] bits to “Normal Mode”, and by programming the LATENCY bit to “Synchronous Sampling Mode”.

In Synchronous Sampling Mode, the most recent interpolated acceleration data sample is latched at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG} (rising edge of Sync Pulse). The data is transmitted starting at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG}.

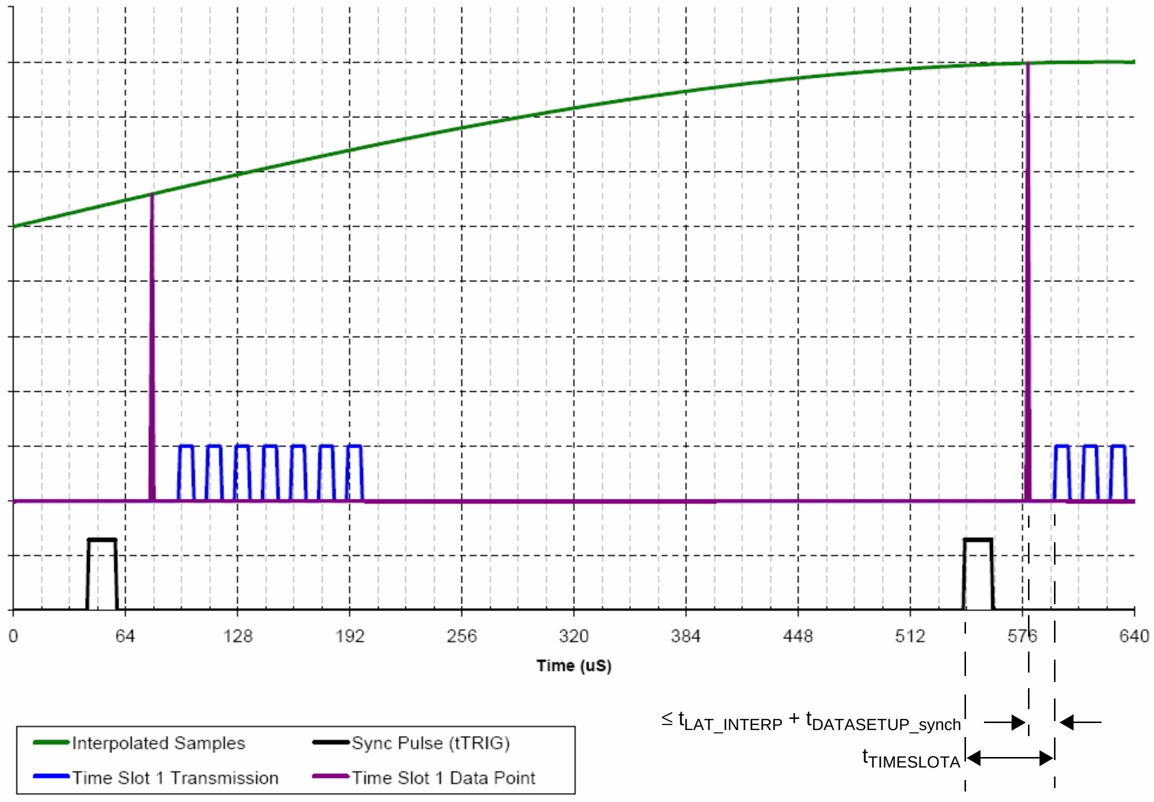


Figure 36. Synchronous Sampling Mode with Minimum Latency

4.5.2 Synchronous Double Sample Rate Mode

The device can be programmed to respond in Synchronous Double Sample Rate Mode with minimum latency by setting the TRANS_MD[1:0] bits to “Synchronous Double Sample Rate Mode”. The LATENCY bit does not affect operation in this mode.

In Synchronous Double Sample Rate Mode, the most recent interpolated acceleration data sample is latched at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG} (rising edge of Sync Pulse). This data is transmitted starting at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG}. In addition, the most recent interpolated acceleration data sample is latched at the time programmed in TIMESLOTB[9:0], relative to t_{TRIG} (rising edge of Sync Pulse) This data is transmitted starting at the time programmed in TIMESLOTB[9:0], relative to t_{TRIG}.

When Synchronous Double Sample Rate Mode is enabled, PSI5 Initialization data is transmitted in both TIMESLOTA[9:0] and TIMESLOTB[9:0]. Identical data is transmitted in both Time slots, including the 10-bit resolution Raw Offset and Self-Test Data in Field 9, D27 though D31 if enabled.

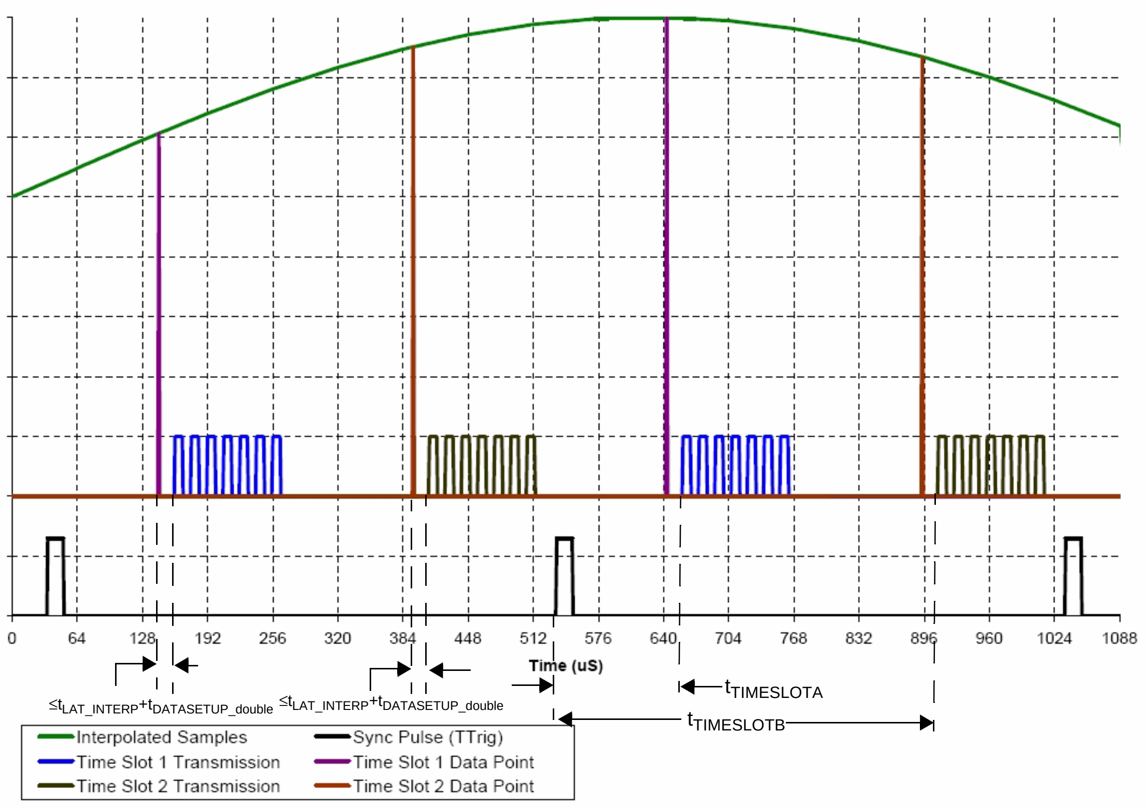


Figure 37. Synchronous Double Sample Rate Mode

Note: In the event that the programmed values in TIMESLOTA[9:0] and TIMESLOTB[9:0] result in a conflict, no data will be transmitted in TIMESLOTB[9:0].

4.5.3 16-Bit Resolution Mode

The device can be programmed to respond in 16-bit Resolution Mode by setting the TRANS_MD[1:0] bits to “16-bit Resolution Mode”. In this mode, the 26 bit digital output from the DSP is clipped and scaled to a 16-bit word. Figure 38 shows the method used to establish the 16-bit data word from the 26 bit DSP output.

Over Range			**Signal**										**Noise**				**Margin**							
D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	...	D2	D1	D0
16-bit Data Word				D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Using Rounding				

Figure 38. 16-Bit Output Scaling Diagram

16-Bit Resolution Mode can be programmed to operate in either “Simultaneous Sampling Mode”, or “Synchronous Sampling Mode”, by setting the LATENCY bit to the desired operating mode. In Simultaneous Sampling Mode, the most recent interpolated acceleration data sample is latched at t_{TRIG} (rising edge of Sync Pulse). In Synchronous Sampling Mode, the most recent interpolated acceleration data sample is latched at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG} (rising edge of Sync Pulse).

The most significant 10 bits (D[21:12]) are truncated and transmitted starting at the time programmed in TIMESLOTA[9:0], relative to t_{TRIG}. The 16-bit value is then clipped to ±480 counts, and the least significant 10 bits (D15:D6) are transmitted starting at the time programmed in TIMESLOTB[9:0], relative to t_{TRIG}.

When 16-Bit Resolution Mode is enabled, PSI5 Initialization data is transmitted in both TIMESLOTA[9:0] and TIMESLOTB[9:0]. Identical data is transmitted in both Time slots, including the 10-Bit Resolution Raw Offset and Self-Test Data in Field 9, D27 though D31 if enabled.

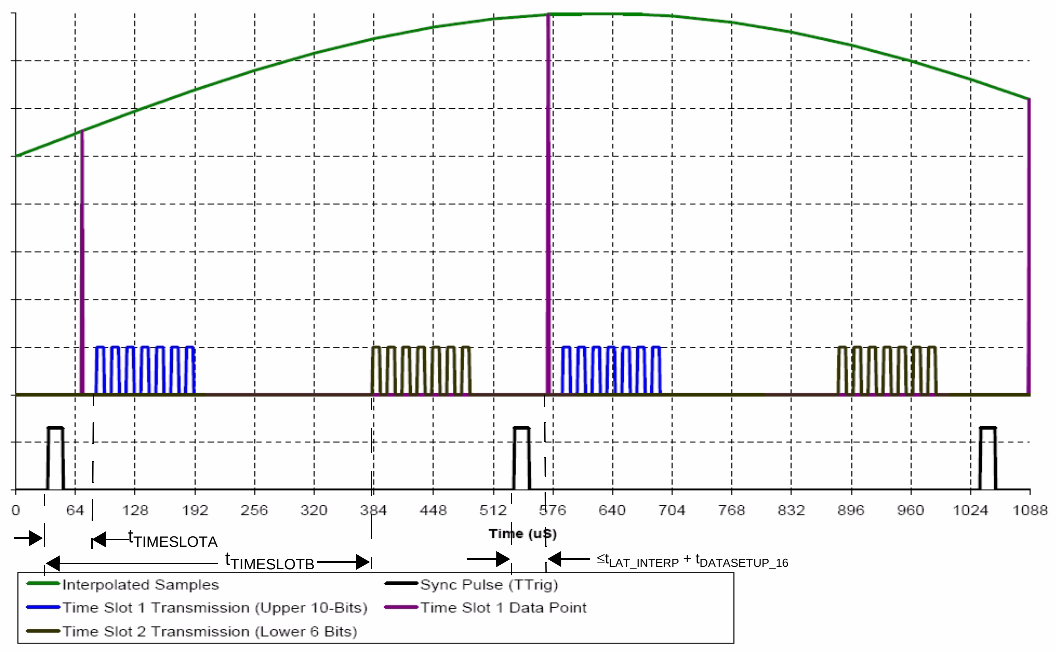


Figure 39. 16-Bit Resolution Mode with Synchronous Sampling

Note: In the event that the programmed values in TIMESLOTA[9:0] and TIMESLOTB[9:0] result in a conflict, no data will be transmitted in TIMESLOTB[9:0].

4.5.4 Daisy Chain Mode

The device can be programmed to operate in Daisy Chain Mode by setting the TRANS_MD[1:0] bits to “Daisy Chain Mode”. Daisy Chain Mode can be programmed to operate in either “Simultaneous Sampling Mode”, or “Synchronous Sampling Mode” by setting the LATENCY bit to the desired operating mode. In Simultaneous Sampling Mode, the most recent interpolated acceleration data sample is latched at t_{TRIG} (rising edge of Sync Pulse). In Synchronous Sampling Mode, the most recent interpolated acceleration data sample is latched at the time slot for the daisy chain address programmed, relative to t_{TRIG} (rising edge of Sync Pulse).

When programmed to operate in Daisy Chain Mode, the procedure below is followed:

- On powerup, the device proceeds through normal PSI5 initialization as specified in Section 4.4 using a pre-defined time slot $t_{TIMESLOT\_DCP}$.
- Upon successful completion of Initialization Phase 3, including the 2 “Sensor Ready” or Sensor Defect” messages, responses to sync. pulses are terminated and the device waits for a PSI5 “Set Address” command defined in Table 15 and Table 16.
  - The Daisy Chain Programming command and response formats are defined in Section 5.4.
  - Valid Daisy Chain Addresses are defined in Table 17.
  - The response to the PSI5 Set Address command uses the pre-defined time slot $t_{TIMESLOT\_DCP}$.
- After receiving a valid address and completing the response, sync. pulses are blanked for $t_{DC\_BLANKING}$. Once the blanking time expires, the device does not respond to any sync. pulses until a “Run Mode” command is received, as defined in Table 15 and Table 16.
- When the “Run Mode” command is received, the device responds to this command using the programmed daisy chain time slot. All commands are then ignored, and sync pulses are responded to with acceleration data using the following response format, regardless of the state of the relevant bits in the Device Configuration Registers:

Parameter	Reference	Value
Time Slot	Section 3.1.4.3	Default time slot specified in Table 17
Data Size	Section 3.1.3.5	10-bit data
Error Checking	Section 3.1.3.7	Even Parity
Baud Rate	Section 3.1.3.8	Low Baud Rate: 125 kBaud

- During initialization and Run Mode, the Sync pulse pulldown is enabled as specified in Section 3.1.3.3.

Table 15. Daisy Chain Programming Commands and Responses

#	CMD Type	SAdr			FC			Command	Response (OK)		Response (Error)	
		A2	A1	A0	F2	F1	F0		RC	RD1	RC	RD1
D0	Short	0	0	0	A2	A1	A0	Set Sensor Address (Daisy Chain)	OK	SAdr	Error	ErrN
D1	Short	1	1	1	0	0	0	Broadcast Message - “Run Mode”	OK	0x000	Error	ErrN

Table 16. Daisy Chain Programming Response Code Definitions

Response Code	Definition	Value
RC = OK	Command Message Received Properly	0x1E1
RC = Error	Error during transmission of Command Message	0x1E2
SAdr	Programmed Sensor Address, prepended with 0s	Varies

Table 17. Valid Daisy Chain Addresses

Sensor Address (SAdr)			Description	Bus Switch Control	Default Time Slot
A2	A1	A0			
0	0	0	Address of un-programmed sensor	N/A	N/A
0	0	1	Sensor Address 1	CLOSED	$t_{TIMESLOT\_DC1}$
0	1	0	Sensor Address 2	CLOSED	$t_{TIMESLOT\_DC2}$
0	1	1	Sensor Address 3	CLOSED	$t_{TIMESLOT\_DC3}$
1	0	0	Sensor Address 4	OPEN	$t_{TIMESLOT\_DC1}$
1	0	1	Sensor Address 5	OPEN	$t_{TIMESLOT\_DC2}$
1	1	0	Sensor Address 6	OPEN	$t_{TIMESLOT\_DC3}$
1	1	1	Global Address for Broadcast Message to all Sensors	N/A	N/A

4.6 Error Handling

4.6.1 Sensor Defect Message

The following failures will cause the device to transmit a “Sensor Defect” error message:

Error Condition	Error Type
Offset Error	Temporary (Normal transmissions continue once offset returns within limits)
Self-Test Failure	Latched until reset
IDEN_B, IDEF_B flag cleared	Latched until reset

4.6.2 No Response Error

The following failures will cause the device to stop transmitting:

Error Condition	Error Type
Undervoltage Failure (V_{CC})	Temporary: Normal transmissions continue once voltage returns above failure limit)

5 Programming Mode Via PSI5

5.1 Introduction

Programming mode via PSI5 is a synchronous communication mode that allows for bidirectional communication with the device. Programming mode is intended for factory programming of the OTP array. It is not intended for use in normal operation.

5.2 Programming Mode Via PSI5 Entry

The device enters programming mode if and only if the following sequence occurs:

- The device is unlocked (the LOCK_U bit in the DEVCFG2 register is ‘0’).
- At least 31 sync pulses are detected, directly preceding the Programming Mode Entry Short Command during the Programming Mode Entry Window shown in Figure 32.
  - The window timing is defined in Section 2.6 (t_{PME}).
  - The Sync pulses and Programming Mode Entry command must be received with a sync pulse period of $t_{S\text{-}S\_PM\_L}$

If the Programming Mode entry requirement is not met:

- Programming Mode Entry is blocked until the device is Reset.
- The device proceeds with PSI5 Initialization Phase 2, and PSI5 Initialization Phase 3.
- The device enters normal mode, and responds as programmed to normal sync pulses.

If the Programming Mode entry requirement is met:

- Normal transmissions to sync pulses are terminated.
- After a pre-defined Start Delay, the device begins to decode PSI5 Short and Long Commands.
- The device responds only to valid PSI5 Short and Long Commands addressed to Sensor Address ‘001’, as defined in Table 19.

Note: The sync pulse pulldown is disabled in the Programming Mode Entry Window regardless of the state of the SYNCPD bit.

5.3 Programming Mode Via PSI5 - Data Link Layer

5.3.1 Programming Mode Via PSI5 - Command Bit Encoding

Commands messages are transmitted via the modulation of the supply voltage. The presence of a sync pulse is a logic '1' and the absence of a sync pulse is a logic '0'. Sync pulses are expected at a rate of $t_{S\text{-}S\_PM\_L}$.

5.3.2 Programming Mode Via PSI5 - Command Message Format

Command message data frames consist of a start condition, 3 Start Bits (S[2:0]), a 3 bit Sensor Address (SAdr[2:0]), a 3-bit Function Code (FC[2:0]), an optional Register Address (RAdr[5:0]), an optional data field (D[3:0]), and a 3-bit CRC (C[2:0]. The start condition consists of one of the following:

1. A minimum of 5 consecutive logic ‘0’s (with not sync bits)
2. A minimum of 31 consecutive logic ‘1’s

The command message format is shown in Figure 41.

Start Bits			Sensor Address			Function Code			Register Address						Data				CRC		
S2	S1	S0	SA0	SA1	SA2	FC0	FC1	FC2	RA0	RA1	RA2	RA3	RA4	RA5	D0	D1	D2	D3	C2	C1	C0
0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	0	0	0

CRC

Data to be written to register (optional)

Register Address (optional)

Function Codes for MMA52xx (Reference Section 5.3.6)

Sensor Address - Fixed at 001 for MMA52xx

Start Bit Sequence = 010

Response		
RC	**RD1**	**RD0**
$3FF	$3FF	$3FF

Figure 40. Programming Mode Via PSI5 Command Data Format

Bit stuffing is necessary to maintain a synchronized time base between the command master and the device. A logic ‘1’ Sync bit is added every 4th bit in the command message to ensure there will never be more than 3 logic '0' bits in a row.

Start Bits				Sensor Address				Function Code				Register Address								Data					CRC			
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	D0	D1	D2	Sy	D3	C2	C1	Sy	C0
0	1	0	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	1	0

Response		
RC	RD1	RD0
$1E2	$3FF	$3FF

Figure 41. Programming Mode Via PSI5 Command Data Format with Sync Bits

Once a command is received and verified, the device expects 2 to 3 consecutive sync pulses (depending upon the command message lengths described below). For each of these sync pulses, the device will respond with the following settings:

Parameter	Register Bits	Reference	Value
Time Slot	N/A	N/A	$t_{TIMESLOT\_DC1}$
Data Size	DATASIZE = 0	Section 3.1.3.5	10-bit data
Error Checking	P_CRC = 0	Section 3.1.3.7	Even Parity
Baud Rate	BAUD	Section 3.1.3.8	125 kBaud
Sync Pulse Pulldown	SYNCPD	Section 3.1.3.3	Disabled

Figure 42. Programming Mode Via PSI5 Response Message Settings

5.3.2.1 Short Frame Command and Response Format

Short frames are the simplest type of command message. No data is transmitted in a short frame command. Only specific instructions are performed in response to short frame commands. The Short Frame format is shown in Figure 43. Short Frame commands and responses are defined in Section 5.3.6, Table 19.

Start Bits				Sensor Address				Function Code				CRC		
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	C2	C1	C0
0	1	0	1	1	0	0	1	0	0	1	1	0	0	0

Response	
RC	RD1
$1E2	$3FF

Figure 43. Programming Mode Via PSI5 Short Command and Response Format

5.3.2.2 Long Frame Command and Response Format

Long frames allow for the transmission of data nibbles for register writes. The device can provide register data in response to a read or write request. The Long Frame format is shown in Figure 44. Long Frame commands and responses are defined in Section 5.3.6.

Start Bits				Sensor Address				Function Code				Register Address								Data					CRC			
S2	S1	S0	Sy	SA0	SA1	SA2	Sy	FC0	FC1	FC2	Sy	RA0	RA1	RA2	Sy	RA3	RA4	RA5	Sy	D0	D1	D2	Sy	D3	C2	C1	Sy	C0
0	1	0	1	1	0	0	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	1	0

Response		
RC	RD1	RD0
$1E2	$3FF	$3FF

Figure 44. Programming Mode Via PSI5 Long Command and Response Format

5.3.3 Command Message CRC

Programming mode command error checking is accomplished by a 3-bit CRC. The 3-bit CRC is calculated using all message bits except start bits and sync bits. The CRC verification uses a generator polynomial of $g(x) = X^3+X+1$, with a seed value = ‘111’. The data is provided to the CRC calculator in the order received (LSB first, SAdr, FC, RAdr, Data), and then augmented with three ‘0’s. Table 9 shows some example CRC calculation values for 10-bit data transmissions.

The calculated CRC is then compared against the received 3-bit CRC (received MSB first). If a CRC mismatch is detected, the device responds with a CRC Error response as defined in Section 5.3.7.

5.3.4 Command Sync Pulse Blanking Time

In Programming Mode and Programming Mode Entry, the device employs a fixed Sync Pulse blanking time of $t_{SYNC\_OFF\_500}$ regardless of the state of the BLANKTIME bit.

5.3.5 Command Timeout

In the event that the device does not detect a sync pulse within a 4-bit window time (missing sync bit), the command reception will be terminated and the device will respond to the next sync pulse with a Short Frame Framing Error response as defined in Section 5.3.7.

5.3.6 Programming Mode Via PSI5 Command and Response Summary

Table 18. Programming Mode Via PSI5 Commands and Responses

#	CMD Type	SAdr	FC	Command	Register Address	Data Field	Response (OK)			Response (Error)		
							RC	RD1	RD0	RC	RD1	RD0
S0	Short	001	100	Execute Programming of NVM	N/A	N/A	OK	0x2AA	N/A	Error	ErrN	N/A
S1	Short		101	Invalid Command	N/A	N/A	No Response			No Response		
S2	Short		110	Invalid Command	N/A	N/A	No Response			No Response		
S3	Short		111	Enter Programming Mode	N/A	N/A	OK	0x0CA	N/A	No Response		
LR	Long		010	Read nibble located at address RA5:RA0	Varies	Varies	OK	RData	RData+1	Error	ErrN	0x000
LW	Long		011	Write nibble to register RA5:RA0	Varies	Varies	OK	WData	RA5:RA0	Error	ErrN	0x000
XLR	XLong		000	Invalid Command	Any	Any	No Response			No Response		
XLW	XLong		001	Invalid Command	Any	Any	No Response			No Response		

Note: When reading the last address in the data array, RData+1 will always return 0x00.

Table 19. Programming Mode Via PSI5 Response Code Definitions

Response Code	Definition	Value
RC = OK	Command Message Received Properly	0x1E1
RC = Error	Error during transmission of Command Message	0x1E2
RData	Byte Contents of Register located at Byte address in which nibble address RA5:RA0 falls in. (Example: For RA5:RA0 = $04 - RData = Data at Byte Address $02)	Varies
RData + 1	Byte Contents of Register located at Byte address in which nibble address RA5:RA0 +2 falls in. (Example: For RA5:RA0 = $04 - RData + 1= Data at Byte Address $03)	Varies
WData	Byte Contents of Register located at Byte address in which nibble address RA5:RA0 falls in after write operation. (Example: For RA5:RA0 = $04 - RData = Data at Byte Address $02)	Varies

5.3.7 Programming Mode Via PSI5 Error Response Summary

Table 20. Error Response Summary

ErrN*	Mnemonic	Description	Supported By MMA52xx
0000	General	General Error	No
0001	Framing	Framing Error	Yes
0010	CRC	CRC Error on Received Message	Yes
0011	Address	Sensor Address Not Supported	No (Invalid Address is ignored)
0100	FC	Function Code Not Supported	No (N/A)
0101	Data Range	Unsupported Register Address	Yes
0110	Write Protect	Destination Address is Write protected (Locked)	Yes
0111	Reserved	Reserved	No
1000	Reserved	Reserved	No
1001			
1010			
1011			
1100			
1101			
1110			
1111			

* ErrN is transmitted in the 4 LSBs of RD1. All other bits in the response data field are set to ‘0’.

5.4 OTP Programming Via PSI5 Procedure

1. Enter Programming Mode.
2. Load desired data into the OTP shadow registers using PSI5 Long Write commands.
3. Send “Execute Programming of NVM“ Short command.
4. Set V_{CC} = V_{PP} prior to, or within t_{PROG_HOLD} after the “Execute Programming of NVM” Command has been transmitted. There is an internal delay of t_{PROG_ARRAY} after the “Execute Programming of NVM” Command is received until the OTP programming begins.
5. Delay a minimum of t_{PROG_USER}. During the OTP Write sequence, sync pulses will be ignored. However, transmission of sync pulses during the OTP Write sequence should be prevented.
6. Read the SC register and verify IDEF_B flag is set (indicating the write is complete and successful, and the shadow registers have been refreshed with the OTP contents).
7. Read the OTP register values and compare to the desired values.

6 SPI Diagnostic and Programming Mode

SPI Diagnostic and Programming Mode allows for the following functions:

- Programming of the OTP array
- Reading of memory registers

SPI transfers follow CPOL = 0, CPHA = 0, MSB first convention. Figure 7 shows the SPI transfer timing, and Figure 45 shows the SPI transfer protocol.

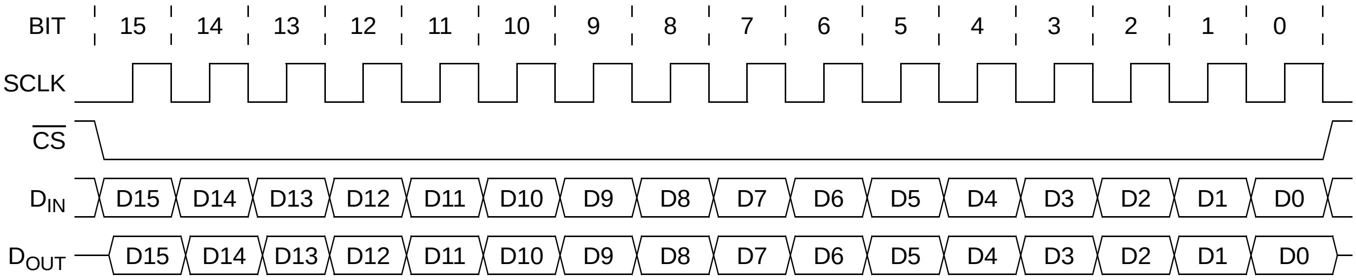


Figure 45. SPI Transfer Protocol

The following operations are supported in DPM:

- Register pointer write
- Register pointer read
- Register data write
- Register data read
- Acceleration data read

6.1 Communication Error Detection

6.1.1 Data Input Parity Detection

All commands except for the DPM Entry command employ odd parity to ensure data integrity. For Read commands, the parity bit is located in bit D10, and the parity is calculated using bits D15 through D11. For Write commands, the parity bit is located in bit D9, and the parity is calculated using bits D15 through D0. If a parity error is detected, both the current and subsequent commands are ignored, and the parity fault response is transmitted during the subsequent SPI transfer.

6.1.2 Data Output Parity

All responses except for the DPM entry response employ odd parity to ensure data integrity. Parity is calculated using the entire 16-bit message.

6.2 DPM Entry

DPM can be activated at any time during the operation of the device, provided the SPI DPM Entry command is the first command transmitted. If an incorrect DPM Entry command is received, DPM is locked out, and cannot be activated until the device is reset.

The device responds to the DPM Entry command with the logical complement of the received data as confirmation that it has been received correctly. Upon completion of a successful transfer DPM is activated. Once activated, the device will remain in DPM until a reset condition occurs.

Following successful transmission of the DPM Entry command, DPM operations may be completed in any order.

6.3 DPM Command/Response Summary

Table 21 provides a summary of SPI commands and responses.

Table 21. SPI Command/Response Summary

Command	Pin	Bit															
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SPI DPM Entry	D_{IN}	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
	D_{OUT}	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
Register Pointer Write	D_{IN}	0	1	0	0	1	1	P	X	A7	A6	A5	A4	A3	A2	A1	A0
	D_{OUT}	1	0	1	1	0	P	0	1	0	0	0	0	0	0	0	0
Register Pointer Read	D_{IN}	0	1	0	0	0	P=0	0	X	X	X	X	X	X	X	X	X
	D_{OUT}	1	0	1	1	0	P	0	1	A7	A6	A5	A4	A3	A2	A1	A0
Register Data Write	D_{IN}	0	1	0	1	1	0	P	X	D7	D6	D5	D4	D3	D2	D1	D0
	D_{OUT}	1	0	1	0	0	P	1	0	A7	A6	A5	A4	A3	A2	A1	A0
Register Data Read	D_{IN}	0	1	0	1	0	P=1	0	X	X	X	X	X	X	X	X	X
	D_{OUT}	1	0	1	0	0	P	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Acceleration Data Read	D_{IN}	0	1	1	0	0	P=1	0	0	0	0	0	0	0	0	0	0
	D_{OUT}	1	0	0	1	1	P	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Invalid Command Response (Waiting for SPI DPM Entry)	D_{IN}	0	0	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
	D_{OUT}	1	No Response (all 0s) - DPM Entry Locked Out														
	D_{IN}	0	1	1	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
	D_{OUT}	1	No Response (all 0s) - DPM Entry Locked Out														
	D_{IN}	1	1	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
	D_{OUT}	0	0	No Response (all 0s) - DPM Entry Locked Out													
	D_{IN}	1	0	D[13]	D[12]	D[11]	...	D[x]	Not SPI DPM Entry Command								
	D_{OUT}	0	1	$\overline{D[13]}$	$\overline{D[12]}$	$\overline{D[11]}$	...	$\overline{D[x]}$	No Response (all 0s) - DPM Entry Locked Out								
Invalid Command Response	D_{IN}	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	D_{OUT}	d[15]	d[14]	d[13]	d[12]	d[11]	d[10]	d[9]	d[8]	d[7]	d[6]	d[5]	d[4]	d[3]	d[2]	d[1]	$\overline{d[0]}$
Parity Fault Response (Subsequent Message Response)	D_{IN}	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	D_{OUT}	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

6.4 Register Pointer Operations

Access to internal registers is accomplished via a pointer register. The pointer contains the address of the register affected by register data write and read operations. Two register pointer operations are provided: Register Pointer Write, and Register Pointer Read. Command and response information is shown in Table 21.

6.5 Register Data Operations

Two register operations are provided: Register Write, and Register Read. In each case, the address of the affected register is contained in the register pointer.

6.5.1 Register Write Command

The Register Write command format is shown in Table 21. The least significant 8 bits of the Register Write command message contain the data to be written to the register pointed to by the register pointer. The least significant 8 bits of the Register Write response message contain the address of the register that was modified.

The write to the register is executed during the clock cycle immediately after $\overline{CS}$ is deasserted.

6.5.2 Register Read Command

The Register Read command format is shown in Table 21. The least significant 8 bits of the Register Read command message are ignored. The least significant 8 bits of the Register Read response message contain the contents of the register pointed to by the register pointer.

16 bit register reads are possible using consecutive Register Read commands. The high byte of a 16 bit register will automatically be frozen on a read of the low byte of the register.

6.5.3 Acceleration Data Read Operations

The Acceleration Data Read command format is shown in Table 21. The response to this command provides either 8-bit, or 10-bit acceleration data depending on the state of the DATASIZE bit in the DEVCFG2 register.

DATASIZE	**Bit**															
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DATASIZE = 1 (8-Bit Data)	1	0	0	1	1	P	0	0	D7	D6	D5	D4	D3	D2	D1	D0
DATASIZE = 0 (10-Bit Data)	1	0	0	1	1	P	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

6.5.4 Error Responses

6.5.4.1 Response to Invalid Commands

Reference Table 21 for responses to Invalid Commands.

6.5.4.2 Parity Fault Response

If the device detects a Command Parity fault, the current, and subsequent SPI commands are ignored and the device responds to the subsequent message with the Parity Fault response, as shown in Table 21.

6.6 SPI OTP Programming Procedure

1. Set $V_{CC} = V_{PP}$.
2. Enter SPI DPM.
3. Load desired data into the OTP shadow registers using SPI Write commands.
    a. Write the desired contents of DEVCFG2 ($05) to address $05
    b. Write the desired contents of DEVCFG2 ($05) to address $1E
    c. Write the desired contents of DEVCFG3 ($06) to address $06
    d. Write the desired contents of DEVCFG3 ($06) to address $1F
    e. Write the desired contents of DEVCFG4 ($07) to address $07
    f. Write the desired contents of DEVCFG4 ($07) to address $20
    g. Write the desired contents of DEVCFG5 ($08) to address $08
    h. Write the desired contents of DEVCFG5 ($08) to address $21
    i. Write the desired contents of DEVCFG6 ($09) to address $09
    j. Write the desired contents of DEVCFG6 ($09) to address $22
    k. Write the desired contents of DEVCFG7 ($0A) to address $0A
    l. Write the desired contents of DEVCFG7 ($0A) to address $23
    m. Write the desired contents of DEVCFG8 ($0B) to address $0B
    n. Write the desired contents of DEVCFG8 ($0B) to address $24
    o. Write the desired contents of MFG_ID ($0D) to address $0D
    p. Write the desired contents of MFG_ID ($0D) to address $2E
4. Write 0x05 to register $44 to initiate the NVM programming.
5. Delay a minimum of t_{PROG_ARRAY}
6. Read the SC register and verify the IDEF_B flag is set (indicating the write is complete and successful).

7 Package

7.1 Case Outline Drawing

Reference Freescale Case Outline Drawing # 98ASA00090D

http://www.freescale.com/files/shared/doc/package_info/98ASA00090D.pdf

7.2 Recommended Footprint

Reference Freescale Application Note AN3111, latest revision:

http://www.freescale.com/files/sensors/doc/app_note/AN3111.pdf

8 Revision History

Table 22. Revision History

Revision number	Revision date	Description of changes
0	03/2014	- Initial data sheet.
1	03/2014	- Added the AXIS bit definition to the memory map.

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