RoHS

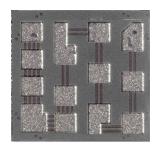
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(5-2008)



# Wire Bondable Thin Film Multi-Tap Resistor Arrays



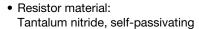
Product may not be to scale

The MTR multi-tap resistors, available in two formats, offer eleven taps allowing the user to select specified increments a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.

These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTRs are 100 % electrically tested and visually inspected to MIL-STD-883.

#### **FEATURES**

- Wire bondable
- · Selectable values by wire bonding
- Chip size: 0.030" x 0.030"
- Case: 0303
- Standard resistance range: 100  $\Omega$  to 24 k $\Omega$  or 800  $\Omega$  to 240 k $\Omega$



- Oxidized silicon substrate for good power dissipation
- · Ideally suited for hybrid prototyping
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>



The MTR series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES				
PARAMETER		VALUE	UNIT	
Total Resistance Range	Format A Format B	100, 200, 400, 800, 2.4K, 8K, 24K 800, 2.4K, 8K, 24K, 80K, 160K, 240K	Ω	
7 Resistors Between Pads 1 and 8 5 Resistors Between Pads 8 and 13		Each 12.5 % of total resistance Each 2.5 % of total resistance		
Standard Tolerances		± 10, ± 20 of total resistance of all 12 resistors	%	
TCR		± 100	ppm/°C	

#### Example:

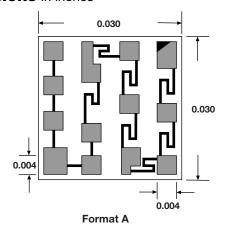
When the total resistance value is 8 k $\Omega$ , the resistors between pads 8 and 13 are 200  $\Omega$  each, and the resistors between pads 1 and 8 are 1 k $\Omega$  each.

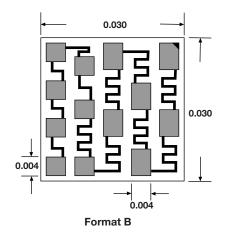
STANDARD ELECTRICAL SPECIFICATIONS			
PARAMETER	VALUE	UNIT	
TCR Tracking Between Elements	± 5	ppm/°C	
Noise, MIL-STD-202, Method 308	-30 typ.	dB	
Moisture Resistance, MIL-STD-202, Method 106	$\pm$ 0.5 max. $\Delta R/R$	%	
Stability, 1000 h, +125 °C, 125 mW	± 0.5 max. ΔR/R	%	
Operating Temperature Range	- 55 to + 125	°C	
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 max. ΔR/R	%	
High Temperature Exposure +150 °C, 100 h	± 0.5 max. ΔR/R	%	
Dielectric Voltage Breakdown	200	V	
Insulation Resistance	10 <sup>12</sup> min.	Ω	
Operating Voltage	100 max.	V	
DC Power Rating at +70 °C (Derated to Zero at +175 °C)	0.250, total <i>R</i>	W	
5 x Rated Power Short-Time Overload, +25 °C, 5 s	± 0.25 max. Δ <i>R/R</i>	%	



# Vishay Electro-Films

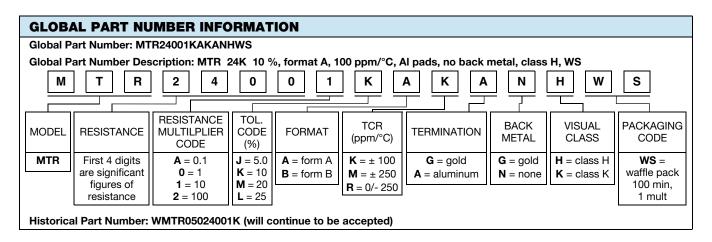
#### **DIMENSIONS** in inches





### **SCHEMATIC**

MECHANICAL SPECIFICATIONS		
PARAMETER		
Chip Size	0.030" x 0.030" ± 0.003" (0.762 mm x 0.762 mm ± 0.076 mm)	
Chip Thickness	0.010" ± 0.002" (0.254 mm ± 0.05 mm)	
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO2	
Resistor Material	Tantalum nitride, self-passivating	
Bonding Pads	0.004" x 0.004" (0.10 mm x 0.10 mm)	
Number of Top Pads	13	
Pad Material	10 kÅ minimum aluminum	
Backing	None, lapped semiconductor silicon	



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