74LV4020

14-stage binary ripple counter

Rev. 01 — 29 November 2005 Product data sheet

1. General description

The 74LV4020 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC4020 and 74HCT4020.

The 74LV4020 is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and 12 fully buffered parallel outputs (Q0, and Q3 to Q13).

The counter advances on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

2. Features

- Optimized for low-voltage applications: 1.0 V to 5.5 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical LOW-level output voltage (peak) or output ground bounce: $V_{OL(p)}$ < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical HIGH-level output voltage (valley) or output V_{OH} undershoot: $V_{OH(v)}$ > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

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4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 2.5 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 3.3 V					
	$\overline{CP}$ to Q0			-	12	-	ns
	Qn to Q(n+1)			-	7	-	ns
t_{PHL}	propagation delay	C_L = 15 pF; V_{CC} = 3.3 V					
	MR to Qn			-	16	-	ns
f_{max}	maximum input clock frequency	C_L = 15 pF; V_{CC} = 3.3 V		-	100	-	MHz
C_i	input capacitance			-	3.5	-	pF
C_{PD}	power dissipation capacitance	per gate; V_I = GND to V_{CC}	[1]	-	20	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4020N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74LV4020D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV4020DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LV4020PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

6. Functional diagram

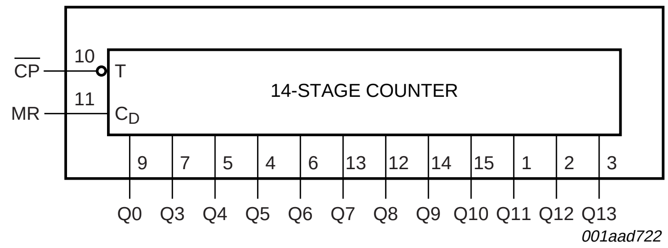


Fig 1. Functional diagram

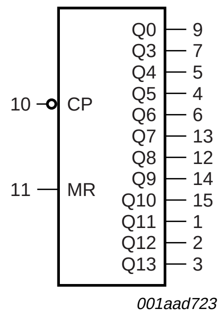


Fig 2. Logic symbol

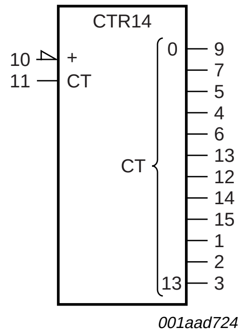


Fig 3. IEC logic symbol

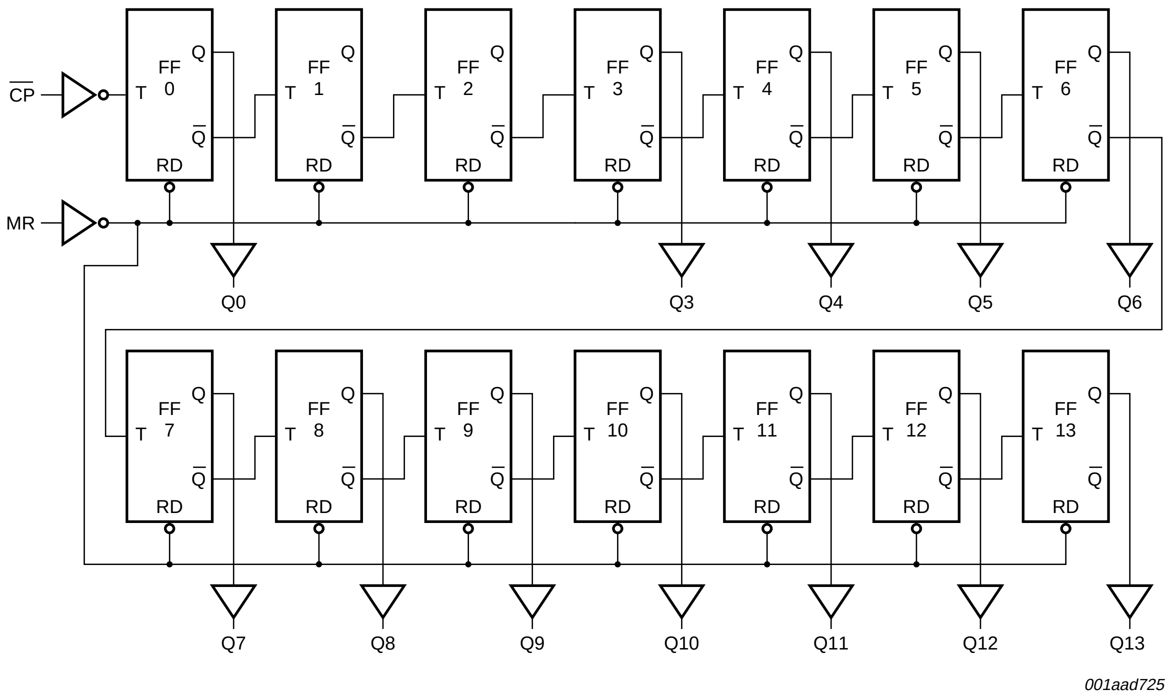


Fig 4. Logic diagram

7. Pinning information

7.1 Pinning

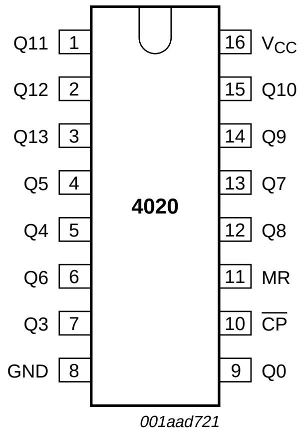


Fig 5. Pin configuration DIP16, SO16, SSOP16 and TSSOP16

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
Q11	1	parallel output 11
Q12	2	parallel output 12
Q13	3	parallel output 13
Q5	4	parallel output 5
Q4	5	parallel output 4
Q6	6	parallel output 6
Q3	7	parallel output 3
GND	8	ground (0 V)
Q0	9	parallel output 0
$\overline{CP}$	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
Q8	12	parallel output 8
Q7	13	parallel output 7
Q9	14	parallel output 9
Q10	15	parallel output 10
V_{CC}	16	supply voltage

8. Functional description

8.1 Function table

Table 4: Function table [1]

Input		Output
$\overline{CP}$	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition;
↓ = HIGH-to-LOW clock transition.

8.1.1 Timing diagram

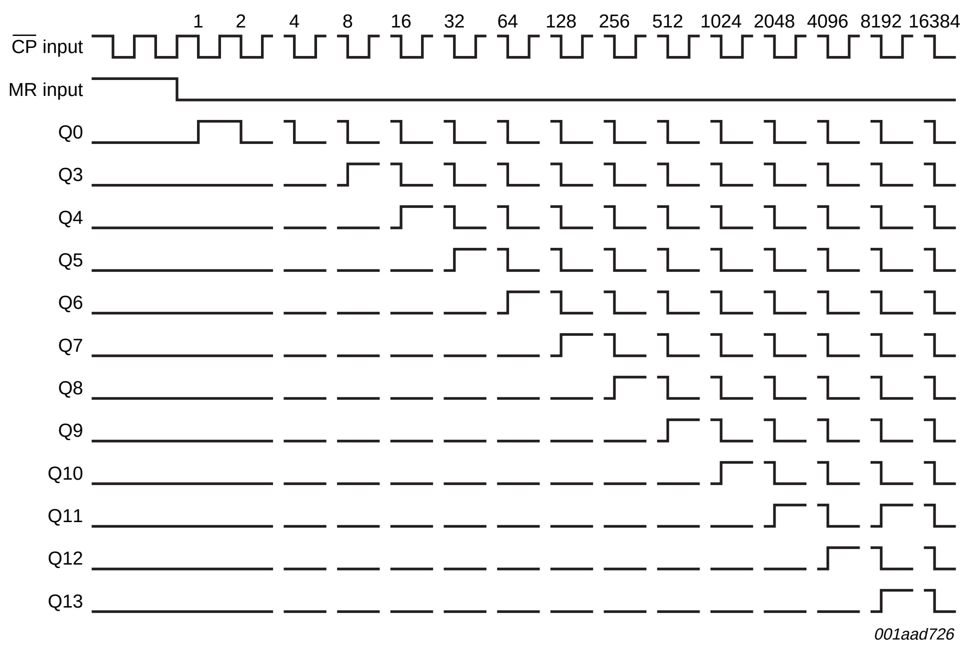


Fig 6. Timing diagram

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±50	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C				
	DIP16 package		[1]	-	750	mW
	SO16 package		[2]	-	500	mW
	SSOP16 and TSSOP16 packages		[3]	-	400	mW

[1] Above $T_{amb} = 70$ °C: P_{tot} derates linearly with 12 mW/K.

[2] Above $T_{amb} = 70$ °C: P_{tot} derates linearly with 8 mW/K.

[3] Above $T_{amb} = 60$ °C: P_{tot} derates linearly with 5.5 mW/K.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage		[1]	1.0	3.3	5.5	V
V_I	input voltage			0	-	V_{CC}	V
V_O	output voltage			0	-	V_{CC}	V
T_{amb}	ambient temperature			–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0$ V to 2.0 V		-	-	500	ns/V
		$V_{CC} = 2.0$ V to 2.7 V		-	-	200	ns/V
		$V_{CC} = 2.7$ V to 3.6 V		-	-	100	ns/V
		$V_{CC} = 3.6$ V to 5.5 V		-	-	50	ns/V

[1] The static characteristics are guaranteed from $V_{CC} = 1.2$ V to $V_{CC} = 5.5$ V, but LV devices are guaranteed to function down to $V_{CC} = 1.0$ V (with input levels GND or V_{CC}).

11. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-state input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 µA; V_{CC} = 1.2 V	-	1.2	-	V
		I_O = –100 µA; V_{CC} = 2.0 V	1.8	2.0	-	V
		I_O = –100 µA; V_{CC} = 2.7 V	2.5	2.7	-	V
		I_O = –100 µA; V_{CC} = 3.0 V	2.8	3.0	-	V
		I_O = –100 µA; V_{CC} = 4.5 V	4.3	4.5	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.40	2.82	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.60	4.20	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.2 V	-	0	-	V
		I_O = 100 µA; V_{CC} = 2.0 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 2.7 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 3.0 V	-	0	0.2	V
		I_O = 100 µA; V_{CC} = 4.5 V	-	0	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	µA
ΔI_{CC}	additional quiescent supply current	per input; V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 1.2 V	0.9	-	-	V
		V_{CC} = 2.0 V	1.4	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-state input voltage	V_{CC} = 1.2 V	-	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 μA; V_{CC} = 1.2 V	-	-	-	V
		I_O = –100 μA; V_{CC} = 2.0 V	1.8	-	-	V
		I_O = –100 μA; V_{CC} = 2.7 V	2.5	-	-	V
		I_O = –100 μA; V_{CC} = 3.0 V	2.8	-	-	V
		I_O = –100 μA; V_{CC} = 4.5 V	4.3	-	-	V
		I_O = –6 mA; V_{CC} = 3.0 V	2.20	-	-	V
		I_O = –12 mA; V_{CC} = 4.5 V	3.50	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.2 V	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	-	0.2	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	-	0.50	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	-	0.65	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	μA
ΔI_{CC}	additional quiescent supply current	per input; V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	850	μA

[1] All typical values are measured at T_{amb} = 25 °C.

12. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; for test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
t_{PHL}, t_{PLH}	propagation delay					
	$\overline{CP}$ to Q0	see Figure 7				
		V_{CC} = 1.2 V	-	60	-	ns
		V_{CC} = 2.0 V	-	27	43	ns
		V_{CC} = 2.7 V	-	19	31	ns
		V_{CC} = 3.0 V to 3.6 V	-	16	26	ns
		V_{CC} = 4.5 V to 5.5 V	-	11	17	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	12	-	ns
	Qn to Q(n+1)	see Figure 7				
		V_{CC} = 1.2 V	-	40	-	ns
		V_{CC} = 2.0 V	-	18	29	ns
		V_{CC} = 2.7 V	-	13	21	ns
		V_{CC} = 3.0 V to 3.6 V	-	11	18	ns
		V_{CC} = 4.5 V to 5.5 V	-	7	12	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	7	-	ns
t_{PHL}	propagation delay					
	MR to Qn	see Figure 8				
		V_{CC} = 1.2 V	-	55	-	ns
		V_{CC} = 2.0 V	-	27	44	ns
		V_{CC} = 2.7 V	-	19	31	ns
		V_{CC} = 3.0 V to 3.6 V	-	16	26	ns
		V_{CC} = 4.5 V to 5.5 V	-	11	17	ns
		V_{CC} = 3.3 V; C_L = 15 pF	-	16	-	ns
t_W	pulse width					
	$\overline{CP}$ (HIGH and LOW)	see Figure 7				
		V_{CC} = 2.0 V	35	7	-	ns
		V_{CC} = 2.7 V	25	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	20	4	-	ns
		V_{CC} = 4.5 V to 5.5 V	15	3	-	ns
	MR (HIGH)	see Figure 8				
		V_{CC} = 2.0 V	35	11	-	ns
		V_{CC} = 2.7 V	25	9	-	ns
		V_{CC} = 3.0 V to 3.6 V	20	8	-	ns
		V_{CC} = 4.5 V to 5.5 V	15	7	-	ns

Table 8: Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; for test circuit see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rec}	recovery time						
	MR to $\overline{CP}$	see Figure 8					
		V_{CC} = 1.2 V		-	10	-	ns
		V_{CC} = 2.0 V		22	5	-	ns
		V_{CC} = 2.7 V		16	4	-	ns
		V_{CC} = 3.0 V to 3.6 V		13	3	-	ns
		V_{CC} = 4.5 V to 5.5 V		10	2	-	ns
f_{max}	maximum input clock frequency	see Figure 7					
		V_{CC} = 2.0 V		14	60	-	MHz
		V_{CC} = 2.7 V		19	76	-	MHz
		V_{CC} = 3.0 V to 3.6 V		24	94	-	MHz
		V_{CC} = 4.5 V to 5.5 V		36	112	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	100	-	MHz
C_{PD}	power dissipation capacitance	per gate; V_I = GND to V_{CC}	[2]	-	20	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay						
	$\overline{CP}$ to Q0	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	54	ns
		V_{CC} = 2.7 V		-	-	38	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	32	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	22	ns
	Qn to Q(n+1)	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	37	ns
		V_{CC} = 2.7 V		-	-	26	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	22	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	15	ns
t_{PHL}	propagation delay						
	MR to Qn	see Figure 8					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.0 V		-	-	55	ns
		V_{CC} = 2.7 V		-	-	39	ns
		V_{CC} = 3.0 V to 3.6 V		-	-	32	ns
		V_{CC} = 4.5 V to 5.5 V		-	-	22	ns

Table 8: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; for test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width					
	$\overline{CP}$ (HIGH and LOW)	see Figure 7				
		V_{CC} = 2.0 V	41	-	-	ns
		V_{CC} = 2.7 V	30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	24	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	18	-	-	ns
	MR (HIGH)	see Figure 8				
		V_{CC} = 2.0 V	41	-	-	ns
		V_{CC} = 2.7 V	30	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	24	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	18	-	-	ns
t_{rec}	recovery time					
	MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.0 V	26	-	-	ns
		V_{CC} = 2.7 V	19	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	15	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	12	-	-	ns
f_{max}	maximum input clock frequency	see Figure 7				
		V_{CC} = 2.0 V	12	-	-	MHz
		V_{CC} = 2.7 V	16	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	20	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	30	-	-	MHz

[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

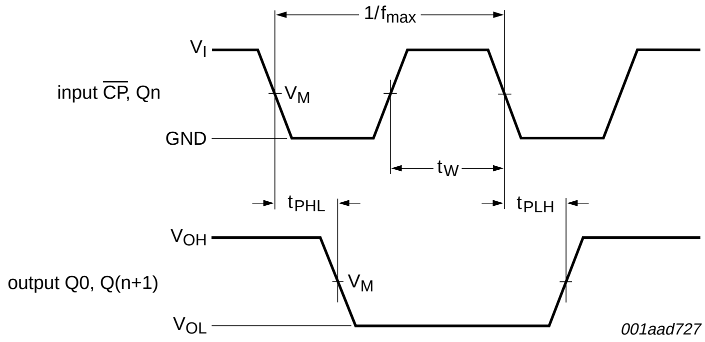
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

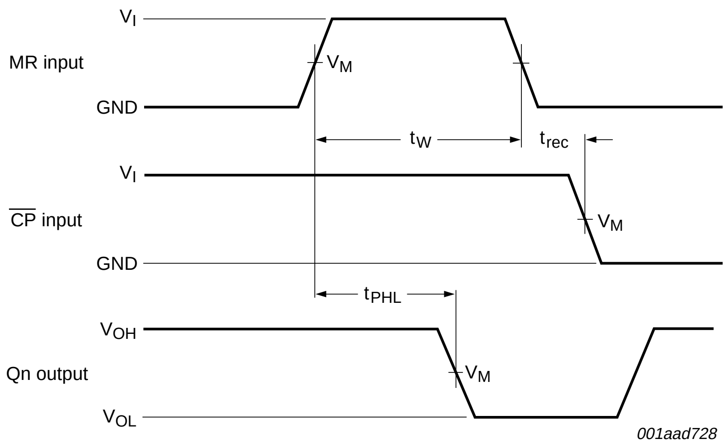
13. Waveforms



Measurement points: $V_M = 0.5 \times V_{CC}$.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

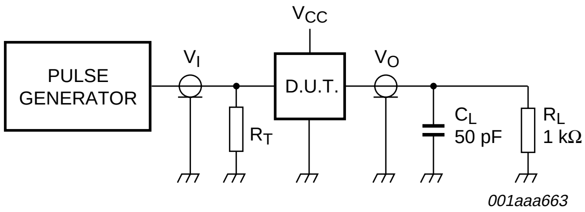
Fig 7. Propagation delay clock ($\overline{CP}$) to output (Qn), clock pulse width and maximum clock frequency



Measurement points: $V_M = 0.5 \times V_{CC}$.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 8. Propagation delay master reset (MR) to output (Qn), pulse width master reset (MR) and removal time master reset (MR) to clock ($\overline{CP}$)



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

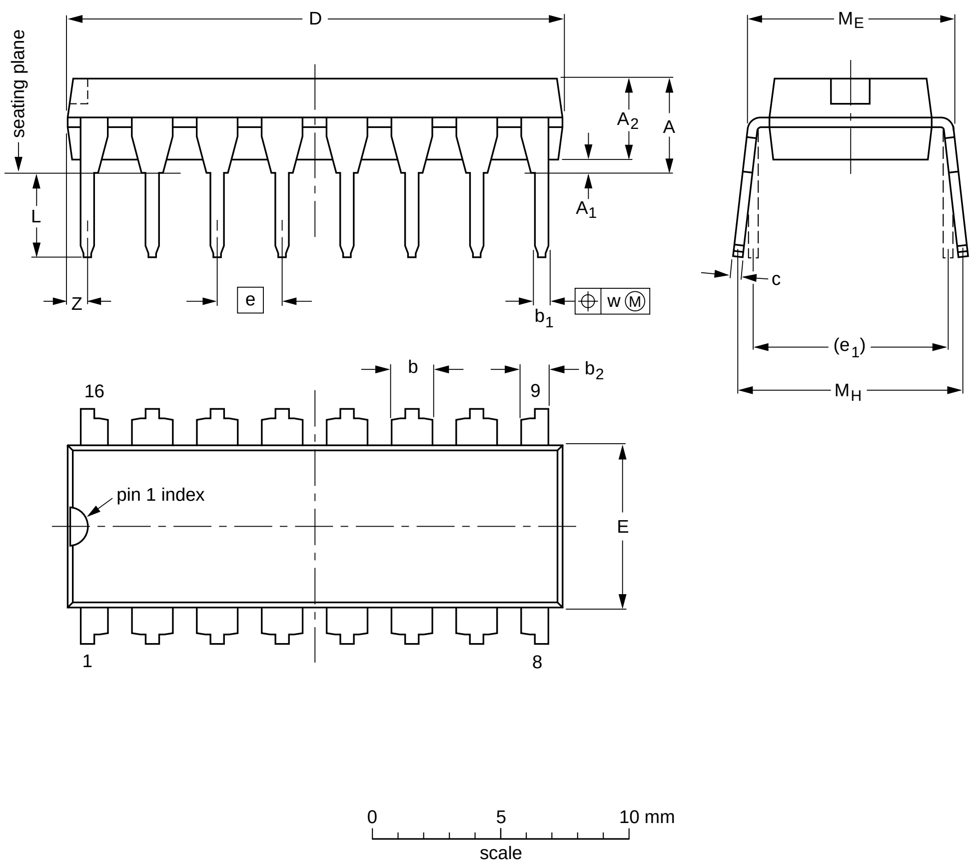
Fig 9. Load circuitry for switching times

Table 9: Test data

Supply voltage	Input		Load		Test
V_{CC}	V_I	t_r, t_f	C_L	R_L	
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.0 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF, 15 pF	1 kΩ	t_{PHL}, t_{PLH}
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

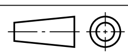
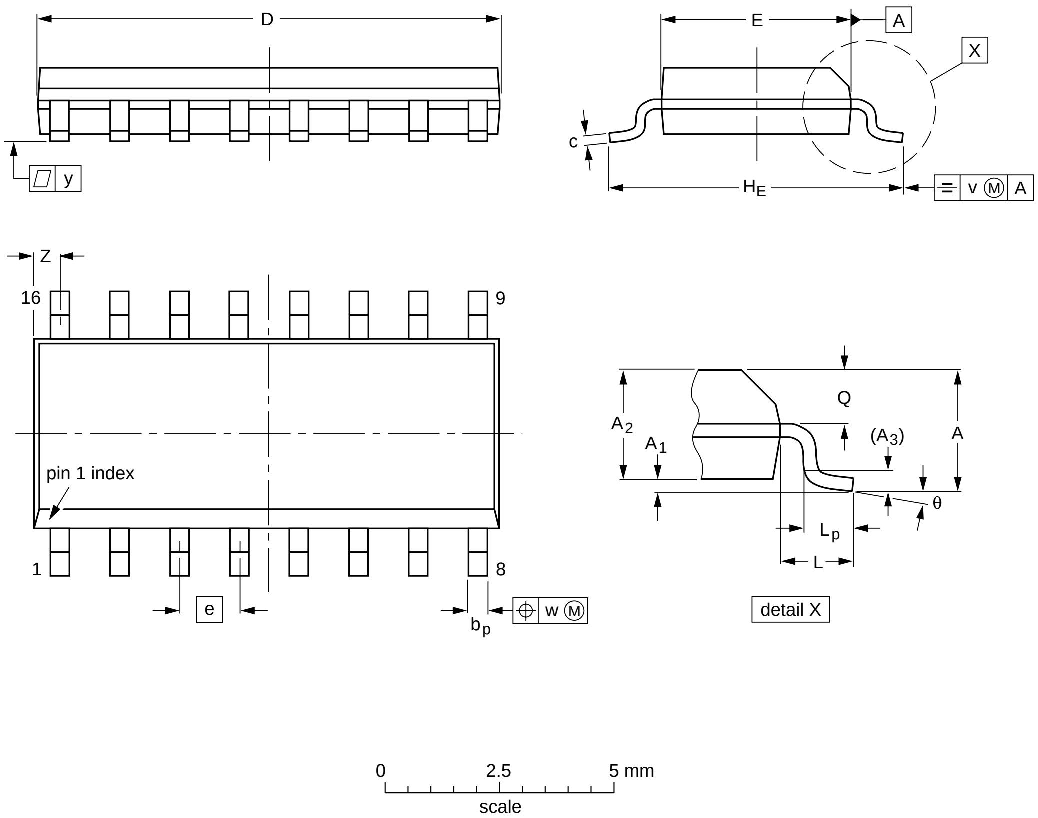
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 10. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

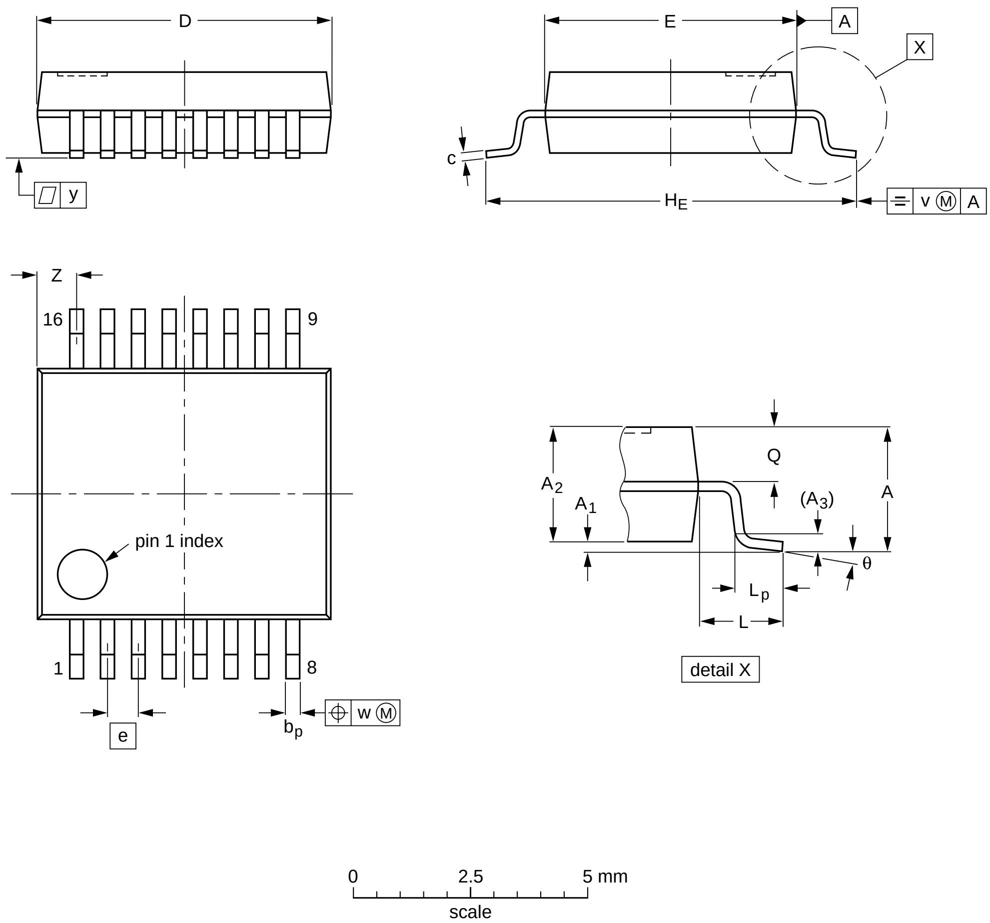
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

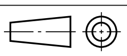
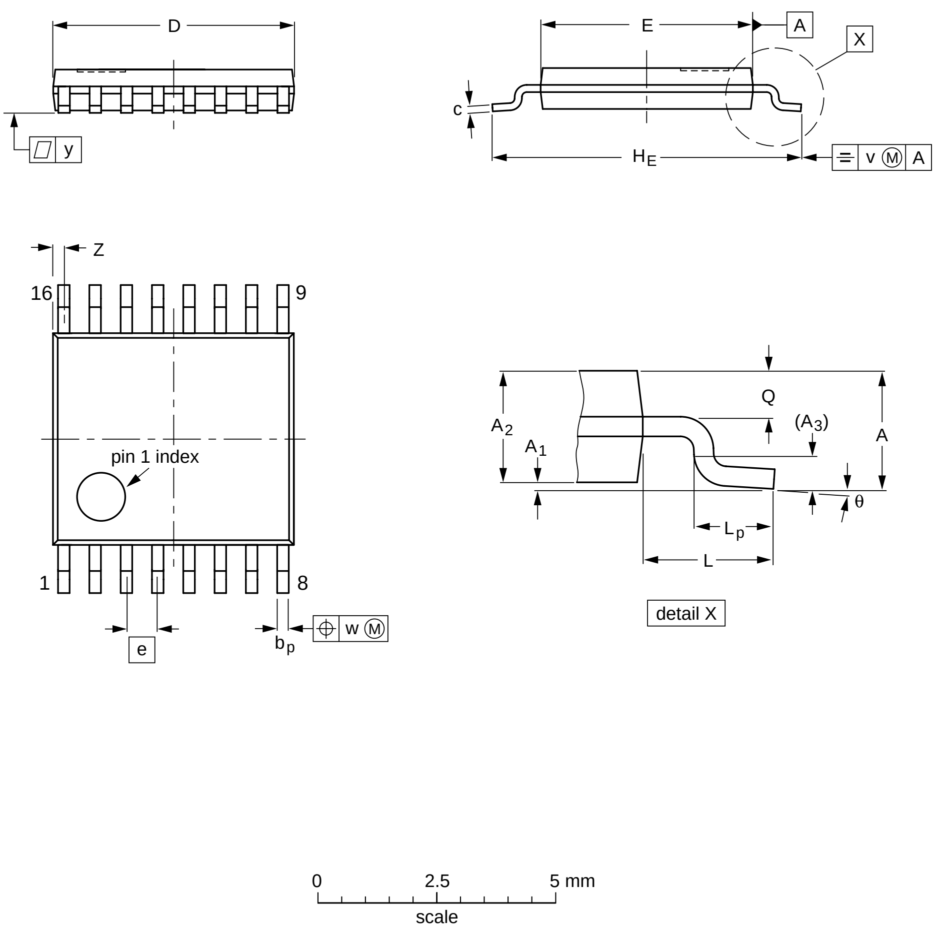
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT403-1 (TSSOP16)

15. Abbreviations

Table 10: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model

16. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LV4020_1	20051129	Product data sheet	-	-	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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