

NX3L4053

Triple low-ohmic single-pole double-throw analog switch

Rev. 5.1 — 30 March 2021

Product data sheet

1 General description

The NX3L4053 is a triple low-ohmic single-pole double-throw analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (nS), two independent inputs/outputs (nY0 and nY1) and a common input/output (nZ). All three switches share an enable input (\bar{E}). A digital enable pin \bar{E} is common to all switches. When \bar{E} is HIGH, the switches are turned off.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC} . This makes it possible for the NX3L4053 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3L4053 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ. Its low ON resistance (0.5 Ω) and flatness (0.13 Ω) ensures minimal attenuation and distortion of transmitted signals.

2 Features and benefits

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
 - 1.8 Ω (typical) at $V_{CC} = 1.4$ V
 - 1.0 Ω (typical) at $V_{CC} = 1.65$ V
 - 0.6 Ω (typical) at $V_{CC} = 2.3$ V
 - 0.6 Ω (typical) at $V_{CC} = 2.7$ V
 - 0.5 Ω (typical) at $V_{CC} = 4.3$ V
- Break-before-make switching
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 4000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
 - IEC61000-4-2 contact discharge exceeds 6000 V for switch ports
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- 1.8 V control logic at $V_{CC} = 3.6$ V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C



3 Applications

- Cell phone
- PDA
- Portable media player
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NX3L4053PW	X3L4053	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NX3L4053HR	M43	HXQFN16	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.5 mm	SOT1039-2

4.1 Ordering options

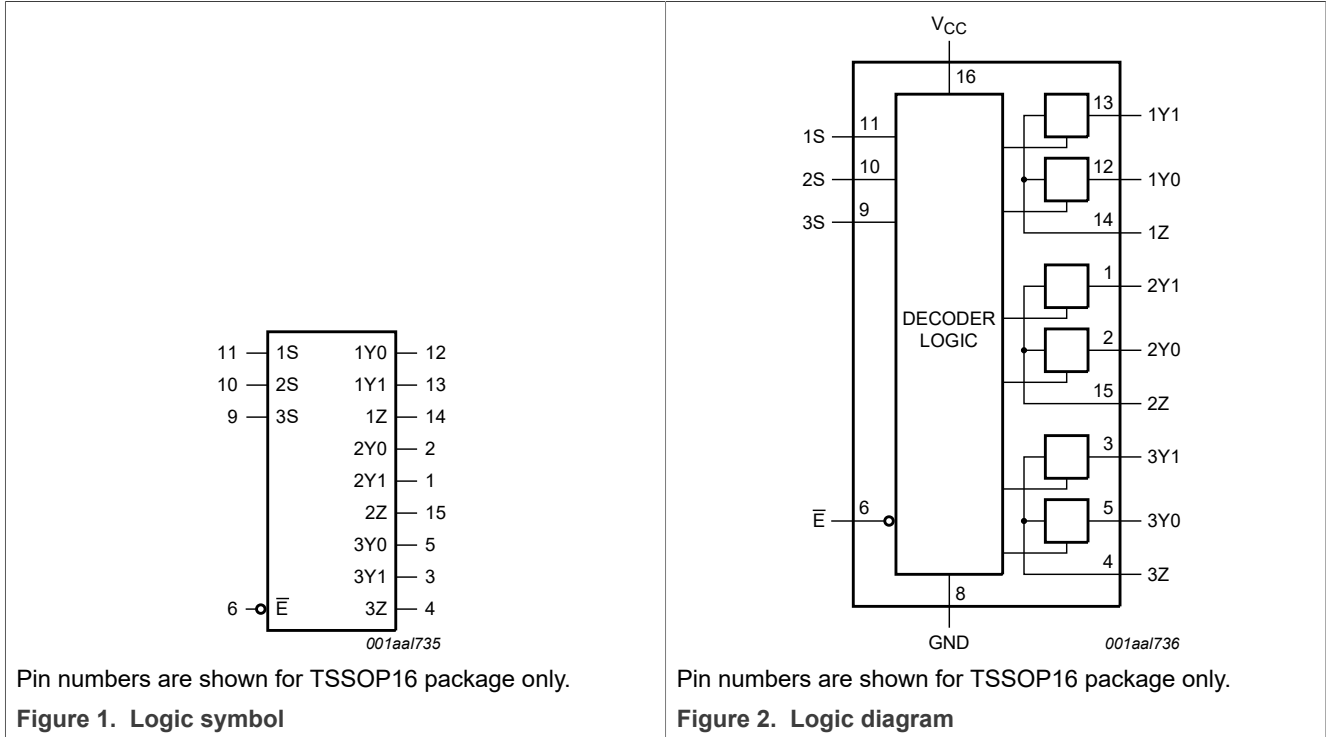
Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX3L4053PW	NX3L4053PW,118	TSSOP16	Reel 13" Q1/T1 NDP	2500	T _{amb} = -40 °C to +125 °C
NX3L4053HR	NX3L4053HRZ	HXQFN16	Reel 7" Q1/T1 NDP SSB ^[1]	1500	T _{amb} = -40 °C to +125 °C
	NX3L4053HR,115 ^[2]	HXQFN16	Reel 7" Q1/T1 NDP	1500	T _{amb} = -40 °C to +125 °C

[1] This packing method uses a Static Shielding Bag (SSB) solution. Material is to be kept in the sealed bag between uses.

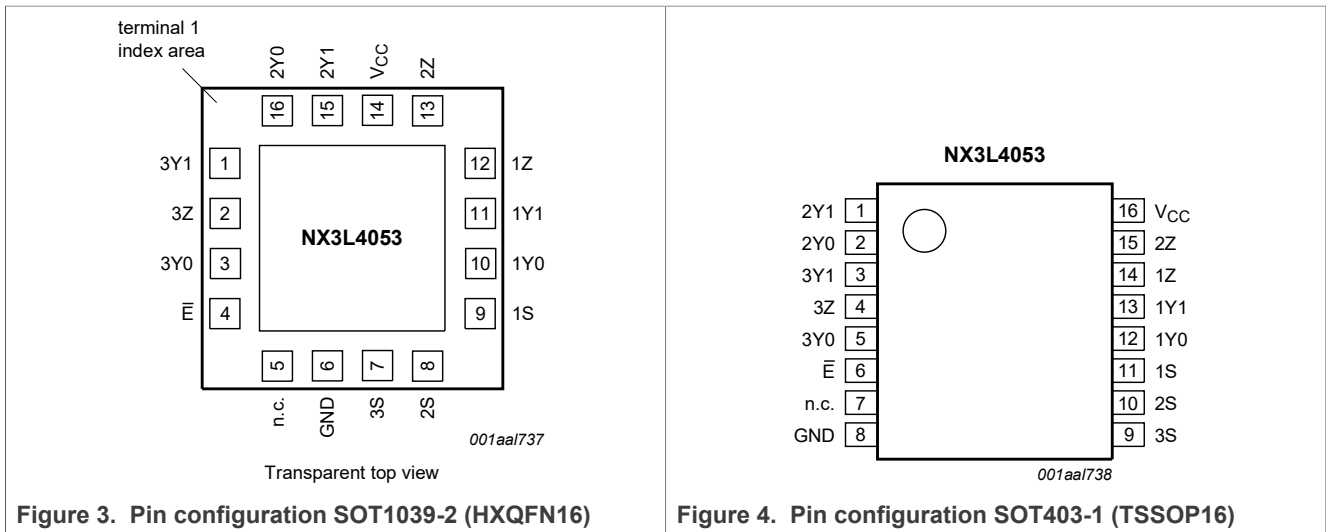
[2] Will go EOL - migrate to new leadframe NX3L2467HRZ orderable part number.

5 Functional diagram



6 Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1039-2	SOT403-1	
\bar{E}	4	6	enable input (active LOW)
n.c.	5	7	not connected
GND	6	8	ground (0 V)
1S, 2S, 3S	9, 8, 7	11, 10, 9	select input
1Y0, 2Y0, 3Y0	10, 16, 3	12, 2, 5	independent input or output
1Y1, 2Y1, 3Y1	11, 15, 1	13, 1, 3	independent input or output
1Z, 2Z, 3Z	12, 13, 2	14, 15, 4	independent output or input
V _{CC}	14	16	supply voltage

7 Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Channel on
\bar{E}	nS	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	switches off

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	nS and \bar{E}	^[1] -0.5	+4.6	V
V _{SW}	switch voltage		^[2] -0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±50	mA
I _{SW}	switch current	V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; source or sink current	-	±350	mA
		V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	±500	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		HXQFN16	^[3] -	250	mW

Table 5. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
		TSSOP16	[4]	-	500	mW

- [1] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.
- [3] For HXQFN16 package: above 135 °C the value of P_{tot} derates linearly with 16.9 mW/K.
- [4] For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			1.4	4.3	V
V _I	input voltage	nS and \bar{E}		0	4.3	V
V _{SW}	switch voltage		[1]	0	V _{CC}	V
T _{amb}	ambient temperature			-40	+125	°C
Δt/ΔV	input transition rise and fall rate	nS and \bar{E} ; V _{CC} = 1.4 V to 4.3 V		-	200	ns/V

- [1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nYn. In this case, there is no limit for the voltage drop across the switch.

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

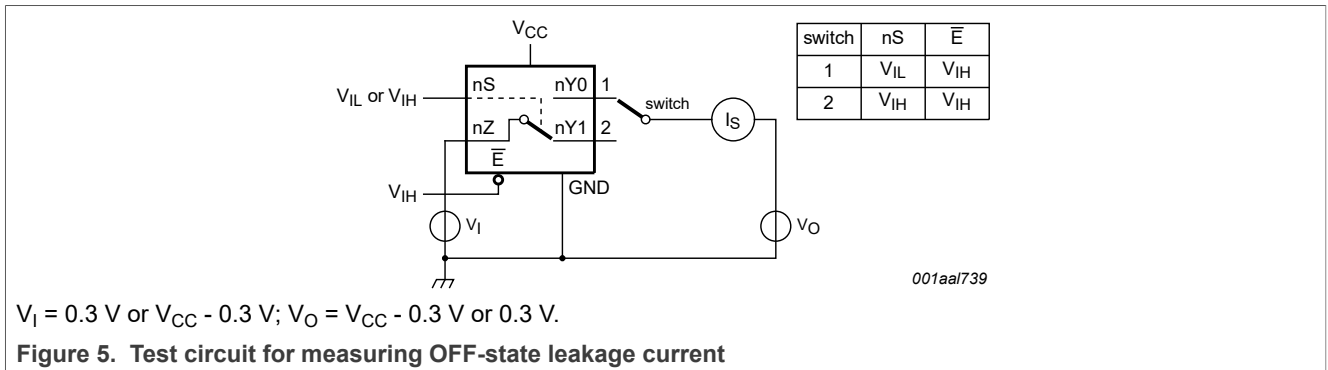
Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.4 V to 1.6 V	0.9	-	-	0.9	-	-	V
		V _{CC} = 1.65 V to 1.95 V	0.9	-	-	0.9	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.1	-	-	1.1	-	-	V
		V _{CC} = 2.7 V to 3.6 V	1.3	-	-	1.3	-	-	V
		V _{CC} = 3.6 V to 4.3 V	1.4	-	-	1.4	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.4 V to 1.6 V	-	-	0.3	-	0.3	0.3	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.4	-	0.4	0.3	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.4	-	0.4	0.4	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	0.5	V
		V _{CC} = 3.6 V to 4.3 V	-	-	0.6	-	0.6	0.6	V
I _I	input leakage current	nS and \bar{E} ; V _I = GND to 4.3 V; V _{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	±1	μA

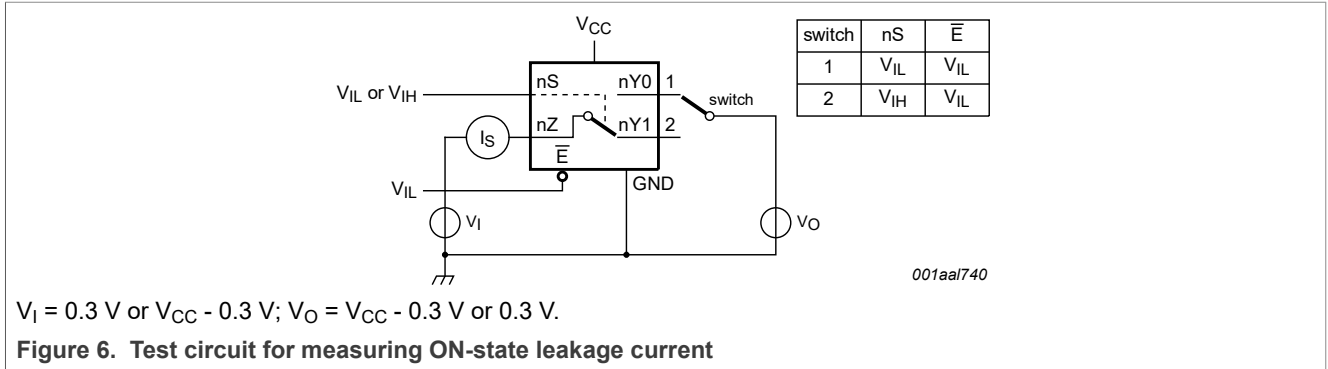
Table 7. Static characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
I _{S(OFF)}	OFF-state leakage current	nY0 and nY1 port; see Figure 5							
		V _{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V _{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
I _{S(ON)}	ON-state leakage current	nZ port; V _{CC} = 1.4 V to 3.6 V; see Figure 6							
		V _{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V _{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{SW} = GND or V _{CC}							
		V _{CC} = 3.6 V	-	-	100	-	500	5000	nA
		V _{CC} = 4.3 V	-	-	150	-	800	6000	nA
ΔI _{CC}	additional supply current	V _{SW} = GND or V _{CC}							
		V _I = 2.6 V; V _{CC} = 4.3 V	-	2.0	4.0	-	7	7	μA
		V _I = 2.6 V; V _{CC} = 3.6 V	-	0.35	0.7	-	1	1	μA
		V _I = 1.8 V; V _{CC} = 4.3 V	-	7.0	10.0	-	15	15	μA
		V _I = 1.8 V; V _{CC} = 3.6 V	-	2.5	4.0	-	5	5	μA
		V _I = 1.8 V; V _{CC} = 2.5 V	-	50	200	-	300	500	nA
C _I	input capacitance	nS and \bar{E}	-	1.0	-	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	35	-	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	130	-	-	-	-	pF

10.1 Test circuits





10.2 ON resistance

Table 8. ON resistance^[1]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see [Figure 8](#) to [Figure 14](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[2]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; I _{SW} = 100 mA; see Figure 7						
		V _{CC} = 1.4 V	-	1.8	3.8	-	4.2	Ω
		V _{CC} = 1.65 V	-	1.0	1.7	-	1.8	Ω
		V _{CC} = 2.3 V	-	0.6	0.9	-	1.0	Ω
		V _{CC} = 2.7 V	-	0.6	0.80	-	1.0	Ω
		V _{CC} = 4.3 V	-	0.5	0.80	-	1.0	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I = GND to V _{CC} ; I _{SW} = 100 mA ^[3]						
		V _{CC} = 1.4 V; V _{SW} = 0.4 V	-	0.23	0.38	-	0.38	Ω
		V _{CC} = 1.65 V; V _{SW} = 0.5 V	-	0.23	0.28	-	0.38	Ω
		V _{CC} = 2.3 V; V _{SW} = 0.7 V	-	0.12	0.15	-	0.18	Ω
		V _{CC} = 2.7 V; V _{SW} = 0.8 V	-	0.12	0.15	-	0.18	Ω
		V _{CC} = 4.3 V; V _{SW} = 0.8 V	-	0.12	0.15	-	0.18	Ω
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} ; I _{SW} = 100 mA ^[4]						
		V _{CC} = 1.4 V	-	1.0	3.3	-	3.6	Ω
		V _{CC} = 1.65 V	-	0.5	1.2	-	1.3	Ω
		V _{CC} = 2.3 V	-	0.15	0.3	-	0.35	Ω
		V _{CC} = 2.7 V	-	0.13	0.3	-	0.35	Ω
		V _{CC} = 4.3 V	-	0.2	0.4	-	0.45	Ω

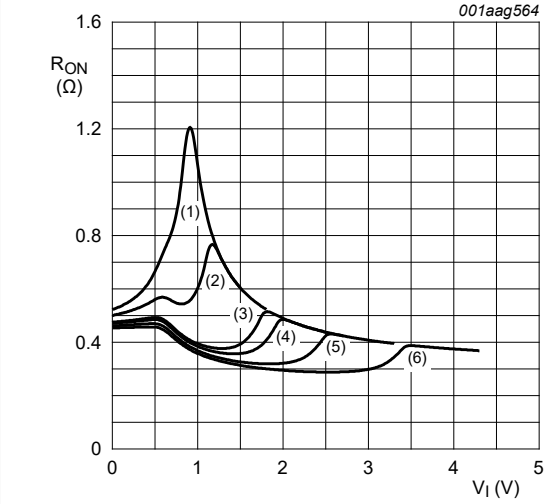
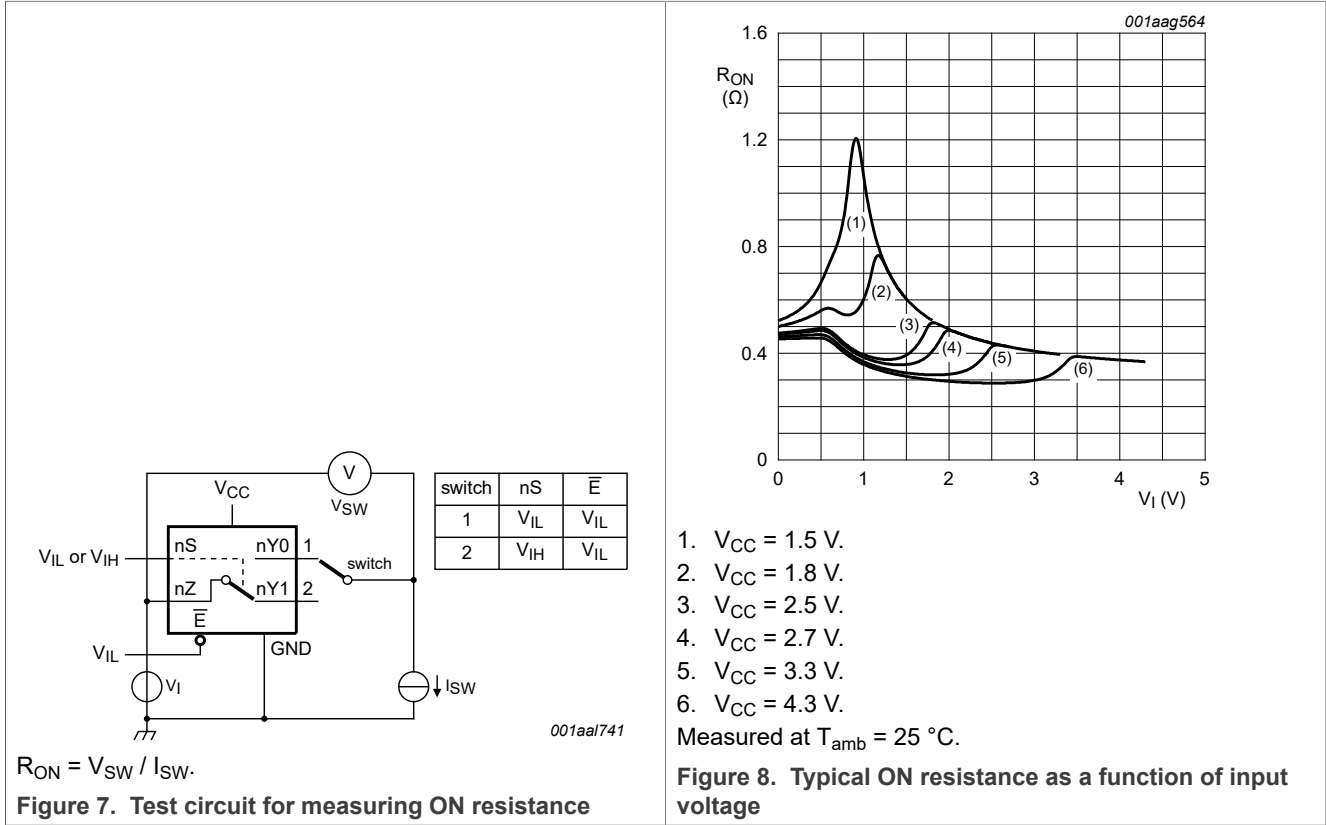
[1] For NX3L4053PW (TSSOP16 package), all ON resistance values are up to 0.05 Ω higher.

[2] Typical values are measured at T_{amb} = 25 °C.

[3] Measured at identical V_{CC}, temperature and input voltage.

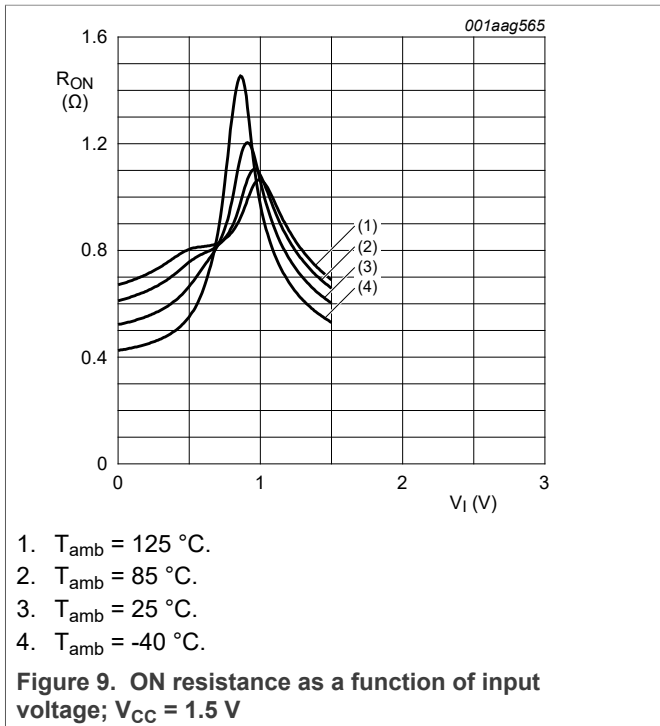
[4] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.3 ON resistance test circuit and graphs



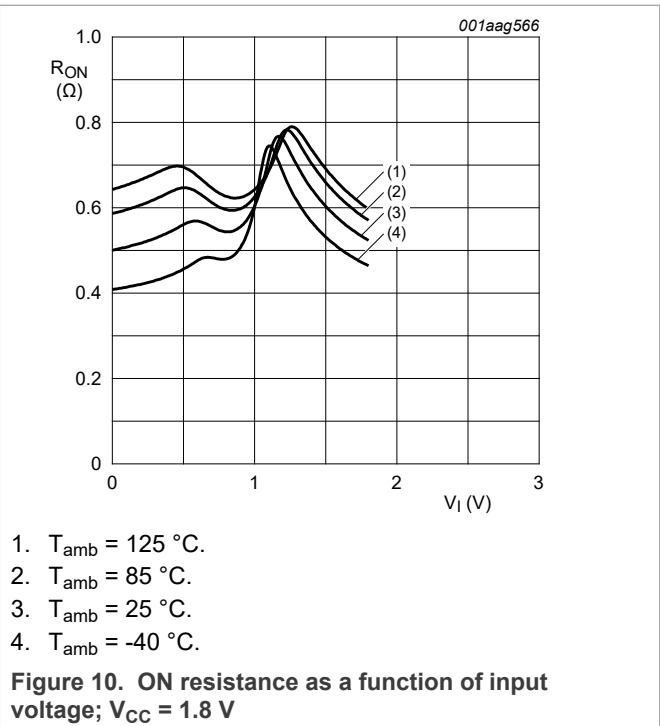
1. V_{CC} = 1.5 V.
 2. V_{CC} = 1.8 V.
 3. V_{CC} = 2.5 V.
 4. V_{CC} = 2.7 V.
 5. V_{CC} = 3.3 V.
 6. V_{CC} = 4.3 V.
- Measured at T_{amb} = 25 °C.

Figure 8. Typical ON resistance as a function of input voltage



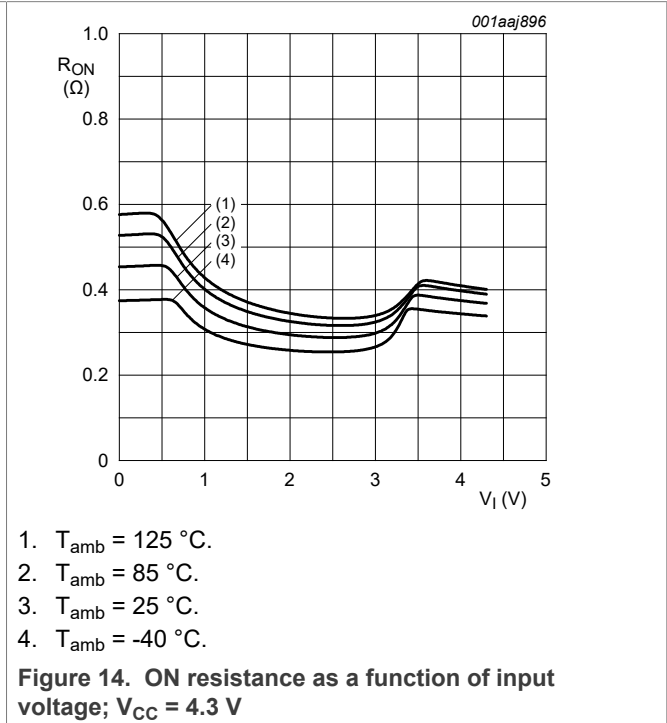
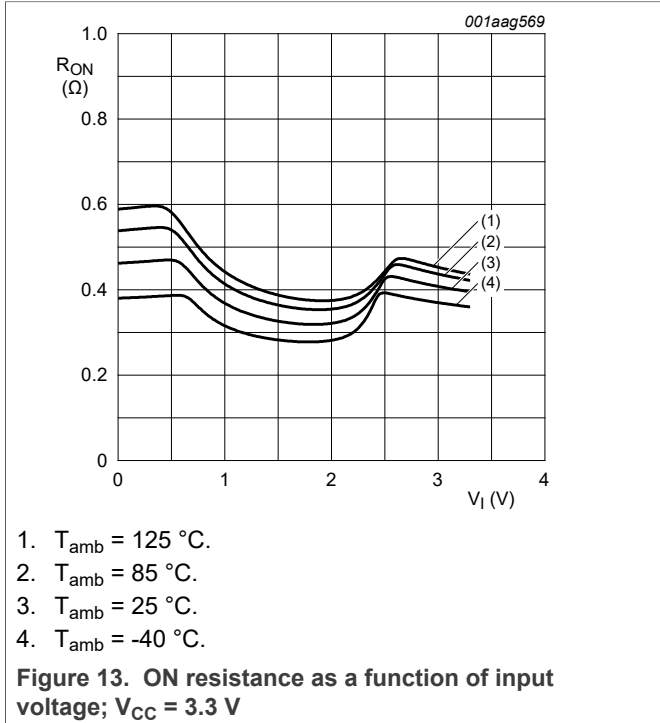
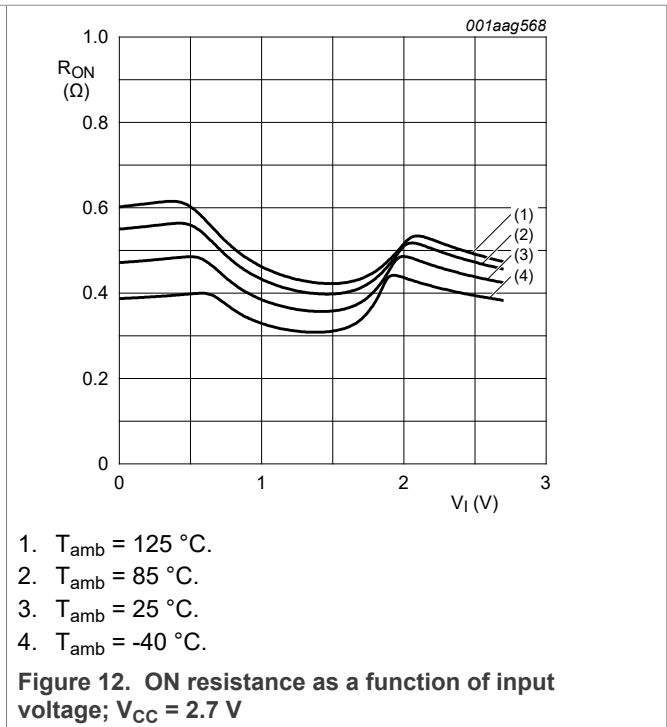
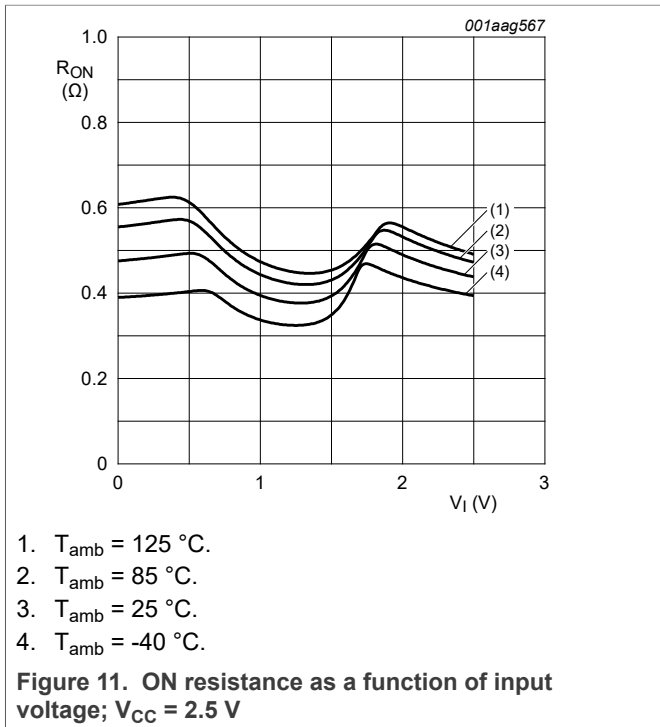
1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 9. ON resistance as a function of input voltage; V_{CC} = 1.5 V



1. T_{amb} = 125 °C.
2. T_{amb} = 85 °C.
3. T_{amb} = 25 °C.
4. T_{amb} = -40 °C.

Figure 10. ON resistance as a function of input voltage; V_{CC} = 1.8 V



11 Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 17.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C			Unit
			Min	Typ ^[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t _{en}	enable time	E, nS to nZ or nYn; see Figure 15							
		V _{CC} = 1.4 V to 1.6 V	-	49	90	-	120	120	ns
		V _{CC} = 1.65 V to 1.95 V	-	35	70	-	80	90	ns
		V _{CC} = 2.3 V to 2.7 V	-	23	45	-	50	55	ns
		V _{CC} = 2.7 V to 3.6 V	-	21	40	-	45	50	ns
		V _{CC} = 3.6 V to 4.3 V	-	21	40	-	45	50	ns
t _{dis}	disable time	E, nS to nZ or nYn; see Figure 15							
		V _{CC} = 1.4 V to 1.6 V	-	32	70	-	80	90	ns
		V _{CC} = 1.65 V to 1.95 V	-	17	55	-	60	65	ns
		V _{CC} = 2.3 V to 2.7 V	-	11	25	-	30	35	ns
		V _{CC} = 2.7 V to 3.6 V	-	8	20	-	25	30	ns
		V _{CC} = 3.6 V to 4.3 V	-	8	20	-	25	30	ns
t _{b-m}	break-before-make time	see Figure 16							
		V _{CC} = 1.4 V to 1.6 V	-	19	-	9	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	17	-	7	-	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	13	-	4	-	-	ns
		V _{CC} = 2.7 V to 3.6 V	-	10	-	3	-	-	ns
		V _{CC} = 3.6 V to 4.3 V	-	9	-	2	-	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

[2] Break-before-make guaranteed by design.

11.1 Waveform and test circuits

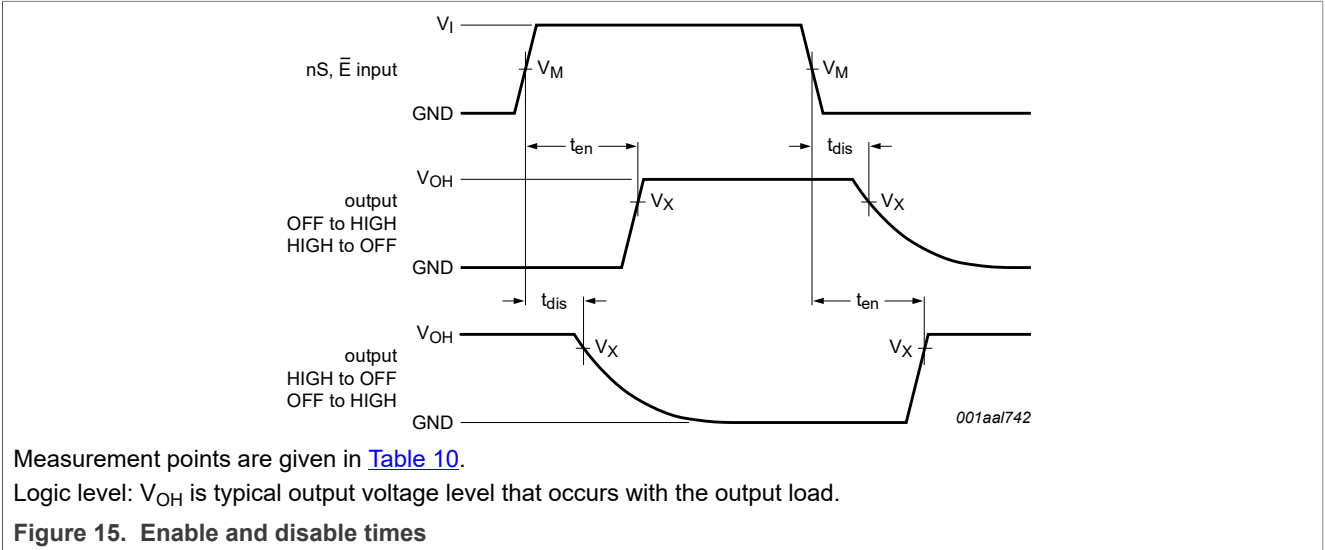


Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

Triple low-ohmic single-pole double-throw analog switch

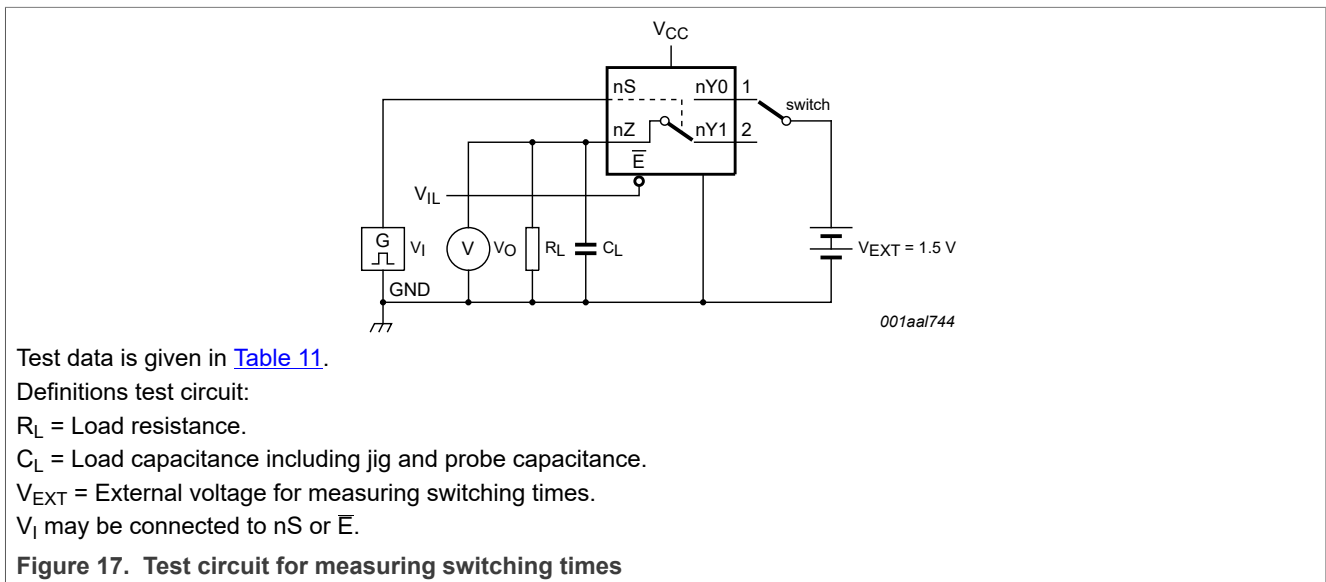
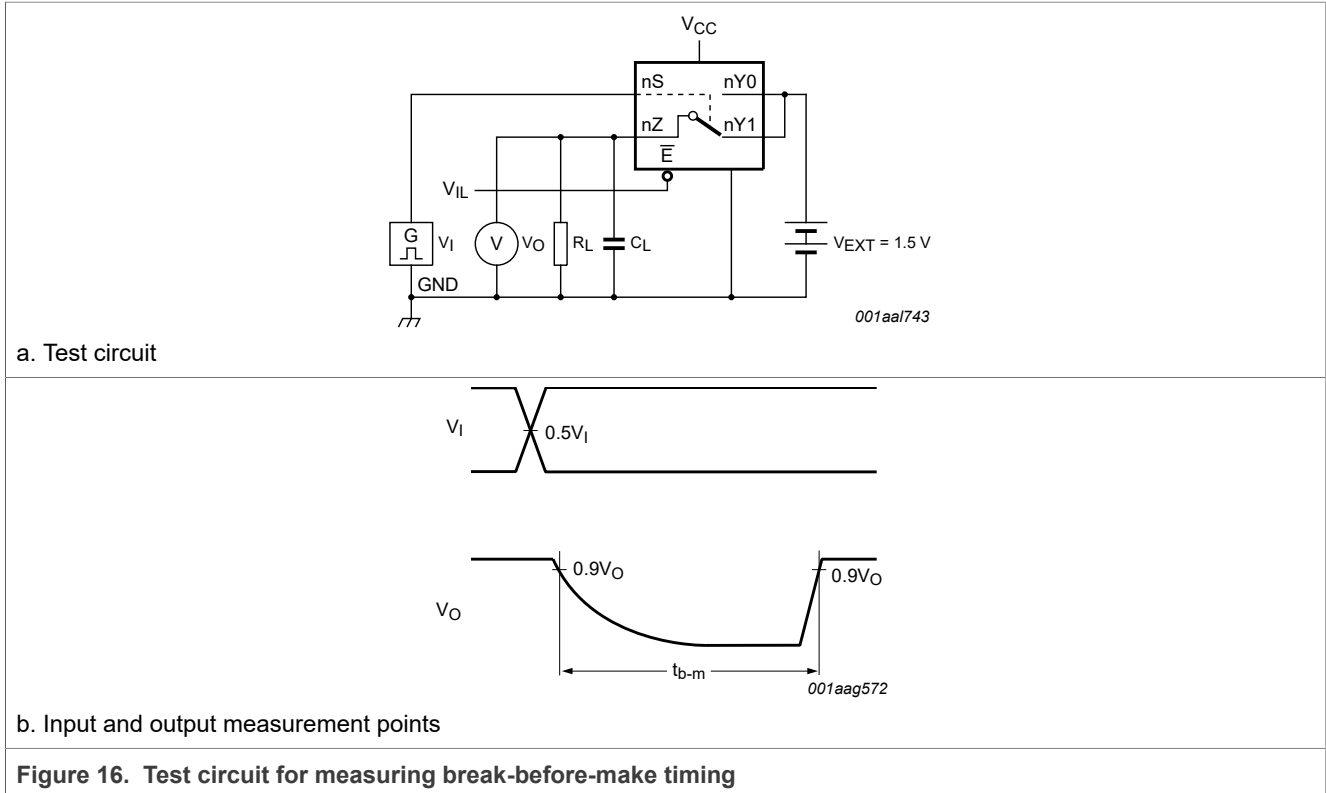


Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND or } V_{CC}$ (unless otherwise specified); $t_r = t_f \leq 2.5 \text{ ns}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
THD	total harmonic distortion	$f_i = 20 \text{ Hz to } 20 \text{ kHz}$; $R_L = 32 \text{ } \Omega$; see Figure 18	[1]				
		$V_{CC} = 1.4 \text{ V}$; $V_I = 1 \text{ V (p-p)}$		-	0.15	-	%
		$V_{CC} = 1.65 \text{ V}$; $V_I = 1.2 \text{ V (p-p)}$		-	0.10	-	%
		$V_{CC} = 2.3 \text{ V}$; $V_I = 1.5 \text{ V (p-p)}$		-	0.02	-	%
		$V_{CC} = 2.7 \text{ V}$; $V_I = 2 \text{ V (p-p)}$		-	0.02	-	%
		$V_{CC} = 4.3 \text{ V}$; $V_I = 2 \text{ V (p-p)}$		-	0.02	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50 \text{ } \Omega$; see Figure 19	[1]				
		$V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$		-	60	-	MHz
α_{iso}	isolation (OFF-state)	$f_i = 100 \text{ kHz}$; $R_L = 50 \text{ } \Omega$; see Figure 20	[1]				
		$V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$		-	-90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 50 \text{ } \Omega$; see Figure 21					
		$V_{CC} = 1.4 \text{ V to } 3.6 \text{ V}$		-	0.2	-	V
		$V_{CC} = 3.6 \text{ V to } 4.3 \text{ V}$		-	0.3	-	V
Xtalk	crosstalk	between switches; $f_i = 100 \text{ kHz}$; $R_L = 50 \text{ } \Omega$; see Figure 22	[1]				
		$V_{CC} = 1.4 \text{ V to } 4.3 \text{ V}$		-	-90	-	dB
Q_{inj}	charge injection	$f_i = 1 \text{ MHz}$; $C_L = 0.1 \text{ nF}$; $R_L = 1 \text{ M}\Omega$; $V_{\text{gen}} = 0 \text{ V}$; $R_{\text{gen}} = 0 \text{ } \Omega$; see Figure 23					
		$V_{CC} = 1.5 \text{ V}$		-	3	-	pC
		$V_{CC} = 1.8 \text{ V}$		-	4	-	pC
		$V_{CC} = 2.5 \text{ V}$		-	6	-	pC
		$V_{CC} = 3.3 \text{ V}$		-	9	-	pC
		$V_{CC} = 4.3 \text{ V}$		-	15	-	pC

[1] f_i is biased at $0.5V_{CC}$.

11.3 Test circuits

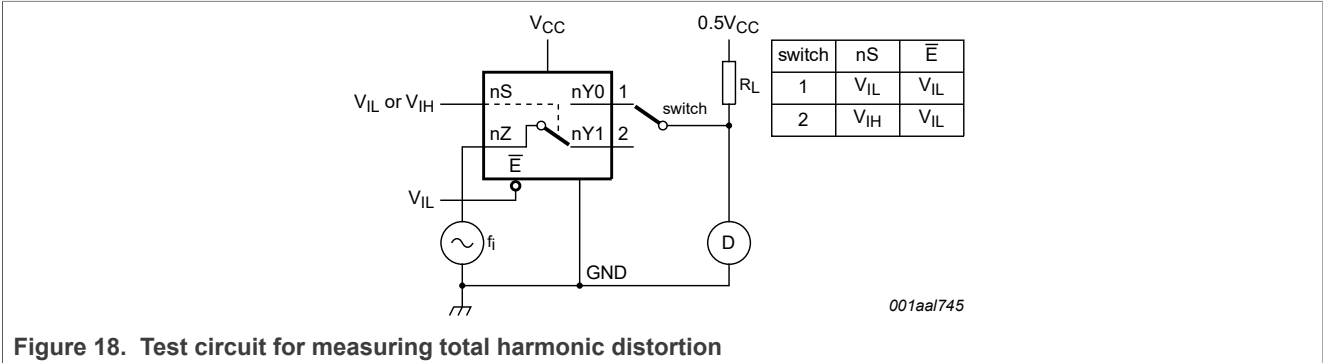


Figure 18. Test circuit for measuring total harmonic distortion

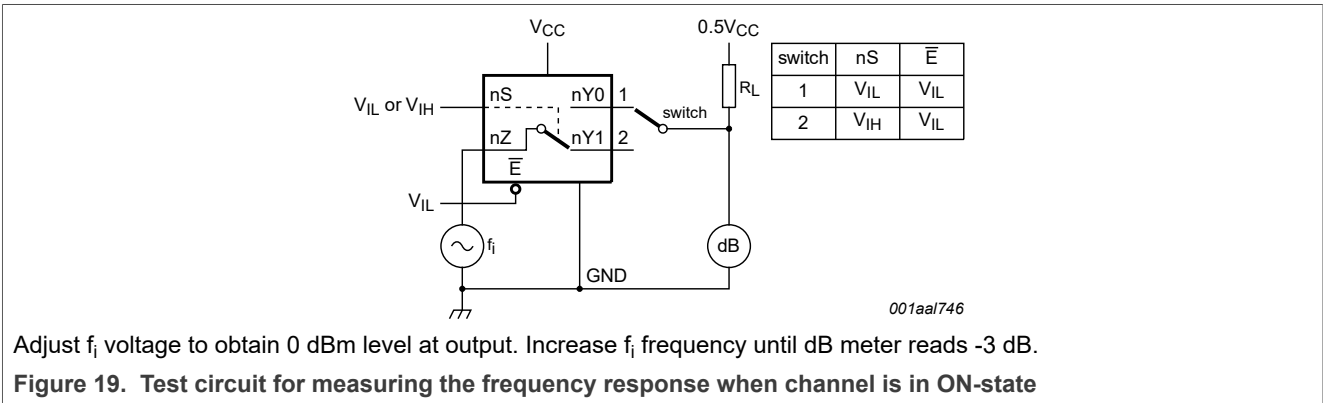


Figure 19. Test circuit for measuring the frequency response when channel is in ON-state

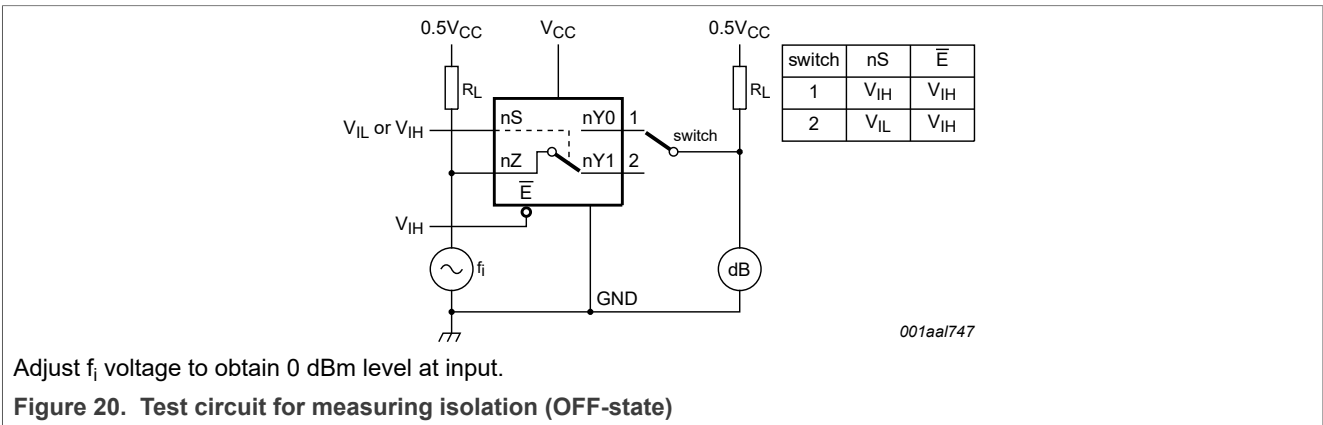


Figure 20. Test circuit for measuring isolation (OFF-state)

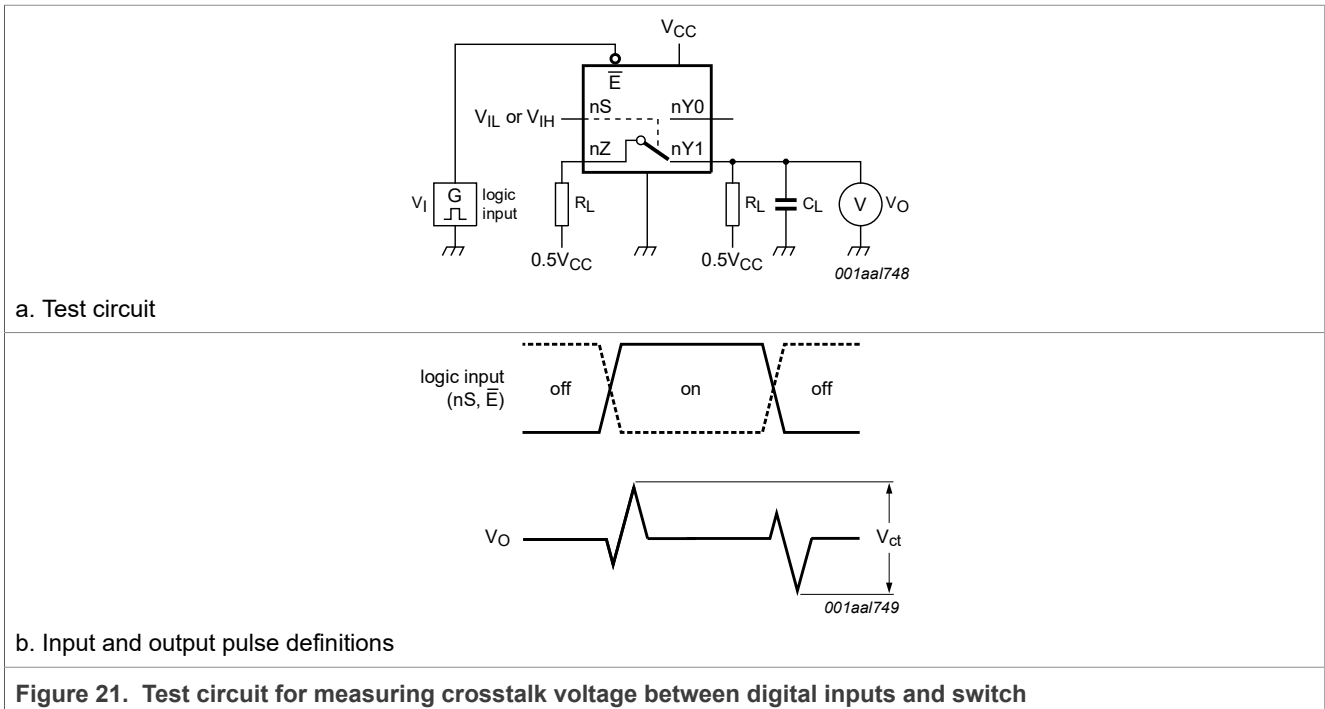


Figure 21. Test circuit for measuring crosstalk voltage between digital inputs and switch

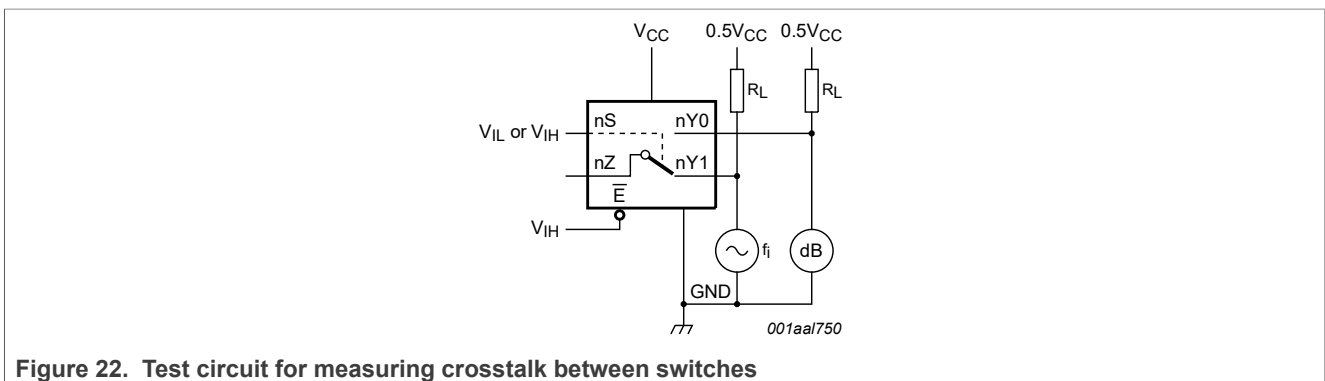


Figure 22. Test circuit for measuring crosstalk between switches

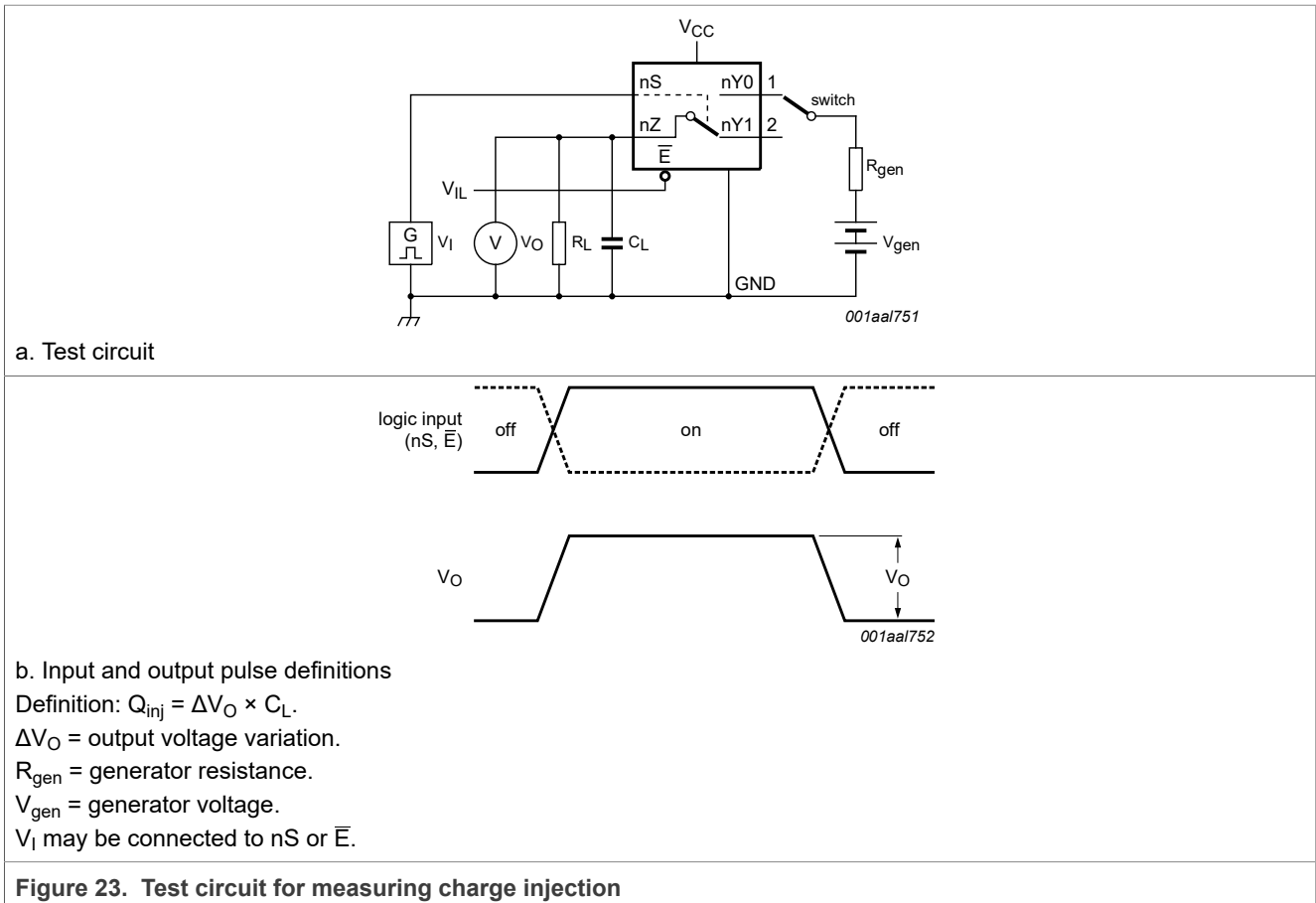


Figure 23. Test circuit for measuring charge injection

12 Package outline

HXQFN16(U): plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.5 mm

SOT1039-2

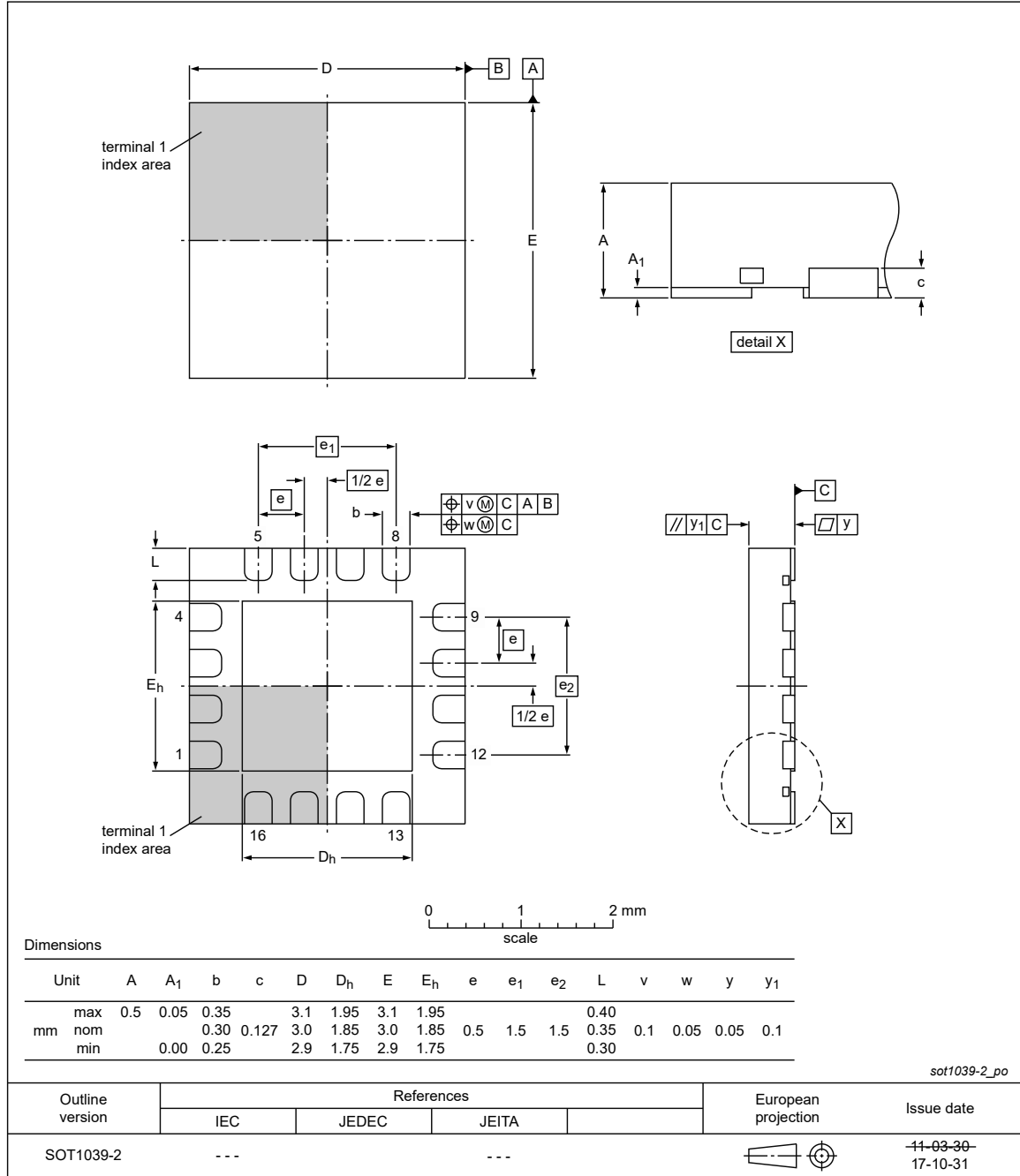
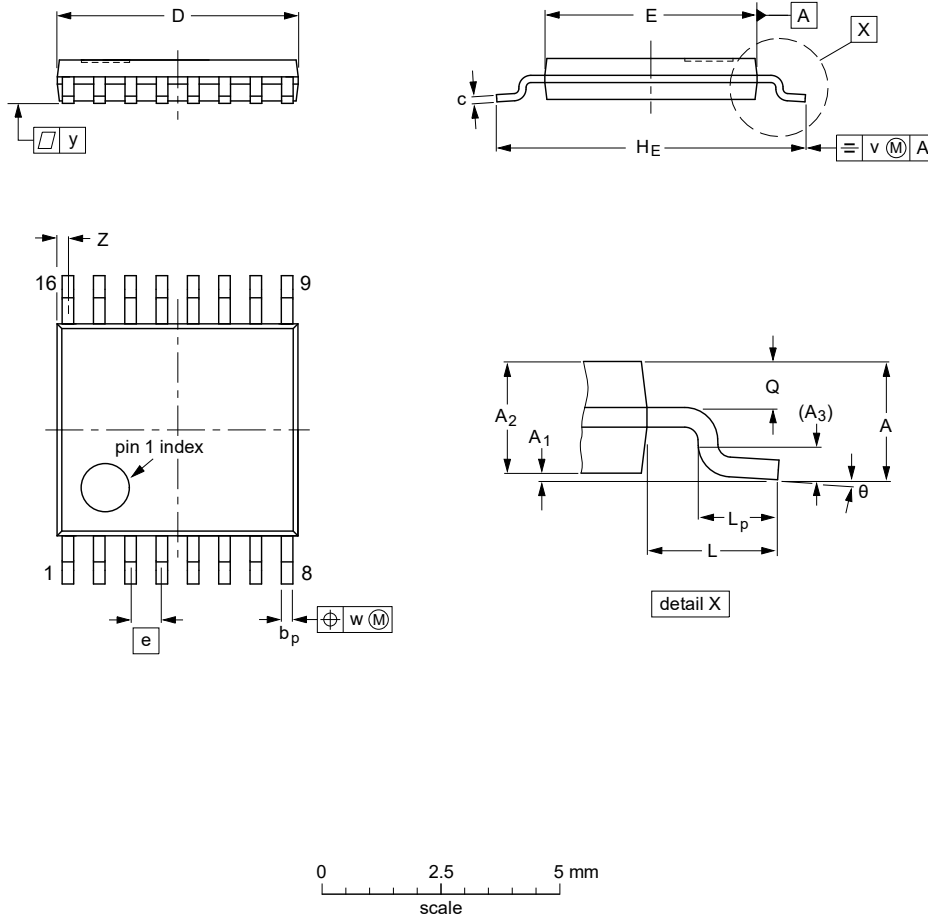


Figure 24. Package outline SOT1039-2 (HXQFN16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Figure 25. Package outline SOT403-1 (TSSOP16)

13 Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant

14 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3L4053 v.5.1	20210330	Product data sheet	-	NX3L4053 v.5
Modifications:	<ul style="list-style-type: none"> Updated Section 4 "Ordering information". 			
NX3L4053 v.5	20120625	Product data sheet	-	NX3L4053 v.4
NX3L4053 v.4	20111107	Product data sheet	-	NX3L4053 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
NX3L4053 v.3	20101223	Product data sheet	-	NX3L4053 v.2
NX3L4053 v.2	20100811	Product data sheet	-	NX3L4053 v.1
NX3L4053 v.1	20100416	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Triple low-ohmic single-pole double-throw analog switch

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