TFA9842J

2-channel audio amplifier; SE: 1 W to 7.5 W; BTL: 2 W to 15 W

Rev. 01 — 26 April 2004 **Preliminary data**

1. General description

The TFA9842J contains two identical audio power amplifiers. The TFA9842J can be used as two Single-Ended (SE) channels with a fixed gain of 26 dB or one Bridge-Tied Load (BTL) channel with a fixed gain of 32 dB.

The TFA9842J comes in a 9-pin DIL-bent-SIL (DBS9P) power package. The TFA9842J is pin compatible with the TFA9841J and TFA9843J.

The TFA9842J contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions with no unnecessary audio holes. Almost any supply voltage and load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heatsink and ambient temperature) allow it.

2. Features

- SE: 1 W to 7.5 W; BTL: 2 W to 15 W operation possibility
- Soft clipping
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Pin compatible with the TFA9841J and TFA9843J.

3. Applications

- Television
- PC speakers
- Boom box
- Mini and micro audio receivers.

PHILIPS

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	operating	9	17	26	V
		no signal	-	-	28	V
I_q	quiescent supply current	V_{CC} = 18 V; R_L = ∞	-	60	100	mA
I_{stb}	standby supply current		-	-	10	µA
P_o	output power	V_{CC} = 17 V; THD = 10 %				
		SE; R_L = 4 Ω	7	7.5	-	W
		BTL; R_L = 8 Ω	14	15	-	W
THD	total harmonic distortion	SE; P_o = 1 W	-	0.1	0.5	%
		BTL; P_o = 1 W	-	0.05	0.5	%
G_v	voltage gain	SE	25	26	27	dB
		BTL	31	32	33	dB
SVRR	supply voltage ripple rejection	f = 1 kHz				
		SE	-	60	-	dB
		BTL	-	65	-	dB

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TFA9842J	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad	SOT523 -1

6. Block diagram

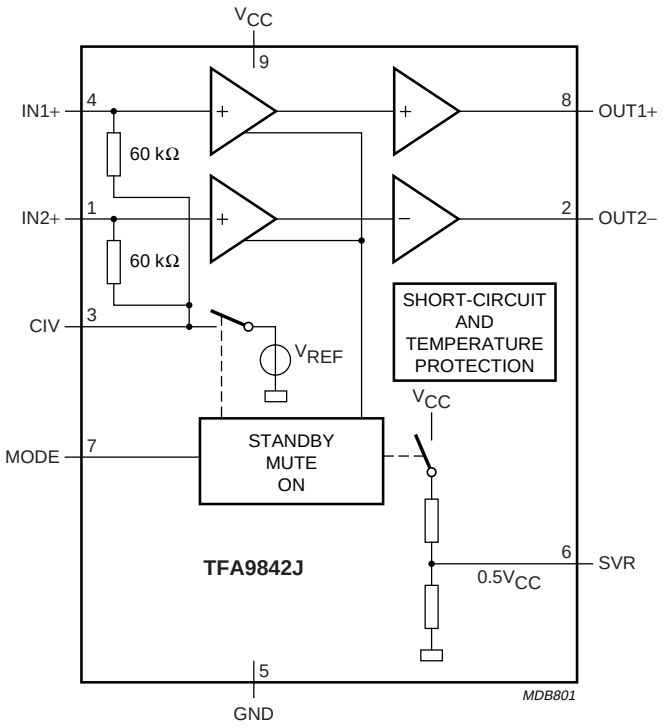


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

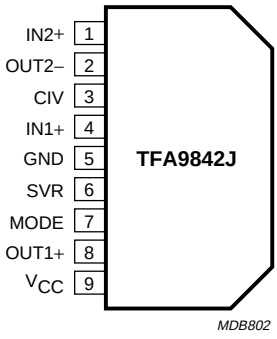


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
IN2+	1	input 2
OUT2–	2	inverted loudspeaker terminal 2
CIV	3	common input voltage decoupling
IN1+	4	input 1
GND	5	ground
SVR	6	half supply voltage decoupling (ripple rejection)
MODE	7	mode selection input (standby, mute and operating)
OUT1+	8	non inverted loudspeaker terminal 1
V_{CC}	9	supply voltage
TAB	-	back side tab or heats spreader has to be connected to ground

8. Functional description

8.1 Input configuration

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)} \quad (1)$$

SE application: R_i = 60 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(60 \times 10^3 \times 220 \times 10^{-9})} = 12 \text{ Hz} \quad (2)$$

BTL application: R_i = 30 kΩ and C_i = 470 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(30 \times 10^3 \times 470 \times 10^{-9})} = 11 \text{ Hz} \quad (3)$$

As shown in Equation 2 and Equation 3, large capacitor values for the inputs are not necessary, so the switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behavior.

8.2 Power amplifier

The power amplifier is a Single-Ended (SE) and/or Bridge-Tied Load (BTL) amplifier with an all-NPN output stage, capable of delivering a peak output current of 3 A.

Using the TFA9842J as a BTL amplifier offers the following advantages:

- Lower peak value of the supply current

- Ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking capacitor
- Good low frequency performance.

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10 %; see Figure 6.

The maximum output power is limited by the supply voltage of 26 V and the maximum available output current is 3 A (repetitive peak current). A minimum load for SE of 4 Ω and for BTL of 16 Ω is required for V_{CC} > 22 V; see Figure 5.

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom, compared to the average power output, for transferring the loudest parts without distortion. At V_{CC} = 18 V and P_o = 5 W (SE with R_L = 4 Ω) or P_o = 10 W (BTL with R_L = 8 Ω) at THD = 0.2 % (see Figure 7), the Average Listening Level (ALL) music power without any distortion yields:

$$P_{o(ALL,\,SE)} = \frac{5 \cdot 10^3}{15.85} = 315\ \text{mW} \quad (4)$$

$$P_{o(ALL,\,BTL)} = \frac{10 \cdot 10^3}{15.85} = 630\ \text{mW} \quad (5)$$

The power dissipation can be derived from Figure 9 (SE and BTL) for a headroom of 0 dB and 12 dB, respectively (see Table 4).

Table 4: Power rating as function of headroom

Headroom	Power output		Power dissipation (both channels driven)
	SE	BTL	
0 dB	P_o = 5 W	P_o = 10 W	P_D = 8.4 W
12 dB	$P_{o(ALL)}$ = 315 mW	$P_{o(ALL)}$ = 630 mW	P_D = 4.2 W

For the average listening level a power dissipation of 4.2 W can be used for a heatsink calculation.

8.3 Mode selection

The TFA9842J has three functional modes, which can be selected by applying the proper DC voltage to pin MODE (see Table 5 and Figure 3).

Table 5: Mode selection

V_{MODE}	Amplifiers 1 and 2
0 to 0.8 V	standby
4.5 V to (V_{CC} – 3.5 V)	mute
(V_{CC} – 2.0 V) to V_{CC}	on

Standby — The current consumption is very low and the outputs are floating. The device is in standby mode when V_{MODE} < 0.8 V, or when pin MODE is grounded.

Mute — The amplifier is DC-biased but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when 4.5 V < V_{MODE} < (V_{CC} − 3.5 V).

On — The amplifier is operating normally. The operating mode is activated at V_{MODE} > (V_{CC} − 2.0 V).

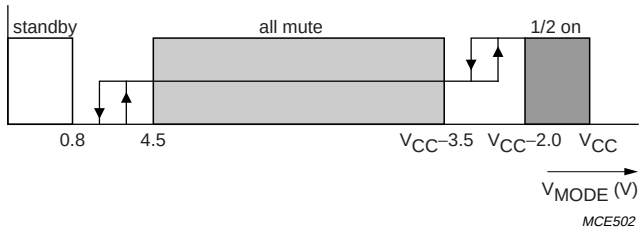


Fig 3. Mode selection.

8.4 Supply voltage ripple rejection

The supply voltage ripple rejection (SVRR) is measured with an electrolytic capacitor of 150 µF on pin SVR using a bandwidth of 20 Hz to 22 kHz. Figure 11 illustrates the SVRR as function of the frequency. A larger capacitor value on pin SVR improves the ripple rejection behavior at the lower frequencies.

8.5 Built-in protection circuits

The TFA9842J contains two types of temperature sensors; one measures local temperatures of the power stages and one measures the global chip temperature. At a local temperature of the power stage of approximately 185 °C or a global temperature of approximately 150 °C this detection circuit switches off the power stages for 2 ms. High impedance of the outputs is the result. After this time period the power stages switch on automatically and the detection will take place again; still a too high temperature switches off the power stages immediately. This protects the TFA9842J against shorts to ground, to the supply voltage, across the load and too high chip temperatures.

The protection will only be activated when necessary, so even during a short-circuit condition, a certain amount of (pulsed) current will still be flowing through the short, just as much as the power stage can handle without exceeding the critical temperature level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	operating	–0.3	+26	V
		no signal	–0.3	+28	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	3	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
P_{tot}	total power dissipation		-	35	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection		-	24	V

10. Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	both channels driven	2.0	K/W

11. Static characteristics

Table 8: Static characteristics

V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = V_{CC}; V_i = 0 V; measured in test circuit Figure 13; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating	[1]	9	17	26	V
I_q	quiescent supply current	R_L = ∞	[2]	-	60	100	mA
I_{stb}	standby supply current	V_{MODE} = 0		-	-	10	µA
V_O	DC output voltage		[3]	-	9	-	V
ΔV_{OUT}	differential output voltage offset	BTL mode	[4]	-	-	200	mV
V_{MODE}	mode selection input voltage	on mode		V_{CC} – 2.0	-	V_{CC}	V
		mute mode		4.5	-	V_{CC} – 3.5	V
		standby mode		0	-	0.8	V
I_{MODE}	input current on pin MODE	0 < V_{MODE} < V_{CC} – 3.5		-	-	20	µA

[1] A minimum load for BTL of 16 Ω is required at V_{CC} > 22 V.

[2] With a load connected at the outputs the quiescent supply current will increase.

[3] The DC output voltage with respect to ground is approximately 0.5V_{CC}.

[4] $\Delta V_{OUT} = |V_{OUT1+} - V_{OUT2-}|$

12. Dynamic characteristics

Table 9: Dynamic characteristics SE

V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 4 Ω; f = 1 kHz; V_{MODE} = V_{CC}; measured in test circuit Figure 12; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10 %; R_L = 4 Ω		7	7.5	-	W
		THD = 0.5 % R_L = 4 Ω		-	6.1	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.1	0.5	%
G_v	SE voltage gain			25	26	27	dB
Z_i	input impedance			40	60	-	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	150	-	μV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	60	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	60	-	dB
$V_{o(mute)}$	output voltage in mute mode		[3]	-	-	150	μV
α_{cs}	channel separation	R_{source} = 0 Ω		50	60	-	dB
$\lvert G_v \rvert$	channel unbalance			-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode (V_{MODE} = 7 V) is measured with an input voltage of 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, including noise.

Table 10: Dynamic characteristics BTL

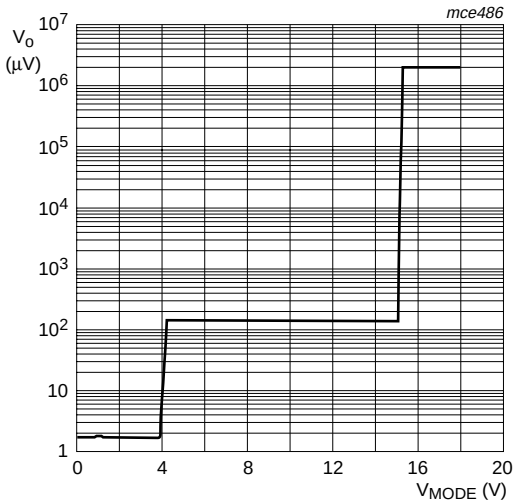
V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = V_{CC}; measured in test circuit Figure 13; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10 %; R_L = 8 Ω		14	15	-	W
		THD = 0.5 %; R_L = 8 Ω		-	14		W
THD	total harmonic distortion	P_o = 1 W		-	0.05	0.5	%
G_v	BTL voltage gain			31	32	33	dB
Z_i	input impedance			20	30	-	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	200	-	μV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	65	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	65	-	dB
$V_{o(mute)}$	output voltage in mute mode		[3]	-	-	250	μV
α_{cs}	channel separation	R_{source} = 0 Ω		50	65	-	dB
$\lvert G_v \rvert$	channel unbalance			-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

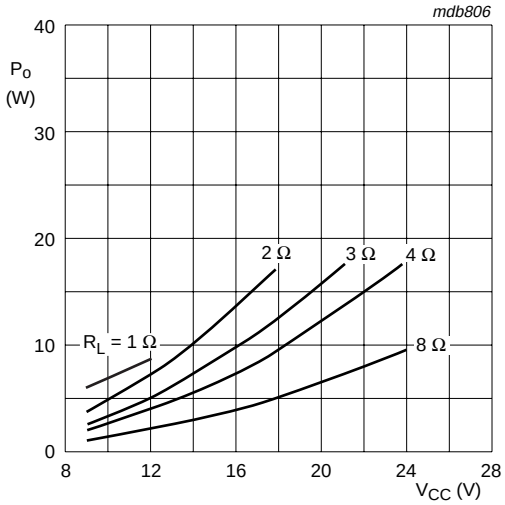
[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode (V_{MODE} = 7 V) is measured with an input voltage of 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, including noise.



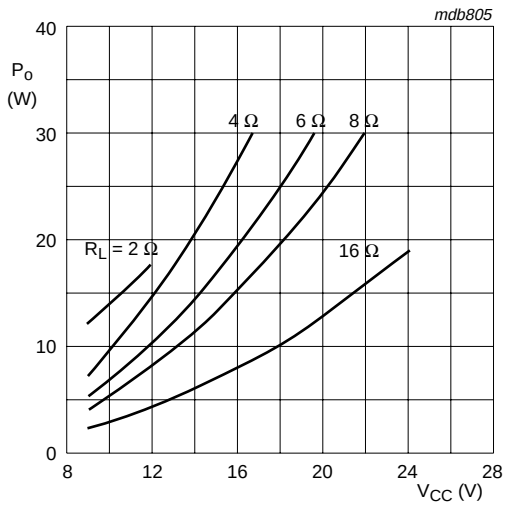
BTL; V_i = 50 mV; V_{CC} = 18 V.

Fig 4. AC output voltage as function of mode selection voltage.



THD = 10 %.

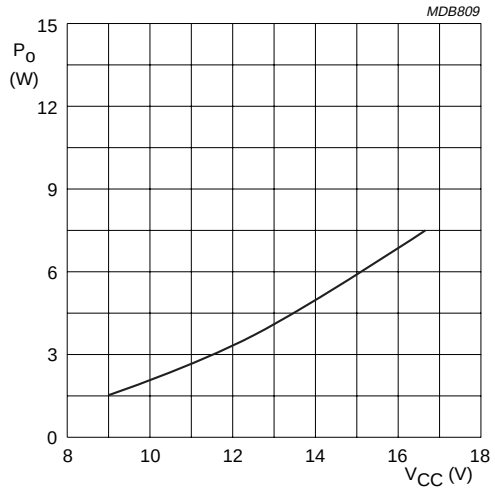
a. SE.



THD = 10 %.

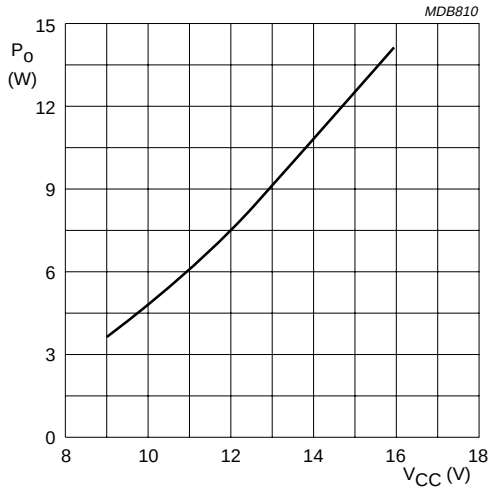
b. BTL.

Fig 5. Output power (one channel) as function of supply voltage for various loads.



THD = 10 %; R_L = 4 Ω; f = 1 kHz.

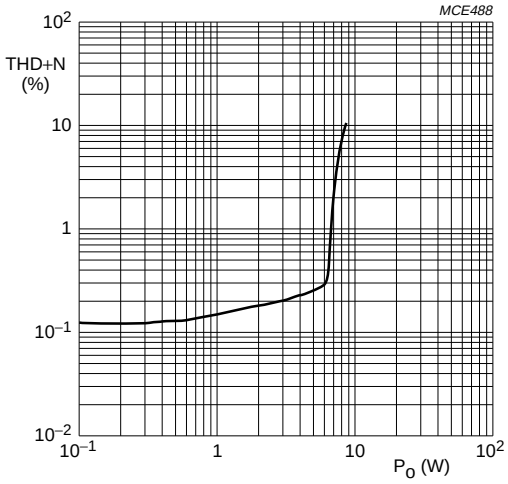
a. SE.



THD = 10 %; R_L = 8 Ω; f = 1 kHz.

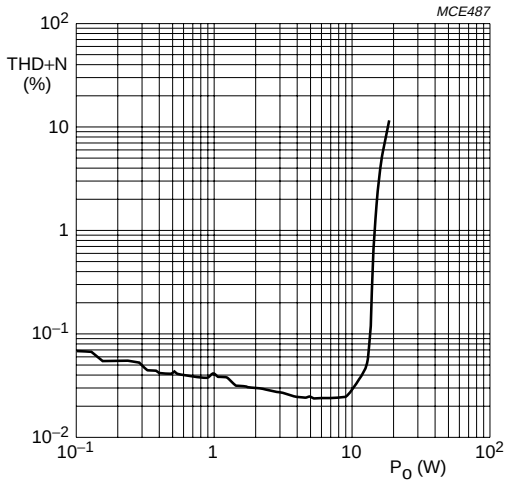
b. BTL.

Fig 6. Output power as function of supply voltage.



V_{CC} = 18 V; f = 1 kHz; R_L = 4 Ω.

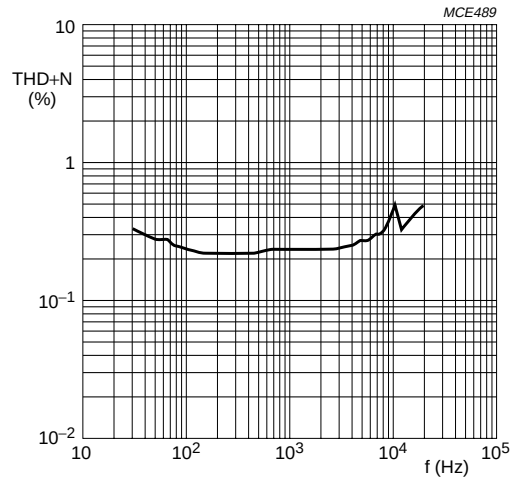
a. SE.



V_{CC} = 18 V; f = 1 kHz; R_L = 8 Ω.

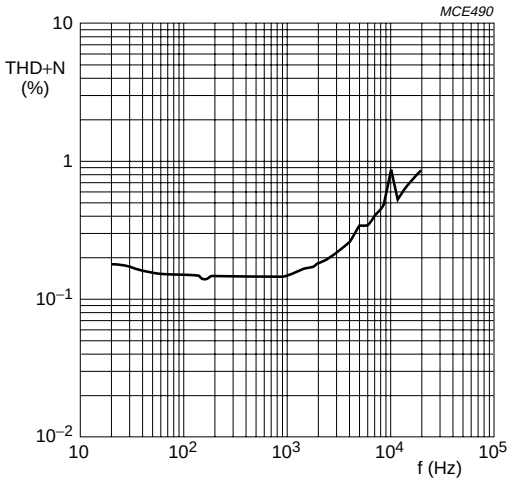
b. BTL.

Fig 7. Total harmonic distortion-plus-noise as function of output power.



V_{CC} = 17 V; P_o = 1 W; R_L = 4 Ω.

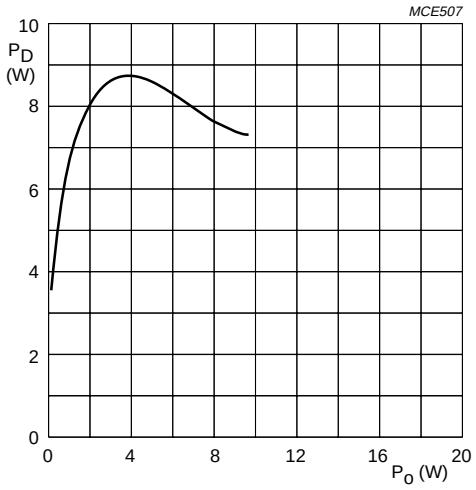
a. SE.



V_{CC} = 17 V; P_o = 1 W; R_L = 8 Ω.

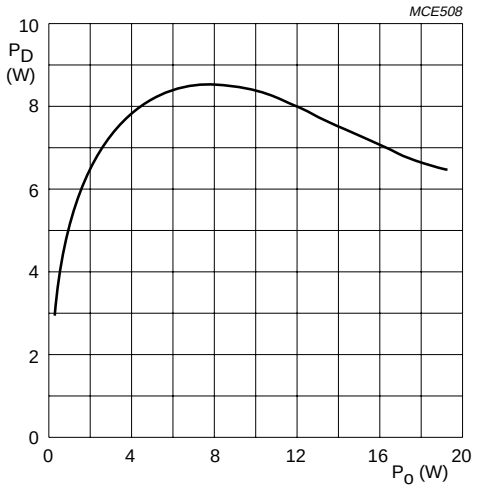
b. BTL.

Fig 8. Total harmonic distortion-plus-noise as function of frequency.



V_{CC} = 18 V; R_L = 4 Ω.

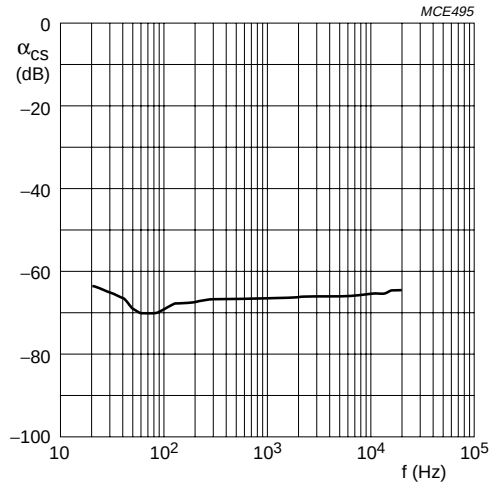
a. SE.



V_{CC} = 18 V; R_L = 8 Ω.

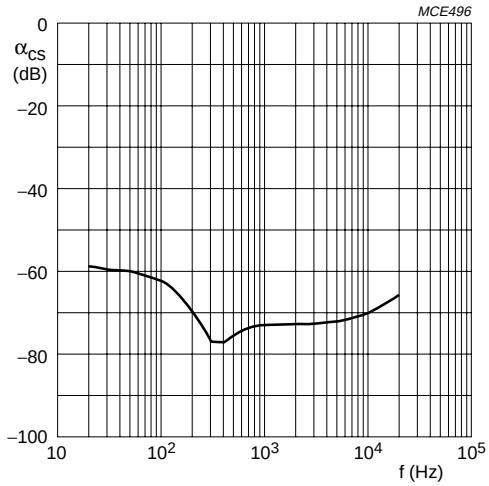
b. BTL.

Fig 9. Total power dissipation as function of channel output power per channel (worst case, both channels driven).



V_{CC} = 17 V; R_L = 4 Ω.

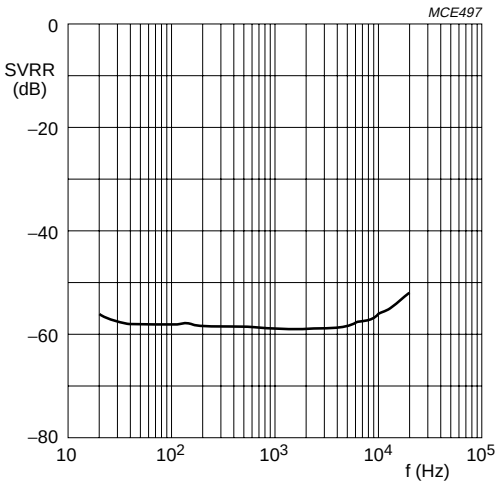
a. SE.



V_{CC} = 17 V; R_L = 8 Ω.

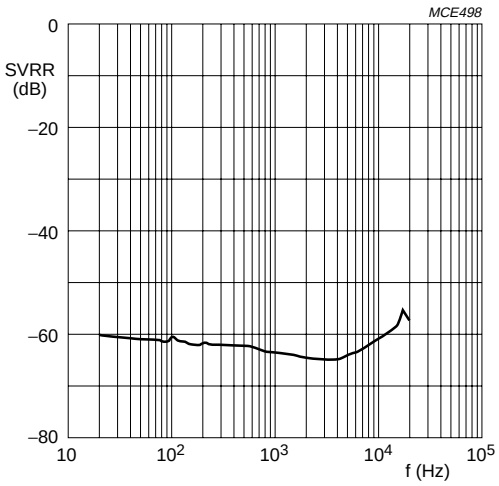
b. BTL.

Fig 10. Channel separation as function of frequency (no bandpass filter applied).



V_{CC} = 17 V; R_{source} = 0 Ω; V_{ripple} = 300 mV (RMS);
a bandpass filter of 20 Hz to 22 kHz has been applied;
inputs short-circuited.

a. SE.



V_{CC} = 17 V; R_{source} = 0 Ω; V_{ripple} = 300 mV (RMS);
a bandpass filter of 20 Hz to 22 kHz has been applied;
inputs short-circuited.

b. BTL.

Fig 11. Supply voltage ripple rejection as function of frequency.

13. Application information

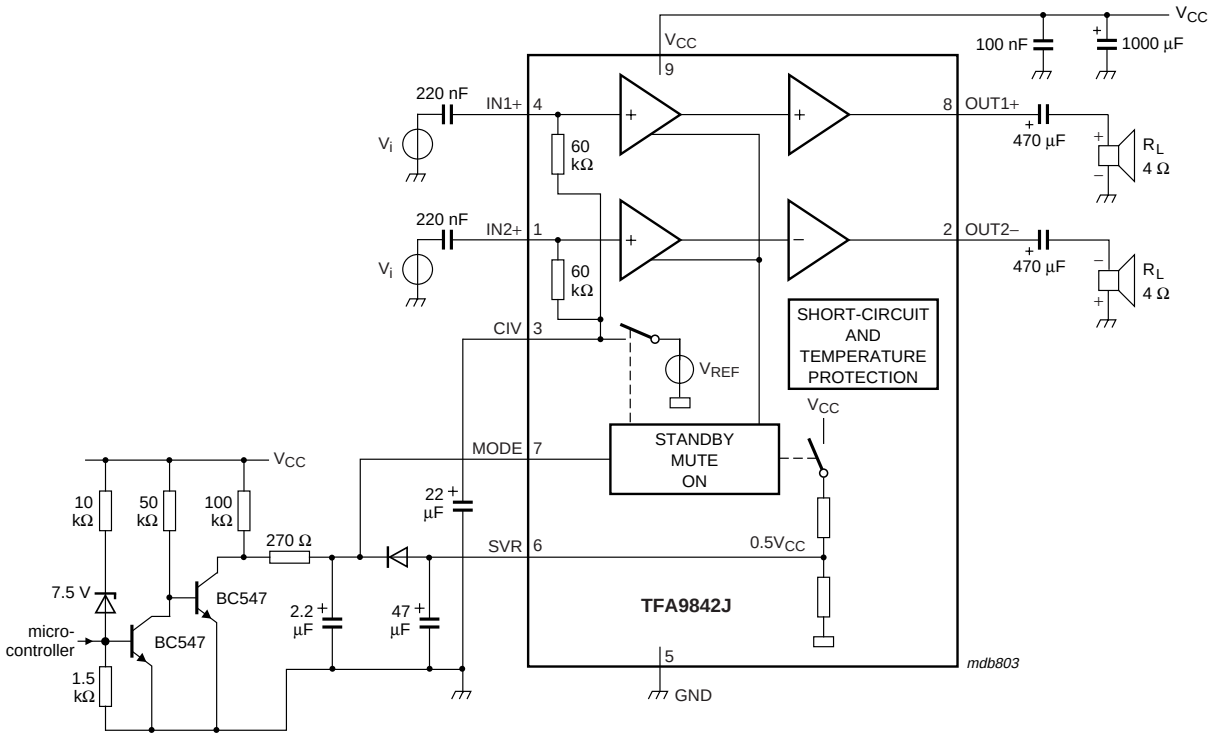


Fig 12. Typical SE application diagram.

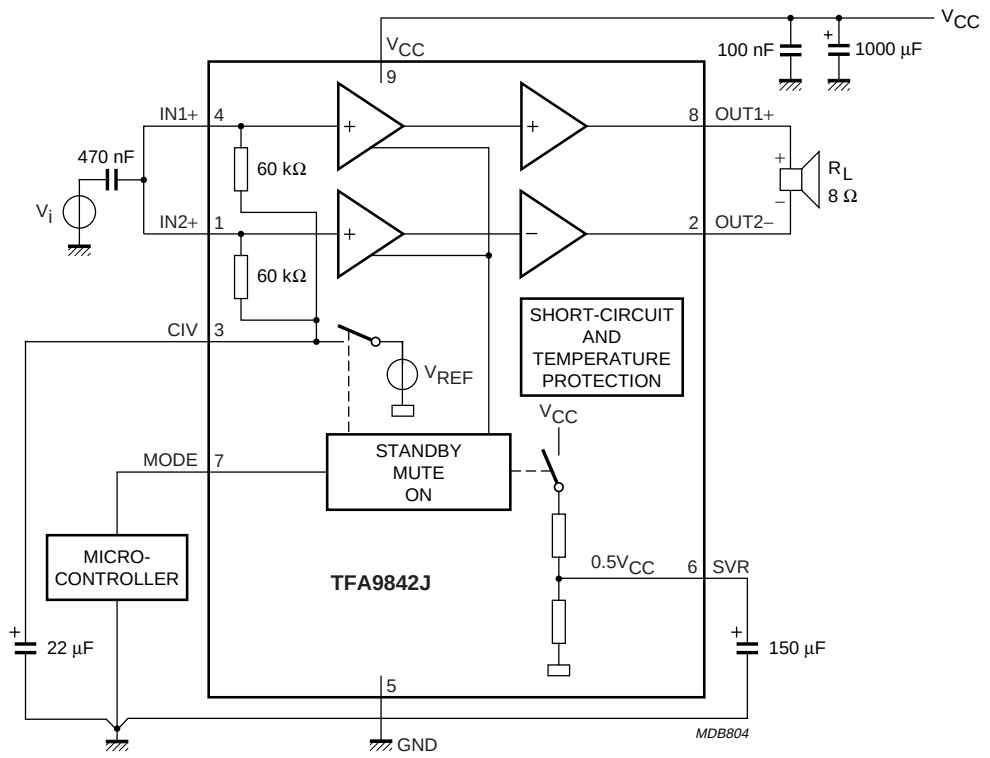


Fig 13. BTL application diagram.

Remark: Because of switching inductive loads, the output voltage can rise beyond the maximum supply voltage of 28 V. At high supply voltages, it is recommended to use (Schottky) diodes to the supply voltage and ground.

13.1 Printed-circuit board

13.1.1 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

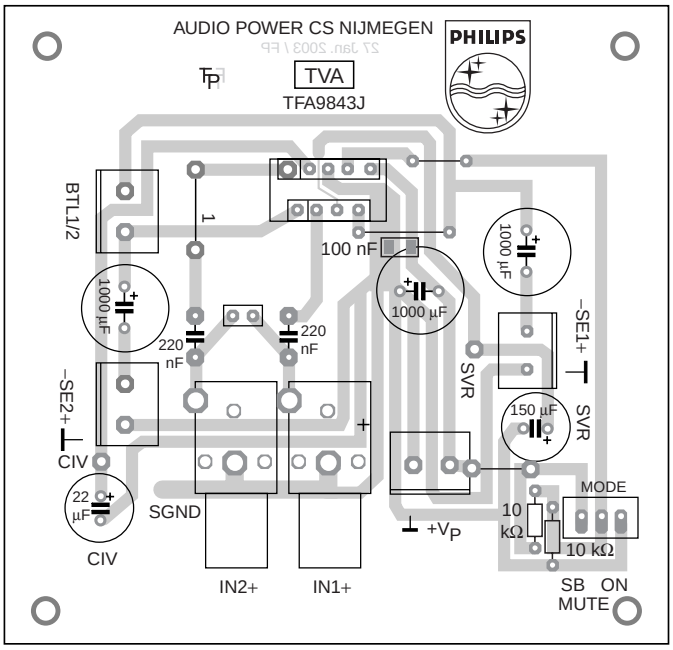


Fig 14. Printed-circuit board layout (single-sided); components view.

13.1.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR, typical 100 nF, has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor, e.g. 1000 µF or greater, must be placed close to the device.

The bypass capacitor on pin SVR reduces the noise and ripple on the mid rail voltage. For good THD and noise performance a low ESR capacitor is recommended.

13.2 Thermal behavior and heatsink calculation

The measured maximum thermal resistance of the IC package, $R_{th(j-mb)}$, is 2.0 K/W. A calculation for the heatsink can be made, with the following parameters:

$T_{amb(max)}$ = 60 °C (example)

V_{CC} = 18 V and R_L = 4 Ω (SE)

$T_{j(max)}$ = 150 °C (specification)

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient including the heatsink. This can be calculated using the maximum temperature increase divided by the power dissipation:

$$R_{th(tot)} = (T_{j(max)} - T_{amb(max)})/P_D$$

At V_{CC} = 18 V and R_L = 4 Ω (2 × SE) the measured worst-case sine-wave dissipation is 8.4 W; see Figure 9.

For $T_{j(max)}$ = 150 °C the temperature raise, caused by the power dissipation, is: 150 − 60 = 90 °C:

$P \times R_{th(tot)} = 90$ °C

$R_{th(tot)} = 90/8.4 = 10.7$ K/W

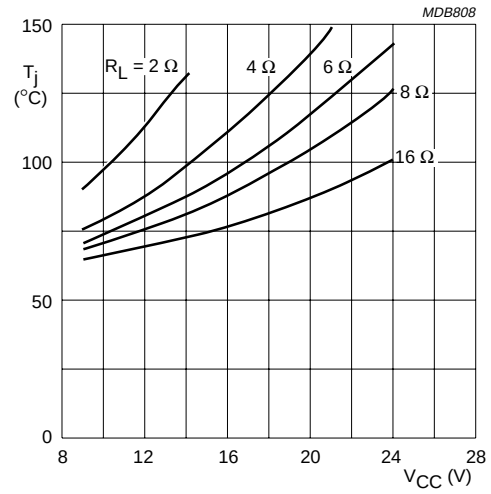
$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 10.7 - 2.0 = 8.7$ K/W.

This calculation is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation (see Section 8.2.2). This allows for the use of a smaller heatsink:

$P \times R_{th(tot)} = 90$ °C

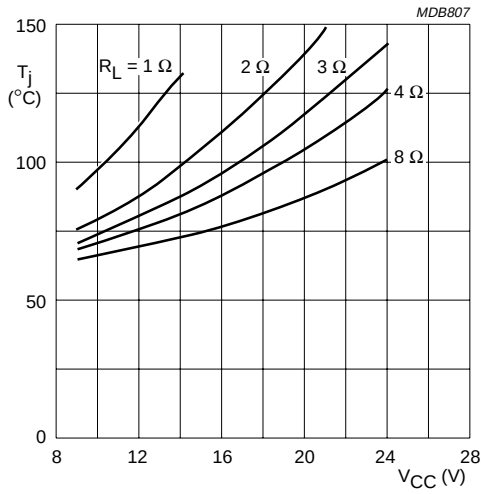
$R_{th(tot)} = 90/4.2 = 21.4$ K/W

$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 21.4 - 2.0 = 19.4$ K/W.



External heatsink of 8 K/W; with music signals; T_{amb} = 25 °C.

a. SE.



External heatsink of 8 K/W; with music signals; T_{amb} = 25 °C.

b. BTL.

Fig 15. Junction temperature as function of supply voltage for various loads.

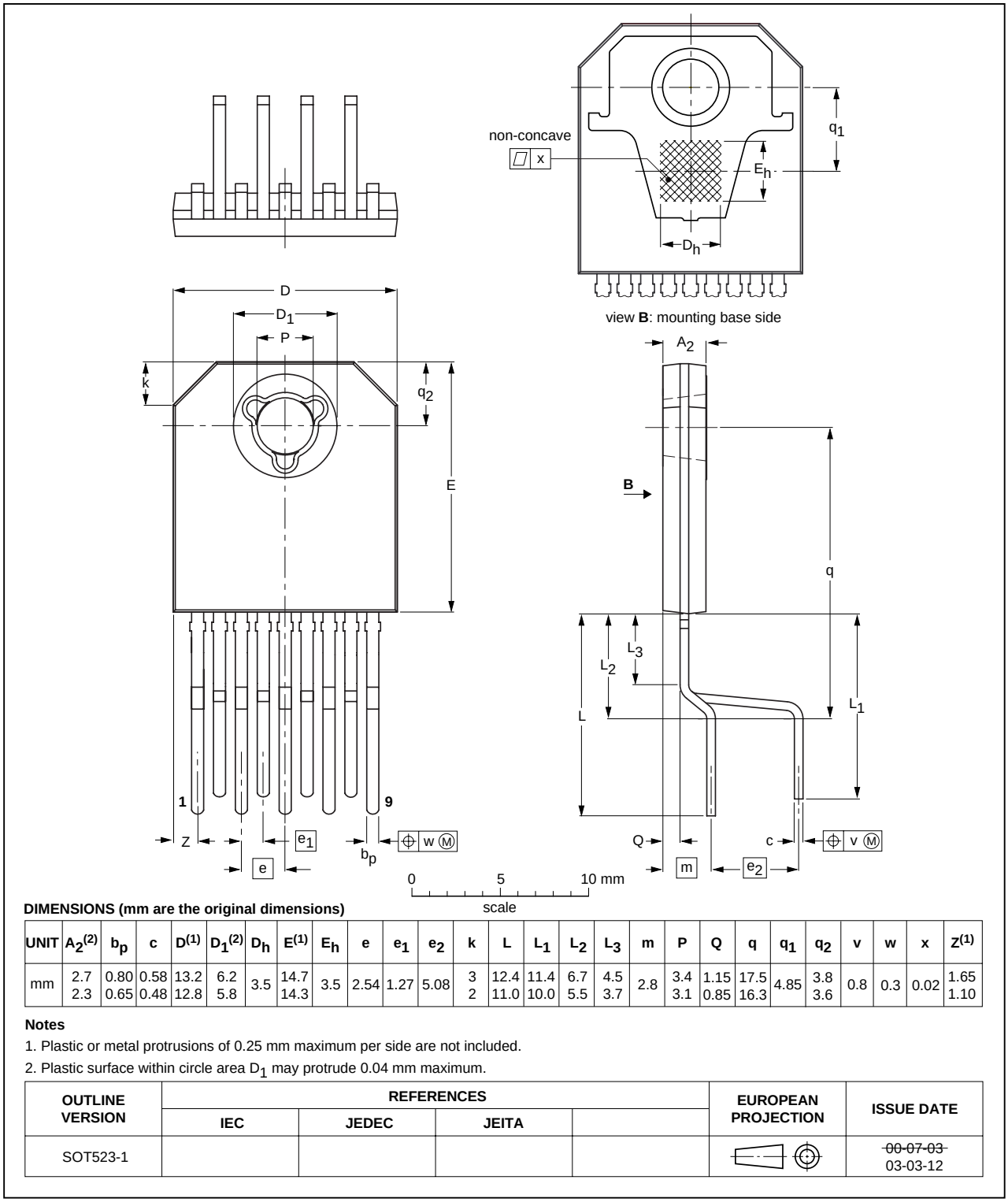
14. Test information

14.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

15. Package outline

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad **SOT523-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2[2]	b_p	c	D[1]	D_1[2]	D_h	E[1]	E_h	e	e_1	e_2	k	L	L_1	L_2	L_3	m	P	Q	q	q_1	q_2	v	w	x	Z[1]
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3 2	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	1.65 1.10

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic surface within circle area D_1 may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT523-1						~~00-07-03~~ 03-03-12

Fig 16. DBS9P package outline.

16. Soldering

16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

16.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.4 Package related soldering information

Table 11: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	–	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

17. Revision history

Table 12: Revision history

Rev	Date	CPCN	Description
01	20040426	-	Preliminary data (9397 750 12013)

18. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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