TDF8599C

I²C-bus controlled stereo class-D amplifier 136 W/8 Ω with full diagnostics

Rev. 1 — 5 August 2011 Product short data sheet

1. General description

The TDF8599C is a dual Bridge-Tied Load (BTL) car audio amplifier comprising an NDMOST-NDMOST output stage based on SOI BCDMOS technology. Low power dissipation enables the TDF8599C high-efficiency, class-D amplifier to be used with a smaller heat sink than those normally used with standard class-AB amplifiers.

The TDF8599C can operate in either non-I²C-bus mode or I²C-bus mode. When in I²C-bus mode, DC load detection results and fault conditions can be easily read back from the device. Up to 15 I²C-bus addresses can be selected depending on the value of the external resistors connected to pins ADS and MOD.

When pin ADS is short circuited to ground, the TDF8599C operates in non-I²C-bus mode. Switching between Operating mode and Mute mode in non-I²C-bus mode is only possible using pins EN and SEL_MUTE.

2. Features and benefits

- High-efficiency
- Low quiescent current
- Operating voltage from 8 V to 48 V
- Two 8 Ω/6 Ω capable BTL channels or one 4 Ω/3 Ω capable BTL channel
- Differential inputs
- Fast-mode I²C-bus
- I²C-bus mode with 15 I²C-bus addresses or non-I²C-bus mode operation
- Clip detect
- Independent short-circuit protection for each channel
- Advanced short circuit protection for load, GND and supply
- Load dump protection
- Thermal foldback and thermal protection
- DC offset protection
- Selectable AD or BD modulation
- Advanced clocking:
  - Switchable oscillator clock source: internal for Master mode or external for Slave mode
  - PLL mode to synchronize with external oscillator
  - Spread spectrum mode
  - Phase staggering
  - Frequency hopping

- No ‘pop noise’ caused by DC output offset voltage
- I²C-bus mode:
  - Load diagnostics
    Speaker load, open load and shorted load
    Amplifier output to ground and to supply shorts
    Tweeter detection
  - Thermal pre-warning diagnostic level setting
  - Identification of activated protections or warnings
  - Selectable diagnostic information available using pins DIAG and CLIP
  - Selectable gain 32 dB/26 dB (32 dB in non-I²C-bus mode)
- Qualified in accordance with AEC-Q100

3. Applications

- Car audio
- Audio entertainment systems

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; V_P = 40 V						
V_P	supply voltage		8	40	48	V
I_P	supply current	off state; V_{EN} < 0.8 V	-	3	10	μA
I_q	quiescent current	no load, snubbers and output filter connected	-	90	120	mA
Output power in stereo mode; V_P = 48 V						
P_o	output power	R_L = 8 Ω; THD = 10 %	-	136	-	W
		R_L = 6 Ω; THD = 10 %	-	155	-	W
Output power in parallel mode; V_P = 48 V						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	270	-	W
		R_L = 3 Ω; THD = 10 %	-	300	-	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDF8599CTH	HSOP36	plastic, heatsink small outline package; 36 leads; low stand-off height	SOT851-2

6. Block diagram

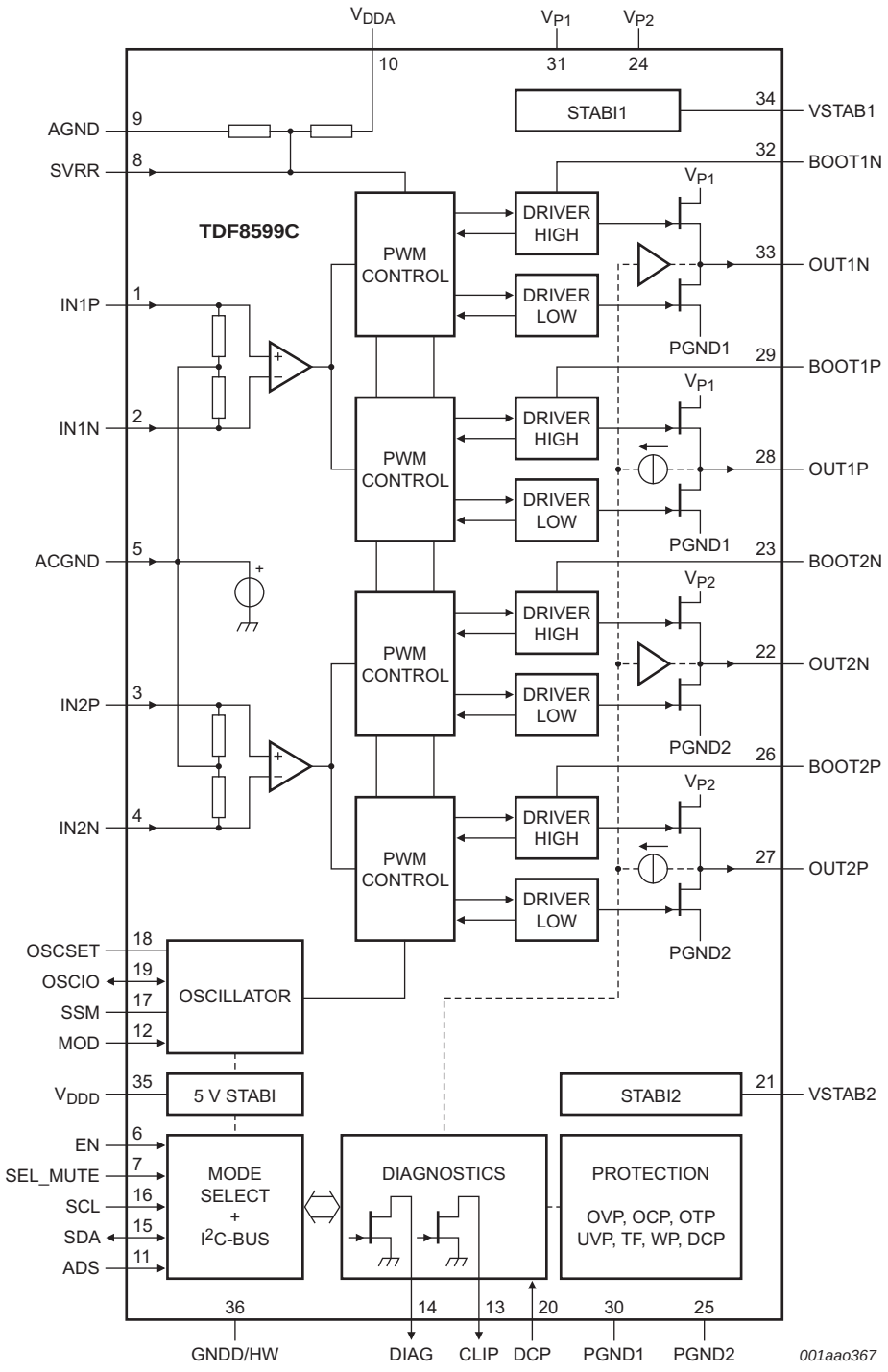


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

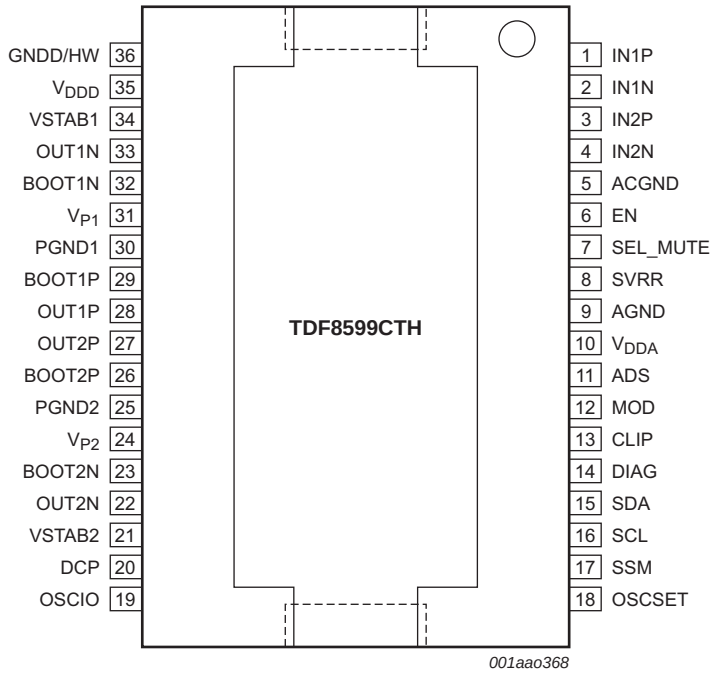


Fig 2. Heatsink up (top view) pin configuration TDF8599CTH

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
IN1P	1	I	channel 1 positive audio input
IN1N	2	I	channel 1 negative audio input
IN2P	3	I	channel 2 positive audio input
IN2N	4	I	channel 2 negative audio input
ACGND	5	I	decoupling for input reference voltage
EN	6	I	enable input: non-I²C-bus mode: switch between off and Mute mode I²C-bus mode: off and Standby mode
SEL_MUTE	7	I	select mute or unmute
SVRR	8	I	decoupling for internal half supply reference voltage
AGND	9	G	analog supply ground
V_{DDA}	10	P	analog supply voltage
ADS	11	I	non-I²C-bus mode: connected to ground I²C-bus mode: address selection pin
MOD	12	I	modulation mode, phase shift and parallel mode select

Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
CLIP	13	O	clip output; open-drain
DIAG	14	O	diagnostic output; open-drain
SDA	15	I/O	I²C-bus data input and output
SCL	16	I	I²C-bus clock input
SSM	17		master setting: Spread spectrum mode frequency slave setting: phase lock operation
OSCSET	18		master/slave oscillator setting master only setting: set internal oscillator frequency
OSCIO	19	I/O	master setting: internal oscillator output slave setting: external oscillator input
DCP	20	I	DC protection input for the filtered output voltages
VSTAB2	21		decoupling internal stabilizer 2 for DMOST drivers
OUT2N	22	O	channel 2 negative PWM output
BOOT2N	23		bootstrap capacitor for channel 2 negative
V_{P2}[2]	24	P	channel 2 power supply voltage
PGND2	25	G	channel 2 power ground
BOOT2P	26		bootstrap capacitor for channel 2 positive
OUT2P	27	O	channel 2 positive PWM output
OUT1P	28	O	channel 1 positive PWM output
BOOT1P	29		bootstrap capacitor for channel 1 positive
PGND1	30	G	channel 1 power ground
V_{P1}[2]	31	P	channel 1 power supply voltage
BOOT1N	32		bootstrap capacitor for channel 1 negative
OUT1N	33	O	channel 1 negative PWM output
VSTAB1	34		decoupling internal stabilizer 1 for DMOST drivers
V_{DDD}	35		decoupling of the internal 5 V logic supply
GNDD/HW	36	G	ground digital supply voltage handle wafer connection

[1] I = input, O = output, I/O = input/output, G = ground and P = power supply.

[2] In this data sheet supply voltage V_P describes V_{P1}, V_{P2} and V_{DDA}.

8. Functional description

8.1 Master and slave mode selection

In a master and slave configuration, multiple TDF8599C devices are daisy-chained together in one audio application with a single device providing the clock frequency signal for all other devices. In this situation, it is recommended that the oscillators of all devices are synchronized for optimum EMI behavior as follows:

All OSCIO pins are connected together and one TDF8599C in the application is configured as the clock-master. All other TDF8599C devices are configured as clock-slaves.

- The clock-master pin OSCIO is configured as the oscillator output. When a resistor (R_{osc}) is connected between pins OSCSET and AGND, the TDF8599C is in Master mode.
- The clock-slave pins OSCIO are configured as the oscillator inputs. When pin OSCSET is directly connected to pin AGND, the TDF8599C is in Slave mode. See Table 4 for all oscillator modes.

Table 4. Oscillator modes

OSCSET pin	OSCIO pin	SSM pin	Oscillator modes
R_{osc} > 22 kΩ	output	C_{SSM} to pin AGND	master, spread spectrum
		shorted to pin AGND	master, no spread spectrum
R_{osc} = 0 Ω	input	C_{PLL} + R_{PLL} to pin AGND	slave, PLL enabled
		shorted to pin AGND	slave, PLL disabled

8.2 Operation mode selection

Pin MOD is used to select specific operating modes. The resistor (R_{MOD}) connected between pins MOD and AGND together with the non-I²C-bus/I²C-bus mode determine the operating mode (see Table 5). This in turn is determined by the resistor value connected between pins ADS and AGND.

In non-I²C-bus mode, pin MOD is used to select:

- AD or BD modulation (see Section 8.2.1).
- ½ π phase shift when oscillator is used in Slave mode (see Section 8.2.2).
- Parallel mode operation (see Section 8.2.3).

In I²C-bus mode, pin MOD can only select Parallel mode and the I²C-bus address range. In addition, the modulation mode and phase shift are programmed using I²C-bus commands.

Table 5. Operation mode selection with the MOD pin

R_{MOD} (kΩ)	Non-I²C-bus mode[2]	I²C-bus mode[1]
0 (short to AGND)	AD modulation: Stereo mode; no phase shift in Slave mode	Stereo mode
4.7	BD modulation: Stereo mode; no phase shift in Slave mode	
13	AD modulation: Stereo mode; ½ π phase shift in Slave mode	
33	BD modulation: Stereo mode; ½ π phase shift in Slave mode	Parallel mode
100	AD modulation: Parallel mode; no phase shift in Slave mode	
∞ (open)	BD modulation: Parallel mode; no phase shift in Slave mode	

[1] $R_{ADS} \geq 4.7$ kΩ; See Table 8 on page 15.

[2] $R_{ADS} = 0$ Ω; pin ADS is short circuited to pin AGND.

8.2.1 Modulation mode

In non-I²C-bus mode, pin MOD is used to select either AD or BD modulation mode (see Table 5). In I²C-bus mode, the modulation mode is selected using I²C-bus command IB3[D0].

- AD modulation mode: the bridge halves switch in opposite phase.
- BD modulation mode: the bridge halves switch in phase.

Figure 4 and Figure 5 show simplified representations of AD and BD modulation.

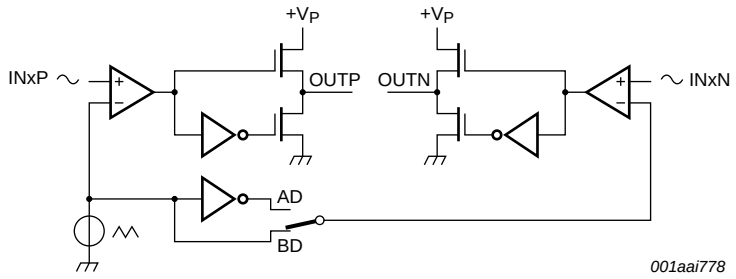
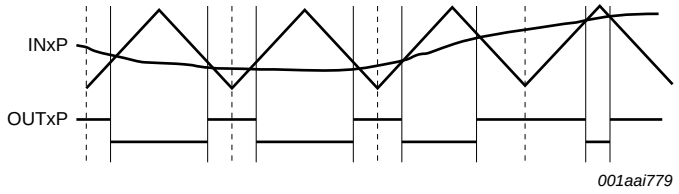
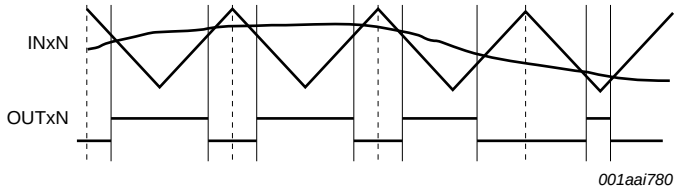


Fig 3. AD/BD modulation switching circuit

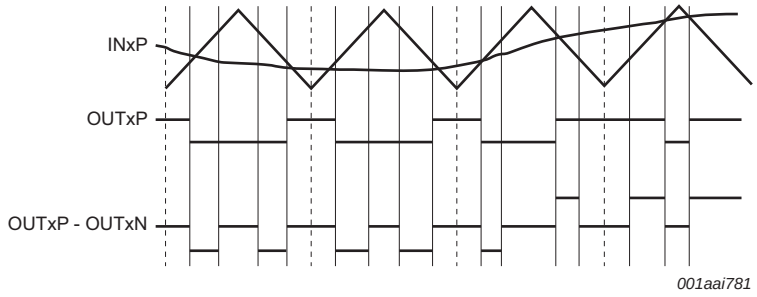


a. Bridge half 1.

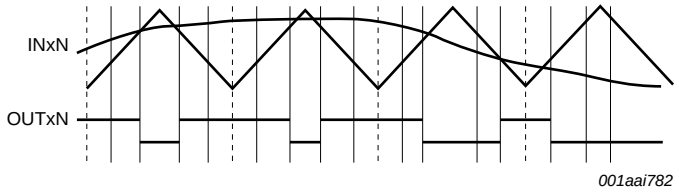


b. Bridge half 2 switched in the opposite phase to bridge half 1.

Fig 4. AD modulation



a. Phase switching cycle.



b. Inverted signal to the modulator.

Fig 5. BD modulation

8.2.2 Phase staggering (Slave mode)

In Slave mode with phase lock operation enabled, a phase shift with respect to the incoming clock signal can be selected to distribute the switching moments over time in multi-amplifier applications. In non-I²C-bus mode, $\frac{1}{2}\ \pi$ phase shift can be programmed using pin MOD. In I²C-bus mode, six different phase shifts (0, $\frac{1}{4}\ \pi$, $\frac{1}{3}\ \pi$, $\frac{1}{2}\ \pi$, $\frac{2}{3}\ \pi$, $\frac{3}{4}\ \pi$) can be selected using the I²C-bus bits (IB3[D1:D3]). See Table 5 for selection of the phase shift in non-I²C-bus mode with pin MOD.

8.2.3 Parallel mode

In Parallel mode, selected with pin MOD, the two output stages operate in parallel to enlarge the drive capability. The inputs and outputs for Parallel mode must be connected on the Printed-Circuit Board (PCB) as shown in Figure 6. The parallel connection can be made after the output filter, as shown in Figure 6 or directly to the device output pins (OUTxP and OUTxN).

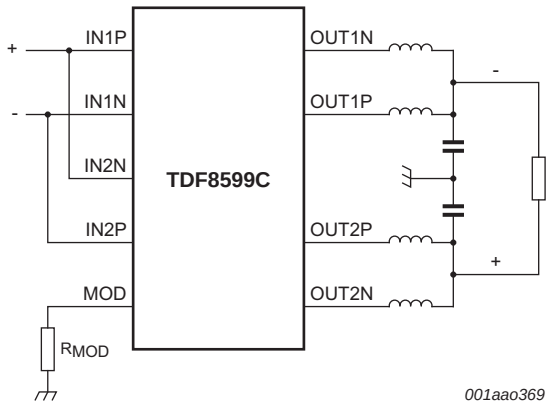


Fig 6. Parallel mode

In Parallel mode, the channel 1 I²C-bus bits can be programmed using the I²C-bus.

8.3 Protection

The TDF8599C includes a range of built-in protection functions. All protections are asynchronous and do not need an (external) clock signal at pin OSCIO to be operational. How the TDF8599C manages the various possible fault conditions for each protection is described in the following sections:

Table 6. Overview of protection types

Protection type	Reference
Thermal foldback	Section 8.3.1
Overtemperature	Section 8.3.2
Overcurrent	Section 8.3.3
Window	Section 8.3.4
DC Offset	Section 8.3.5
Undervoltage	Section 8.3.6
Overvoltage	Section 8.3.6

8.3.1 Thermal foldback

The TDF8599C has a built-in Thermal Foldback Protection (TFP) which is tripped when the average junction temperature exceeds the threshold level. TFP decreases amplifier gain such that the combination of power dissipation and $R_{th(j-a)}$ create a junction temperature around the threshold level. The device will not completely switch off but remains operational at the lower output power levels. If the average junction temperature continues to increase, a second built-in temperature protection threshold level shuts down the amplifier completely.

8.3.2 Overtemperature protection

If the average junction temperature (T_j) > 160 °C, OverTemperature Protection (OTP) is tripped and the power stages shut down immediately.

8.3.3 Overcurrent protection

OverCurrent Protection (OCP) is tripped when the output current exceeds the threshold. OCP regulates the output voltage such that the maximum output current is limited. The amplifier outputs keep switching and the amplifier is NOT shutdown completely. This is called current limiting.

OCP also detects when the loudspeaker terminals are short circuited or one of the amplifier's demodulated outputs is short circuited to one of the supply lines. In either case, the shorted channel(s) are switched off.

The amplifier can distinguish between loudspeaker impedance drops and a low-ohmic short across the load or one of the supply lines. This impedance threshold depends on the supply voltage used. When a short is made across the load causing the impedance to drop below the threshold level, the shorted channel(s) are switched off. They try to restart every 50 ms. If the short circuit condition is still present after 50 ms, the cycle repeats. The average power dissipation will be low because of this reduced duty cycle.

When a channel is switched off due to a short circuit on one of the supply lines, Window Protection (WP) is activated. WP ensures the amplifier does not start-up after 50 ms until the supply line short circuit is removed.

8.3.4 Window protection

Window Protection (WP) checks the PWM output voltage before switching from Standby mode to Mute mode (with both outputs switching) and is activated as follows:

- During the start-up sequence:
  - When the TDF8599C is switched from standby to mute ($t_{d(stb\text{-}mute)}$). When a short circuit on one of the output terminals (i.e. between V_P or GND) is detected, the start-up procedure is interrupted and the TDF8599C waits for open circuit outputs. No large currents flow in the event of a short circuit to the supply lines because the check is performed before the power stages are enabled.
- During operation:
  - A short to one of the supply lines trips OCP causing the amplifier channel to shutdown. After 50 ms the amplifier channel restarts and WP is activated. However, the corresponding amplifier channel will not start-up until the supply line short circuit has been removed.

WP will provide short-circuit diagnostic information in I²C-bus mode data bits DBx[D1,D0].

8.3.5 DC offset protection

DC Protection (DCP) is activated (using IB1[D6] or IB2[D6]) when the DC content in the demodulated output voltage exceeds a set threshold. DCP is active in both Mute mode and Operating mode. False triggering of the DCP by low frequencies in the audio signal is prevented by use of an external capacitor (C_F) between pin DCP and pin AGND to generate a cut-off frequency. Connecting pin DCP to pin AGND disables DCP in both I²C-bus and non-I²C-bus modes.

8.3.6 Supply voltage protection

UnderVoltage Protection (UVP) is activated when the supply voltage drops below the UVP threshold. UVP triggers the UVP circuit causing the system to first mute and then stop switching. The SVRR and SEL_MUTE pin capacitors will discharge. The information on the MOD and ADS pins is latched while UVP is active. When the supply voltage rises above the threshold level, the system restarts.

OverVoltage Protection (OVP) is activated when the supply voltage exceeds the OVP threshold. The OVP (or load dump) circuit is activated and the power stages are shutdown. The SVRR and SEL_MUTE pin capacitors will discharge. When the supply voltage drops below the OVP threshold level the system restarts.

8.4 Diagnostic output

8.4.1 Diagnostic table

The diagnostic information for I²C-bus mode and non-I²C-bus mode is shown in Table 7. The instruction bitmap and data bytes are described in Table 9 and Table 11.

Pins DIAG and CLIP have an open-drain output which must have an external pull-up resistor connected to an external voltage. Pins CLIP and DIAG can show both fixed and I²C-bus selectable information.

Pin DIAG goes LOW when a short-circuit to one of the amplifier outputs occurs. The microprocessor reads the failure information using the I²C-bus. The I²C-bus bits are set for a short-circuit. These bits can be reset with the I²C-bus read command.

Even after the short has been removed, the microprocessor knows what was wrong after reading the I²C-bus. Old information is read when a single I²C-bus read command is used. To read the current information, two read commands must be sent, one after another.

When selected, pin DIAG gives the current diagnostic information. Pin DIAG is released instantly when the failure is removed, independent of the I²C-bus latches.

Table 7. Available data on pins DIAG and CLIP

Diagnostic	I²C-bus mode		Non-I²C-bus mode	
	Pin DIAG	Pin CLIP	Pin DIAG	Pin CLIP
Power-on reset	yes	yes	yes	yes
UVP or OVP	yes	no	yes	no
Clip detection	no	selectable	no	yes
Temperature pre-warning	no	selectable	no	yes
OCP/WP	yes	no	yes	no
DCP	selectable	no	yes	no
OTP	yes	no	yes	no
AC load detection; see Section 8.4.2.2	no	selectable	no	no

8.4.2 Load identification (I²C-bus mode only)

8.4.2.1 DC load detection

DC load detection is only available in I²C-bus mode and is controlled using bit IB2[D2]. The default setting is logic 0 for bit IB2[D2] which disables DC load detection. DC load detection is enabled when bit IB2[D2] = 1. Load detection takes place before the SVRR capacitor is charged and before the class-D amplifier output stage starts switching. The start-up time from Standby mode to Mute mode is increased by $t_{det(DCload)}$ (see Figure 7).

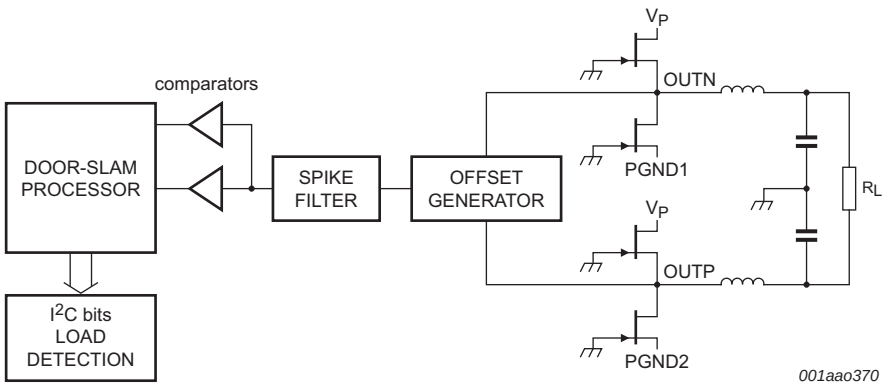


Fig 7. DC load detection circuit

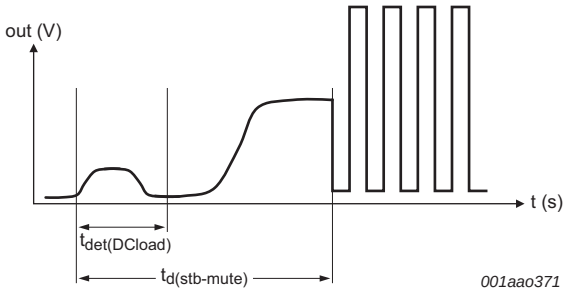


Fig 8. DC load detection procedure

An inaudible current test pulse is created between the amplifier outputs. The external capacitor connected to pin SEL_MUTE is used for timing. Load diagnostics based on the voltage difference between pins OUTxP and OUTxN are shown in Figure 9.

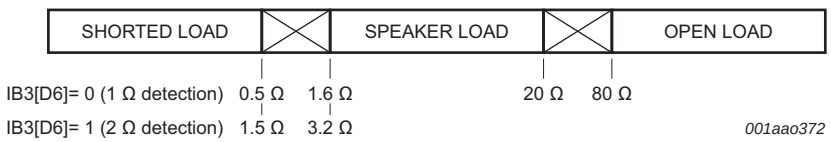


Fig 9. DC load detection limits

DC Load detection has built in spike filtering and a door-slam processor to remove disturbances caused by switching relays in the wiring harness, EMC or the closing of a car door. Reliable load detection is performed in one diagnostic cycle with these filter techniques.

8.4.2.2 AC load detection (tweeter detection)

AC load detection is only available in I²C-bus mode and is controlled using bit IB3[D4]. The default setting for bit IB3[D4] = 0 disables AC load detection. When AC load detection is enabled (bit IB3[D4] = 1), the amplifier load current is measured and compared with a reference level. Pin CLIP is activated when this threshold is reached. Using this information, AC load detection can be performed using a predetermined input signal frequency and level. The frequency and signal level should be chosen so that the load current exceeds the programmed current threshold when the AC coupled load (tweeter) is present.

8.4.3 CLIP detection

CLIP detection gives information for clip levels exceeding a threshold defined as the THD level of a sinusoidal output signal of ≥ 0.2 %. In non-I²C-bus mode pin CLIP is used as the output for the clip detection circuitry on both channel 1 and channel 2. Setting either bit IB1[D5] or bit IB2[D5] to logic 0 in I²C-bus mode defines which channel reports clip information on the CLIP pin.

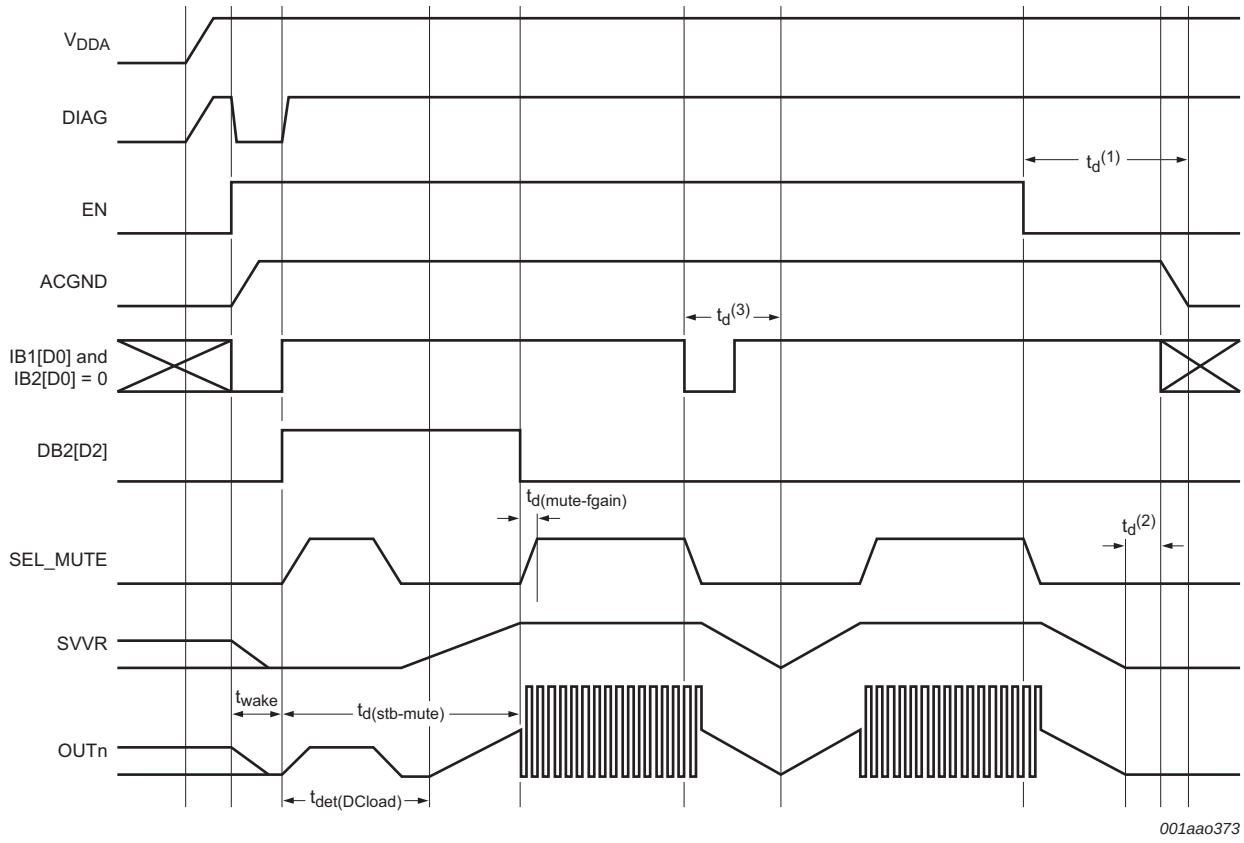
8.4.4 Start-up and shutdown sequence

To prevent switch on or switch off ‘pop noises’, a capacitor (C_{SVRR}) connected to pin SVRR is used to smooth start-up and shutdown. During start-up and shutdown, the output voltage tracks the voltage on pin SVRR. Increasing C_{SVRR} results in a longer start-up and shutdown time. Enhanced pop noise performance is achieved by muting the amplifier until the SVRR voltage reaches its final value and the outputs start switching. The capacitor value on pin SEL_MUTE (C_{ON}) determines the unmute and mute timing. The voltage on pin SEL_MUTE determines the amplifier gain. Increasing C_{ON} increases the unmute and mute times. In addition, a larger C_{ON} value increases the DC load detection cycle time.

When the amplifier is switched off with an I²C-bus command or by pulling pin EN LOW, the amplifier is first muted and then capacitor (C_{SVRR}) is discharged.

In Slave mode, the device enters the off state immediately after capacitor (C_{SVRR}) is discharged. In Master mode, the clock is kept active by an additional delay ($t_d^{(2)}$) of approximately 50 ms to allow slave devices to enter the off state.

A clock signal is needed during the start-up and shutdown sequence. When an external clock is connected to pin OSCIO (in Slave mode), the clock must remain active during the shutdown sequence for delay ($t_d^{(1)}$) to ensure that the slaved TDF8599C devices are able to enter the off state. A watchdog is added to protect against clock failure.

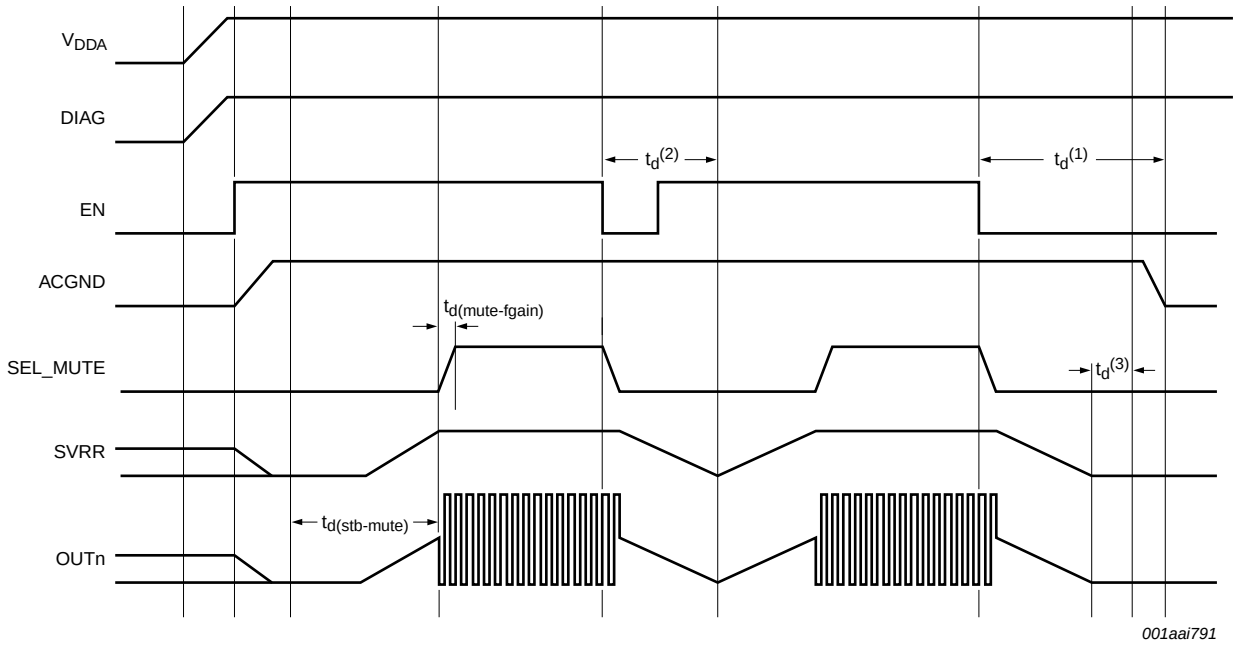


(1) Shutdown hold delay.

(2) Master mode shutdown delay.

(3) Shutdown delay.

Fig 10. Start-up and shutdown timing in I²C-bus mode with DC load detection



(1) Shutdown hold delay.

(2) Shutdown delay.

(3) Master mode shutdown delay.

Fig 11. Start-up and shutdown timing in non-I²C-bus mode

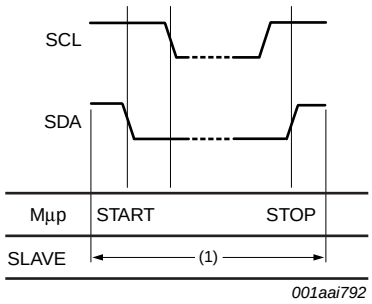
9. I²C-bus specification

TDF8599C address with hardware address select.

Table 8. I²C-bus write address selection using pins MOD and ADS

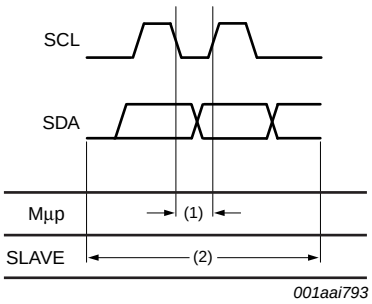
R_{ADS} (kΩ)	R_{MOD} (kΩ)						R/W
	Stereo mode			Parallel mode			
	0[1]	4.7	13	33	100	open	
Open	58h	68h	78h	58h	68h	78h	1 = Read from TDF8599C
100	56h	66h	76h	56h	66h	76h	0 = Write to TDF8599C
33	54h	64h	74h	54h	64h	74h	
13	52h	62h	72h	52h	62h	72h	
4.7	50h	60h	70h	50h	60h	70h	
0[1]	non-I²C-bus mode select						

[1] Short circuited to ground.



(1) When SCL is HIGH, SDA changes to form the start or stop condition.

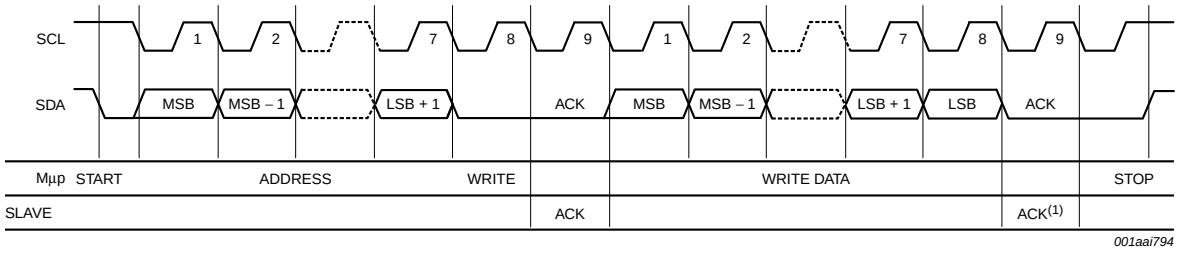
Fig 12. I²C-bus start and stop conditions



(1) SDA is allowed to change.

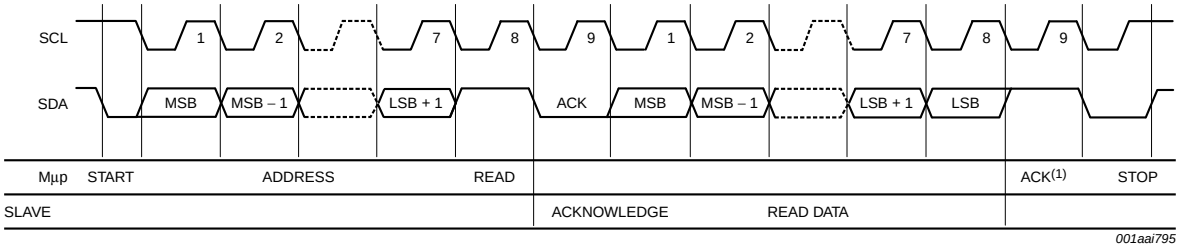
(2) All data bits must be valid on the positive edges of SCL.

Fig 13. Data bits sent from Master microprocessor (Mμp)



(1) To stop the transfer after the last acknowledge a stop condition must be generated.

Fig 14. I²C-bus write



(1) To stop the transfer, the last byte must not be acknowledged (SDA is HIGH) and a stop condition must be generated.

Fig 15. I²C-bus read

9.1 Instruction bytes

If R/W bit = 0, the TDF8599C expects three instruction bytes: IB1, IB2 and IB3. After a power-on reset, all instruction bits are set to zero.
The channel 1 bits are used in parallel mode.

Table 9. Instruction byte descriptions

Bit	Value	Description		
		Instruction byte IB1	Instruction byte IB2	Instruction byte IB3
D7	0	offset detection on pin DIAG	offset protection on	latch information on pins ADS and MOD when the amplifier starts switching
	1	no offset detection on pin DIAG	offset protection off	latch information on pins ADS and MOD
D6	0	channel 1 offset monitoring on	channel 2 offset monitoring on	1 Ω detection level for shorted load detection
	1	channel 1 offset monitoring off	channel 2 offset monitoring off	2 Ω detection level for shorted load detection
D5	0	channel 1 clip detect on pin CLIP	channel 2 clip detect on pin CLIP	select 32 dB gain
	1	channel 1 no clip detect on pin CLIP	channel 2 no clip detect on pin CLIP	select 26 dB gain
D4	0	disable frequency hopping	thermal pre-warning on pin CLIP	disable AC load detection
	1	enable frequency hopping[1]	no thermal pre-warning on pin CLIP	enable AC load detection
D3	0	oscillator frequency as set with R_{osc} − 10 %	temperature pre-warning at 140 °C	oscillator phase shift bits IB3[D3] to IB3[D1][2]
	1	oscillator frequency as set with R_{osc} + 10 %	temperature pre-warning at 120 °C	
D2	0	reserved	DC-load detection disabled	
	1	reserved	DC-load detection enabled	
D1	0	channel 1 enabled	channel 2 enabled	
	1	channel 1 disabled	channel 2 disabled	
D0	0	TDF8599C in Standby mode	all channels operating	AD modulation
	1	TDF8599C in Mute or Operating modes[3]	all channels muted	BD modulation

[1] See IB1[D3].

[2] See Table 10 “Phase shift bit settings” for information on IB3[D3] to IB3[D1].

[3] See IB2[D0].

Table 10. Phase shift bit settings

D3	D2	D1	Phase
0	0	0	0
0	0	1	$\frac{1}{4}\pi$
0	1	0	$\frac{1}{3}\pi$
0	1	1	$\frac{1}{2}\pi$
1	0	0	$\frac{2}{3}\pi$
1	0	1	$\frac{3}{4}\pi$

9.2 Data bytes

If R/W = 1, the TDF8599C sends two data bytes to the microprocessor (DB1 and DB2). All short diagnostic and offset protection bits and bits OTP, UVP and OVP are latched. In addition, all bits are reset after a read operation except the DC load detection bits (DBx[D3,D4], DB1[D6]). The default setting for all bits is logic 0.

In Parallel mode, the diagnostic information is stored in byte DB1.

Table 11. Description of data bytes

Bit	Value	DB1 channel 1	DB2 channel 2
D7	0	at least 1 instruction bit set to logic 1	below maximum temperature
	1	all instruction bits are set to logic 0	maximum temperature protection occurred
D6	0	load diagnostics by OCP/WP	no temperature warning
	1	load diagnostics by DC load detection	temperature pre-warning active
D5	0	no overvoltage	no undervoltage
	1	overvoltage protection occurred	undervoltage protection occurred
D4	0	speaker load channel 1	speaker load channel 2
	1	open load channel 1	open load channel 2
D3	0	no shorted load channel 1	no shorted load channel 2
	1	shorted load channel 1	shorted load channel 2
D2	0	no offset	startup diagnostic finished
	1	offset detected	startup diagnostic in progress
D1	0	no short to V_P channel 1	no short to V_P channel 2
	1	short to V_P channel 1	short to V_P channel 2
D0	0	no short to ground channel 1	no short to ground channel 2
	1	short to ground channel 1	short to ground channel 2

Data byte DB1[D7] indicates whether the instruction bits have been set to logic 0. In principle, DB1[D7] is set after a POR or when all the instruction bits are programmed to logic 0. Pin DIAG is driven LOW when bit DB1[D7] = 1.

10. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	pins V_{DDA}, V_{P1} and V_{P2}		-	53	V
		load dump; duration 50 ms; t_r > 2.5 ms		-	50	V
I_{ORM}	repetitive peak output current	maximum output current limiting	[1]	6.5	-	A
I_{OM}	peak output current	maximum; non-repetitive				
		stereo mode		-	18	A
		parallel mode		-	12	A
V_i	input voltage	pins SCL, SDA, ADS, MOD, SSM, OSCIO, EN and SEL_MUTE		0	5.5	V
		pins IN1N, IN1P, IN2N and IN2P		0	10	V
V_o	output voltage	pins DIAG and CLIP		0	10	V
R_{ESR}	equivalent series resistance	as seen between pins V_P and PGNDn		-	350	mΩ
T_j	junction temperature			−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM	[2]			
		C = 100 pF; R_s = 1.5 kΩ		-	2000	V
		CDM	[3]			
		non-corner pins (except pin 10, V_{DDA})		-	500	V
		pin 10, V_{DDA}		-	250	V
		corner pins		-	750	V
$V_{(prot)}$	protection voltage	AC and DC short circuit voltage of output pins across load and to supply and ground	[4]	0	V_P	V

[1] Current limiting concept.

[2] Human Body Model (HBM).

[3] Charged-Device Model (CDM).

[4] The output pins are defined as the output pins of the filter connected between the TDF8599C output pins and the load.

11. Thermal characteristics

Table 13. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	35	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W

12. Static characteristics

Table 14. Static characteristics

V_P = 40 V; f_{osc} = 315 kHz; gain = 26 dB; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage	Operating mode		8	40	48	V
I_P	supply current	off state; $T_j \leq 85$ °C		-	3	10	μA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers and no filter connected		-	90	120	mA
I²C-bus interface: pins SCL and SDA							
V_{IL}	LOW-level input voltage			0	-	1.5	V
V_{IH}	HIGH-level input voltage			2.3	-	5.5	V
V_{OL}	LOW-level output voltage	pin SDA; I_{load} = 5 mA		0	-	0.4	V
Enable and SEL_MUTE input: pins EN and SEL_MUTE							
V_i	input voltage	pin EN; off state		0	-	0.8	V
		pin EN; Standby mode; I²C-bus mode		2	-	5	V
		pin EN; Mute mode or Operating mode; non-I²C-bus mode		2	-	5	V
		pin SEL_MUTE; Mute mode; voltage on pin EN > 2 V		0	-	0.8	V
		pin SEL_MUTE; Operating mode; voltage on pin EN > 2 V		3	-	5	V
I_i	input current	pin EN; 2.5 V		-	-	5	μA
		pin SEL_MUTE; Operating mode; 0.8 V		-	-	50	μA
Diagnostic output							
THD_{clip}	total harmonic distortion clip detection level			-	0.2	-	%
$V_{th(offset)}$	threshold voltage for offset detection		[1]	1	2	3	V
V_{OL}	LOW-level output voltage	DIAG or CLIP pins activated; I_o = 1 mA		-	-	0.3	V
I_L	leakage current	DIAG and CLIP pins; diagnostic not activated		-	-	50	μA
Audio inputs; pins IN1N, IN1P, IN2N and IN2P							
V_i	input voltage			-	2.45	-	V
SVRR voltage and ACGND input bias voltage in Mute and Operating modes							
V_{ref}	reference voltage	input ACGND pin		-	2.45	-	V
		half supply reference SVRR pin		-	20	-	V
Amplifier outputs; pins OUT1N, OUT1P, OUT2N and OUT2P							
$V_{O(offset)}$	output offset voltage	BTL; Mute mode		-	-	25	mV
		BTL; Operating mode	[2]	-	-	70	mV
		BTL; Operating mode; gain = 32 dB	[2]	-	-	140	mV

Table 14. Static characteristics *...continued*

V_P = 40 V; f_{osc} = 315 kHz; gain = 26 dB; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Stabilizer output; pins VSTAB1 and VSTAB2							
V_o	output voltage	stabilizer output in Mute mode and Operating mode		-	10	-	V
Voltage protections							
$V_{(prot)}$	protection voltage	undervoltage; amplifier is muted		6.8	7.2	8	V
		overvoltage; load dump protection is activated		50	52	54	V
		V_P that a POR occurs at		-	4.1	-	V
Current protection							
$I_{O(ocp)}$	overcurrent protection output current	current limiting concept		6.5	8	-	A
Temperature protection							
T_{prot}	protection temperature			-	152	-	°C
$T_{act(th\_fold)}$	thermal foldback activation temperature	gain = −1 dB		-	145	-	°C
$T_{j(AV)(warn1)}$	average junction temperature for pre-warning 1	IB2[D3] = 0; non-I²C-bus mode		-	140	-	°C
$T_{j(AV)(warn2)}$	average junction temperature for pre-warning 2	IB2[D3] = 1		-	120	-	°C
DC load detection levels: I²C-bus mode only							
$Z_{th(load)}$	load detection threshold impedance	for normal speaker load; IB3[D6] = 0; 1 Ω shorted load detection level		1.6	-	20	Ω
		for normal speaker load; IB3[D6] = 1; 2 Ω shorted load detection level		3.2	-	20	Ω
$Z_{th(open)}$	open load detection threshold impedance			80	-	-	Ω
$Z_{th(short)}$	shorted load detection threshold impedance	for shorted speaker load; IB3[D6] = 0; 1 Ω shorted load detection level		-	-	0.5	Ω
		for shorted speaker load; IB3[D6] = 1; 2 Ω shorted load detection level		-	-	1.5	Ω
AC load detection levels: I²C-bus mode only							
$I_{th(o)det(load)AC}$	AC load detection output threshold current			-	500	-	mA
Start-up/shut-down/mute timing							
t_{wake}	wake-up time	on pin EN before first I²C-bus transmission is recognized	[3]	-	-	500	µs
$t_{det(DCload)}$	DC load detection time	C_{ON} = 470 nF	[3]	-	320	-	ms
$t_{d(stb-mute)}$	delay time from standby to mute	measured from amplifier enabling to start of unmute (no DC load detection); C_{SVRR} = 22 µF		-	115	-	ms
$t_{d(mute-fgain)}$	mute to full gain delay time	C_{ON} = 470 nF	[4]	-	50	-	ms

Table 14. Static characteristics *...continued*

V_P = 40 V; f_{osc} = 315 kHz; gain = 26 dB; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_d	delay time	shutdown delay time from EN pin LOW to SVRR LOW; voltage on pin SVRR < 1 V; C_{SVRR} = 22 µF; V_P = 40 V	130	190	250	ms
		shutdown hold delay time from pin EN LOW to ACGND LOW; voltage on pin ACGND < 1 V; Master mode	-	100	-	ms
		hold delay in Master mode to allow slaved devices to shutdown f_{osc} = 315 kHz	-	50	-	ms

[1] Maximum leakage current from DCP pin to ground = 3 µA.

[2] DC output offset voltage is applied to the output gradually during the transition between Mute mode and Operating mode.

[3] I²C-bus mode only.

[4] The transition time between Mute mode and Operating mode is determined by the time constant on the SEL_MUTE pin.

12.1 Switching characteristics

Table 15. Switching characteristics

V_P = 40 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	oscillator frequency	external clock frequency; R_{osc} = 39 kΩ	-	315	-	kHz
		internal fixed frequency and Spread spectrum mode frequency based on the resistor value connected to pin OSCSET for the master setting	300	-	500	kHz
Master/slave setting (OSCIO pin)						
R_{osc}	oscillator resistance	resistor value on pin OSCSET; master setting	22	39	49	kΩ
V_{OL}	LOW-level output voltage	output	-	-	0.8	V
V_{OH}	HIGH-level output voltage	output	4	-	-	V
V_{IL}	LOW-level input voltage	input	-	-	0.8	V
V_{IH}	HIGH-level input voltage	input	3	-	-	V
f_{track}	tracking frequency	PLL enabled	300	-	500	kHz
C_{OSCIO}	capacitance on pin OSCIO	output	-	-	220	pF
Spread spectrum mode setting						
Δf_{osc}	oscillator frequency variation	between maximum and minimum values; Spread spectrum mode activated	-	10	-	%
f_{sw}	switching frequency	Spread spectrum mode activated; C_{SSM} = 1 µF	-	7	-	Hz

Table 15. Switching characteristics *...continued*

V_P = 40 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frequency hopping						
$f_{osc(int)}$	internal oscillator frequency	change positive; IB1[D4] = 1; IB1[D3] = 0	-	f_{osc} + 10 %	-	kHz
		change negative; IB1[D4] = 1; IB1[D3] = 1	-	f_{osc} − 10 %	-	kHz

13. Dynamic characteristics

Table 16. Dynamic characteristics

V_P = 40 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 315 kHz; $G_{v(cl)}$ = 26 dB; $R_{s(L)}$ < 0.04 Ω [1]; T_{amb} = 25 °C; Stereo mode; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	Stereo mode:	[2]				
		THD = 1 %; R_L = 8 Ω		76	78	-	W
		THD = 10 %; R_L = 8 Ω		95	100	-	W
		square wave (EIAJ); R_L = 8 Ω		-	150	-	W
		V_P = 48 V; THD = 1 %; R_L = 8 Ω		-	105	-	W
		V_P = 48 V; THD = 10 %; R_L = 8 Ω		-	136	-	W
		V_P = 48 V; THD = 10 %; R_L = 6 Ω		-	155	-	W
		Parallel mode:	[2]				
		THD = 1 %; R_L = 4 Ω		140	145	-	W
		THD = 10 %; R_L = 4 Ω		185	195	-	W
		square wave (EIAJ); R_L = 4 Ω		-	300	-	W
		V_P = 48 V; THD = 1 %; R_L = 4 Ω		-	205	-	W
		V_P = 48 V; THD = 10 %; R_L = 4 Ω		-	270	-	W
		V_P = 48 V; THD = 10 %; R_L = 3 Ω		-	300	-	W
THD	total harmonic distortion	f_i = 1 kHz; P_o = 1 W	[3]	-	0.02	0.1	%
$G_{v(cl)}$	closed-loop voltage gain	IB3[D5] = 1	[4]	25	26	27	dB
		IB3[D5] = 0	[4]	31	32	33	dB
α_{cs}	channel separation	f_i = 1 kHz; P_o = 1 W		60	70	-	dB
SVRR	supply voltage rejection ratio	BD mode, f_{ripple} = 1 kHz	[5]	-	70	-	dB
$\|Z_{i(dif)}\|$	differential input impedance			-	100	-	kΩ
$V_{n(o)}$	output noise voltage	Operating mode					
		BD mode	[6]	-	75	120	μV
		AD mode	[6]	-	230	300	μV
		Mute mode					
		BD mode	[7]	-	30	40	μV
		AD mode	[7]	-	215	280	μV
$\alpha_{bal(ch)}$	channel balance			-	0	1	dB

Table 16. Dynamic characteristics *...continued*

V_P = 40 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 315 kHz; $G_{v(cl)}$ = 26 dB; $R_{s(L)}$ < 0.04 Ω[1]; T_{amb} = 25 °C; Stereo mode; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{mute}	mute attenuation		[8]	66	-	-	dB
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V RMS		65	80	-	dB
η_{po}	output power efficiency	P_o = 80 W		-	90	-	%

[1] $R_{s(L)}$ is the sum of the inductor series resistance from the low-pass LC filter in the application together with all resistance from PCB traces or wiring between the output pin of the TDF8599C and the inductor to the measurement point. LC filter dimensioning is L = 22 μH, C = 0.68 μF for 8 Ω load and L = 10 μH, C = 1 μF for 4 Ω load.

[2] Output power is measured indirectly based on R_{DSon} measurement.

[3] Total harmonic distortion is measured at the bandwidth of 22 Hz to 20 kHz, AES brick wall. The maximum limit is guaranteed but may not be 100 % tested.

[4] 32 dB gain in non-I²C-bus mode.

[5] $V_{ripple} = V_{ripple(max)}$ = 1 V (p-p); R_s = 0 Ω.

[6] B = 22 Hz to 20 kHz, AES brick wall, R_s = 0 Ω.

[7] B = 22 Hz to 20 kHz, AES brick wall, independent of R_s.

[8] $V_i = V_{i(max)}$ = 0.5 V RMS.

14. Application information

14.1 Output power estimation (Stereo mode)

The output power, just before clipping, can be estimated using Equation 1:

$$P_{o(1)} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)}\right) \times \left(1 - t_{w(min)} \times \frac{f_{osc}}{2}\right) \times V_P\right)^2}{2 \times R_L} [W] \quad (1)$$

Where,

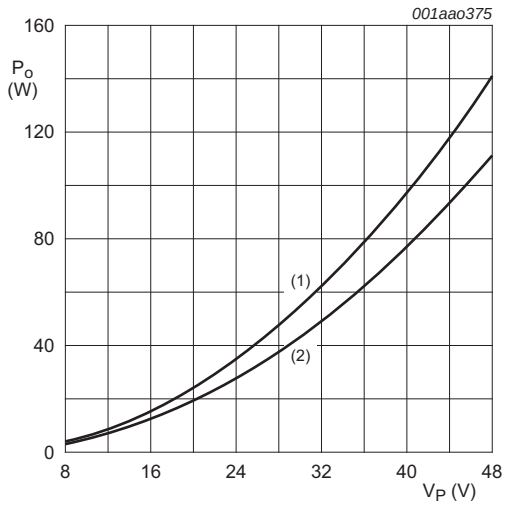
- V_P = supply voltage (V)
- R_L = load impedance (Ω)
- R_{DSon} = drain source on-state resistance (Ω)
- R_s = series resistance of the output inductor (Ω)
- $t_{w(min)}$ = minimum pulse width(s) depending on output current (s)
- f_{osc} = oscillator frequency in Hz (typically 315 kHz)

The output power at 10 % THD can be estimated using Equation 2:

$$P_{o(2)} = 1.25 \times P_{o(1)} \quad (2)$$

where $P_{o(1)}$ = 0.5 % and $P_{o(2)}$ = 10 %

Figure 16 and Figure 17 show the estimated output power at THD = 0.5 % and THD = 10 % as a function of supply voltage for different load impedances in stereo mode.



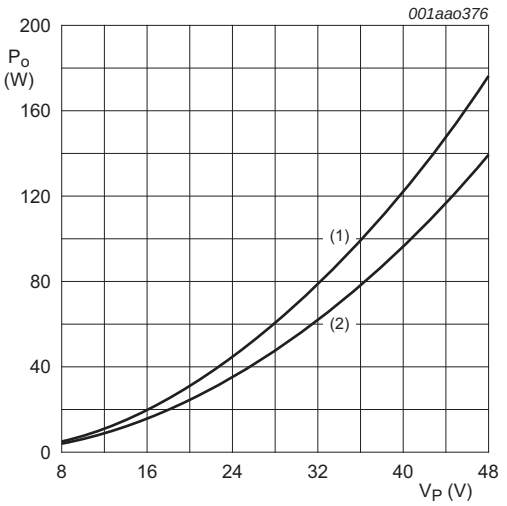
THD = 0.5 %.

R_{DSon} = 0.31 Ω (at T_j = 100 °C), R_s = 0.05 Ω, $t_{w(min)}$ = 250 ns and $I_{O(ocp)}$ = 8 A (typical).

(1) R_L = 6 Ω.

(2) R_L = 8 Ω.

Fig 16. P_o as a function of V_P in stereo mode with THD = 0.5 %



THD = 10 %.

R_{DSon} = 0.31 Ω (at T_j = 100 °C), R_s = 0.05 Ω, $t_{w(min)}$ = 250 ns and $I_{O(ocp)}$ = 8 A (typical).

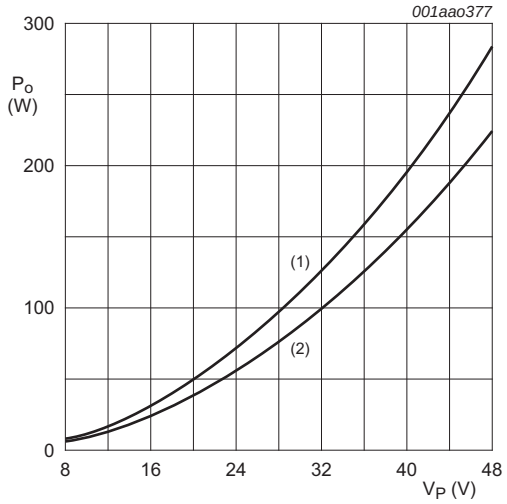
(1) R_L = 6 Ω.

(2) R_L = 8 Ω.

Fig 17. P_o as a function of V_P in stereo mode with THD = 10 %

14.2 Output power estimation (Parallel mode)

Figure 18 and Figure 19 show the estimated output power at THD = 0.5 % and THD = 10 % as a function of the supply voltage for different load impedances in parallel mode.



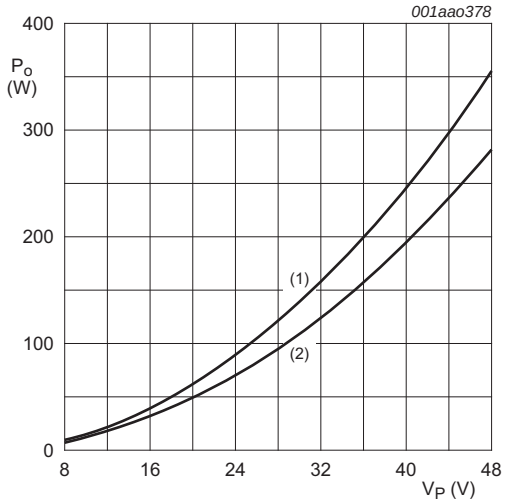
THD = 0.5 %.

R_{DSon} = 0.31 Ω (at T_j = 100 °C), R_s = 0.025 Ω, $t_{w(min)}$ = 250 ns and $I_{O(ocp)}$ = 16 A (typical).

(1) R_L = 3 Ω.

(2) R_L = 4 Ω.

Fig 18. P_o as a function of V_P in parallel mode with THD = 0.5 %



THD = 10 %.

R_{DSon} = 0.31 Ω (at T_j = 100 °C), R_s = 0.025 Ω, $t_{w(min)}$ = 250 ns and $I_{O(ocp)}$ = 16 A (typical).

(1) R_L = 3 Ω.

(2) R_L = 4 Ω.

Fig 19. P_o as a function of V_P parallel mode with THD = 10 %

14.3 Output current limiting

The peak output current is internally limited to 6.5 A minimum. During normal operation, the output current should not exceed this threshold level otherwise the output signal will be distorted. The peak output current can be estimated using Equation 3:

$$I_o \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 6.5\ [A] \quad (3)$$

- I_o = output current (A)
- V_P = supply voltage (V)
- R_L = load impedance (Ω)
- R_{DSon} = on-resistance of power switch (Ω)
- R_s = series resistance of output inductor (Ω)

Example: A 6 Ω speaker can be used with a supply voltage of 45 V before current limiting is triggered.

Current limiting (clipping) avoids audio holes but causes distortion similar to voltage clipping.

14.4 Speaker configuration and impedance

A flat-frequency response (due to a 2nd order Butterworth filter) is obtained by changing the low-pass filter components (L_{LC}, C_{LC}) based on the speaker configuration and impedance. Figure 20 shows the required values.

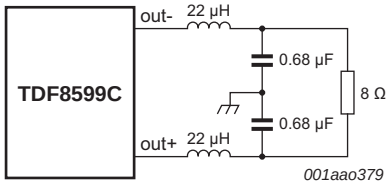


Fig 20. Filter component values

14.5 Heat sink requirements

In most applications, it is necessary to connect an external heat sink to the TDF8599C. Thermal foldback activates at T_j = 140 °C. The expression below shows the relationship between the maximum power dissipation before activation of thermal foldback and the total thermal resistance from junction to ambient:

$$R_{th(j\text{-}a)} = \frac{T_{j(max)} - T_{amb}}{P_{max}} [\mathrm{K/W}] \quad (4)$$

P_{max} is determined by the efficiency (η) of the TDF8599C. The efficiency measured as a function of output power is given in Figure 27. The power dissipation can be derived as a function of output power (see Figure 26).

Example 1:

- V_P = 40 V
- P_o = 2 × 25 W into 8 Ω (THD = 10 % continuous)
- $T_{j(max)}$ = 140 °C
- T_{amb} = 25 °C
- P_{max} = 9 W (from Figure 26)
- The required $R_{th(j\text{-}a)}$ = 115 °C / 9 W = 12 K/W

The total thermal resistance $R_{th(j\text{-}a)}$ consists of: $R_{th(j\text{-}c)}$ + $R_{th(c\text{-}h)}$ + $R_{th(h\text{-}a)}$

Where:

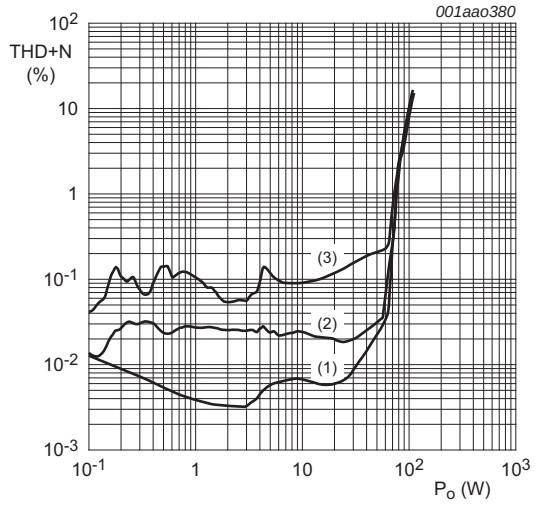
- Thermal resistance from junction to case ($R_{th(j\text{-}c)}$) = 1 K/W
- Thermal resistance from case to heat sink ($R_{th(c\text{-}h)}$) = 0.5 K/W to 1 K/W (depending on mounting)
- Thermal resistance from heat sink to ambient ($R_{th(h\text{-}a)}$) would then be 12 − (1 + 1) = 10 K/W.

If an audio signal has a crest factor of 10 (the ratio between peak power and average power = 10 dB) then T_j will be much lower.

Example 2:

- V_P = 40 V
- P_o = 2 × (25 W / 10) = 2 × 2.5 W into 8 Ω (audio with crest factor of 10)
- T_{amb} = 25 °C
- P_{max} = 6 W
- $R_{th(j-a)}$ = 10 K/W
- $T_{j(max)}$ = 25 °C + (6 W × 10 K/W) = 85 °C

14.6 Curves measured in reference design

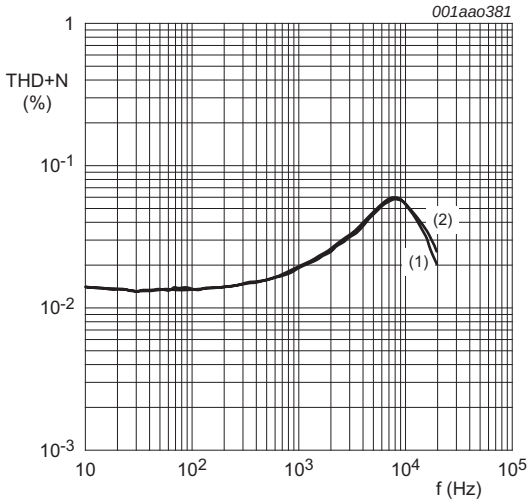


(1) V_P = 40 V; R_L = 8 Ω at 100 Hz.

(2) V_P = 40 V; R_L = 8 Ω at 1 kHz.

(3) V_P = 40 V, R_L = 8 Ω at 6 kHz.

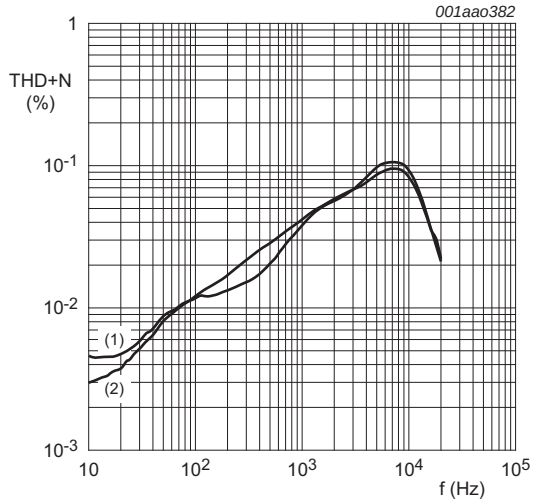
Fig 21. THD + N as a function of output power with a 8 Ω load; V_P = 40 V



(1) Channel 1; V_P = 40 V; R_L = 8 Ω at 1 W.

(2) Channel 2; V_P = 40 V; R_L = 8 Ω at 1 W.

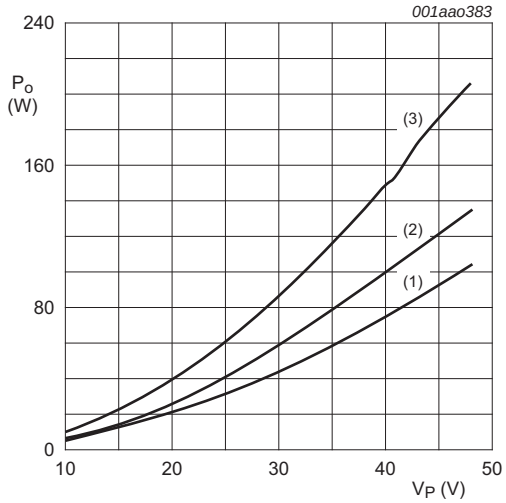
Fig 22. THD + N as a function of frequency with an 8 Ω load, P_o = 1 W



(1) Channel 1; V_P = 40 V; R_L = 8 Ω at 10 W.

(2) Channel 2; V_P = 40 V; R_L = 8 Ω at 10 W.

Fig 23. THD + N as a function of frequency with an 8 Ω load, P_o = 10 W



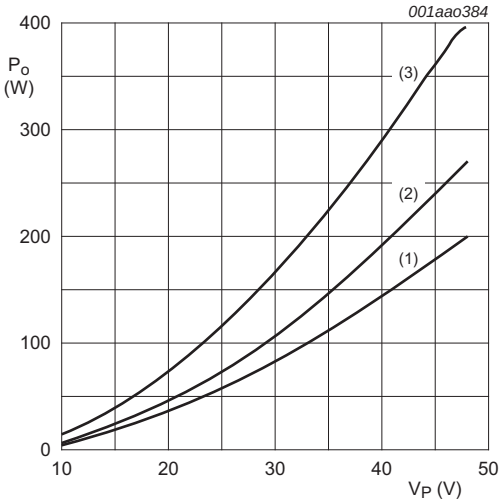
f = 1 kHz; R_L = 8 Ω.

(1) THD = 1 %.

(2) THD = 10 %.

(3) Maximum output power.

Fig 24. Output power as a function of supply voltage; stereo mode



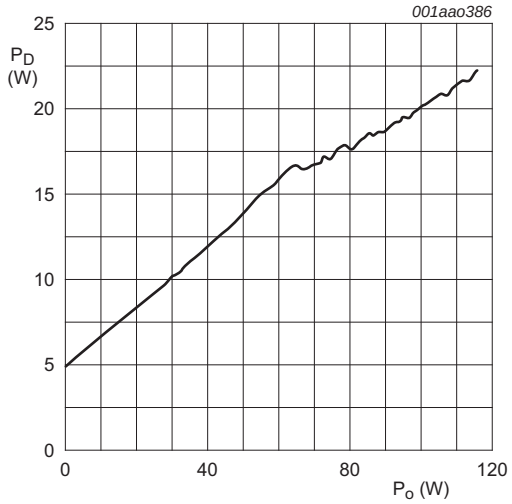
f = 1 kHz; R_L = 4 Ω.

(1) THD = 1 %.

(2) THD = 10 %.

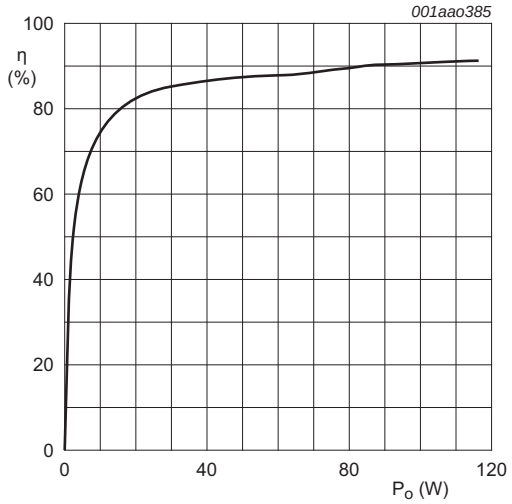
(3) Maximum output power.

Fig 25. Output power as a function of supply voltage; parallel mode



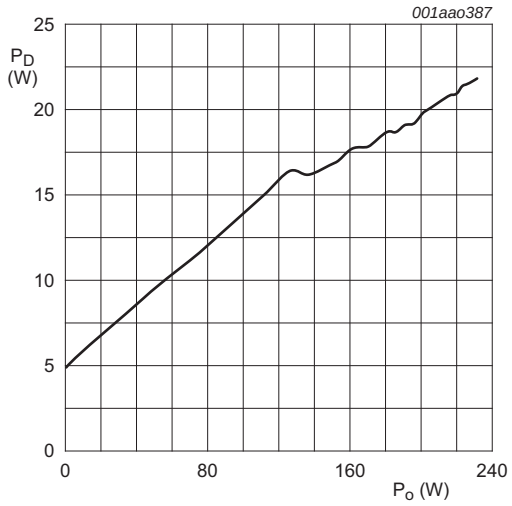
V_P = 40 V; R_L = 8 Ω; f = 1 kHz.

Fig 26. Power dissipation as a function of output power per channel with both channels driven



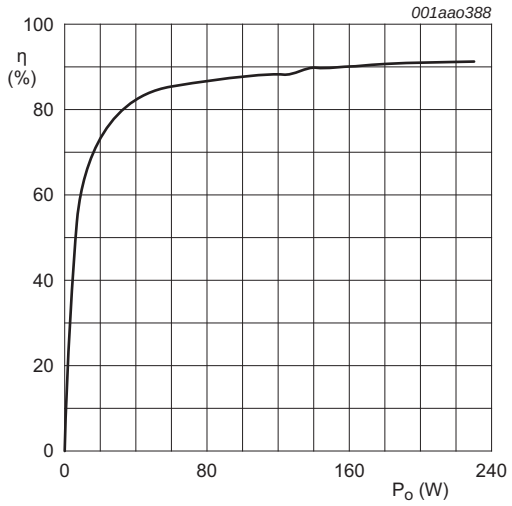
V_P = 40 V; R_L = 8 Ω; f = 1 kHz.

Fig 27. Efficiency as a function of output power per channel with both channels driven



V_P = 40 V; R_L = 4 Ω; f = 1 kHz.

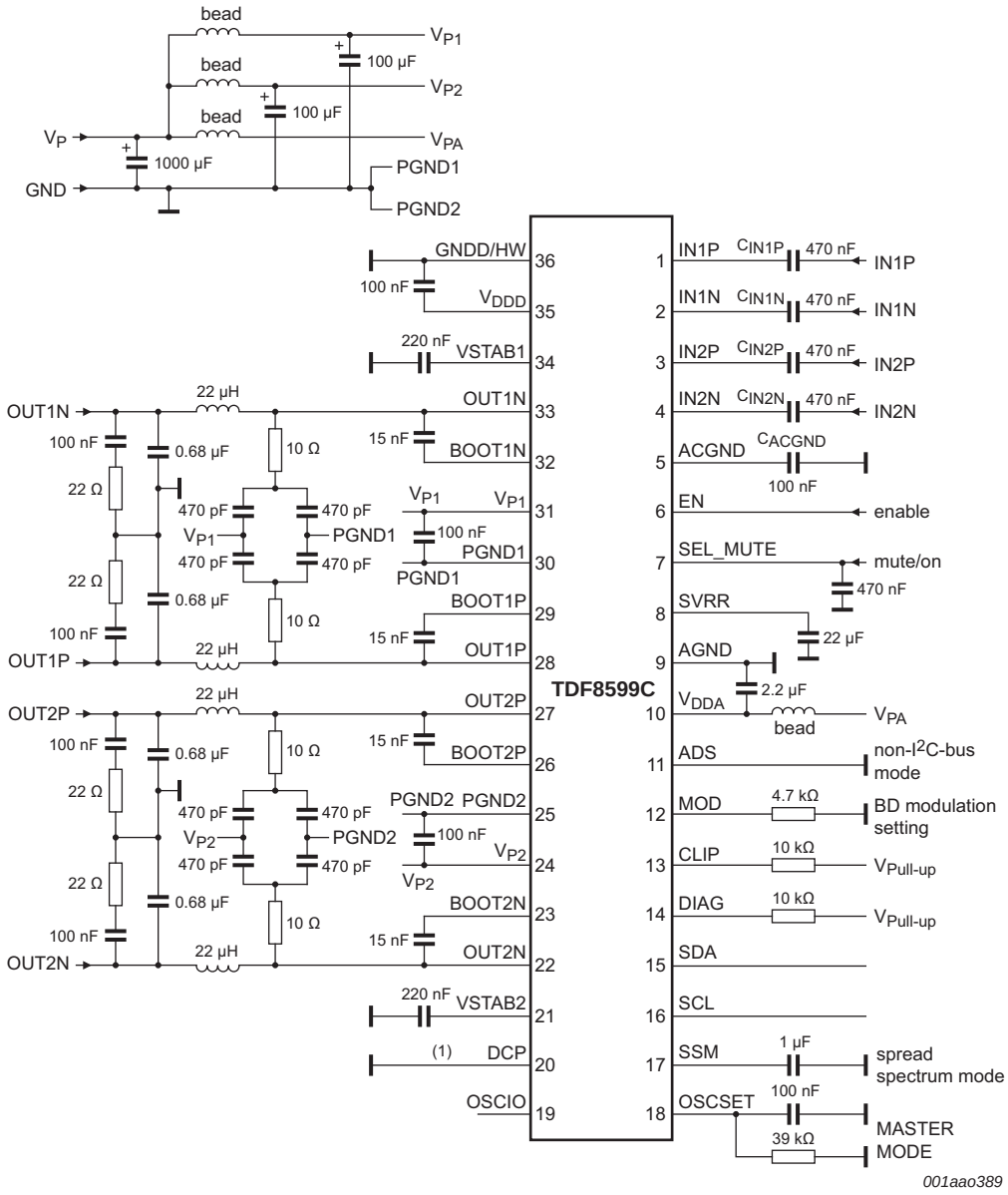
Fig 28. Power dissipation as a function of output power; parallel mode



V_P = 40 V; R_L = 4 Ω; f = 1 kHz.

Fig 29. Efficiency as a function of output power; parallel mode

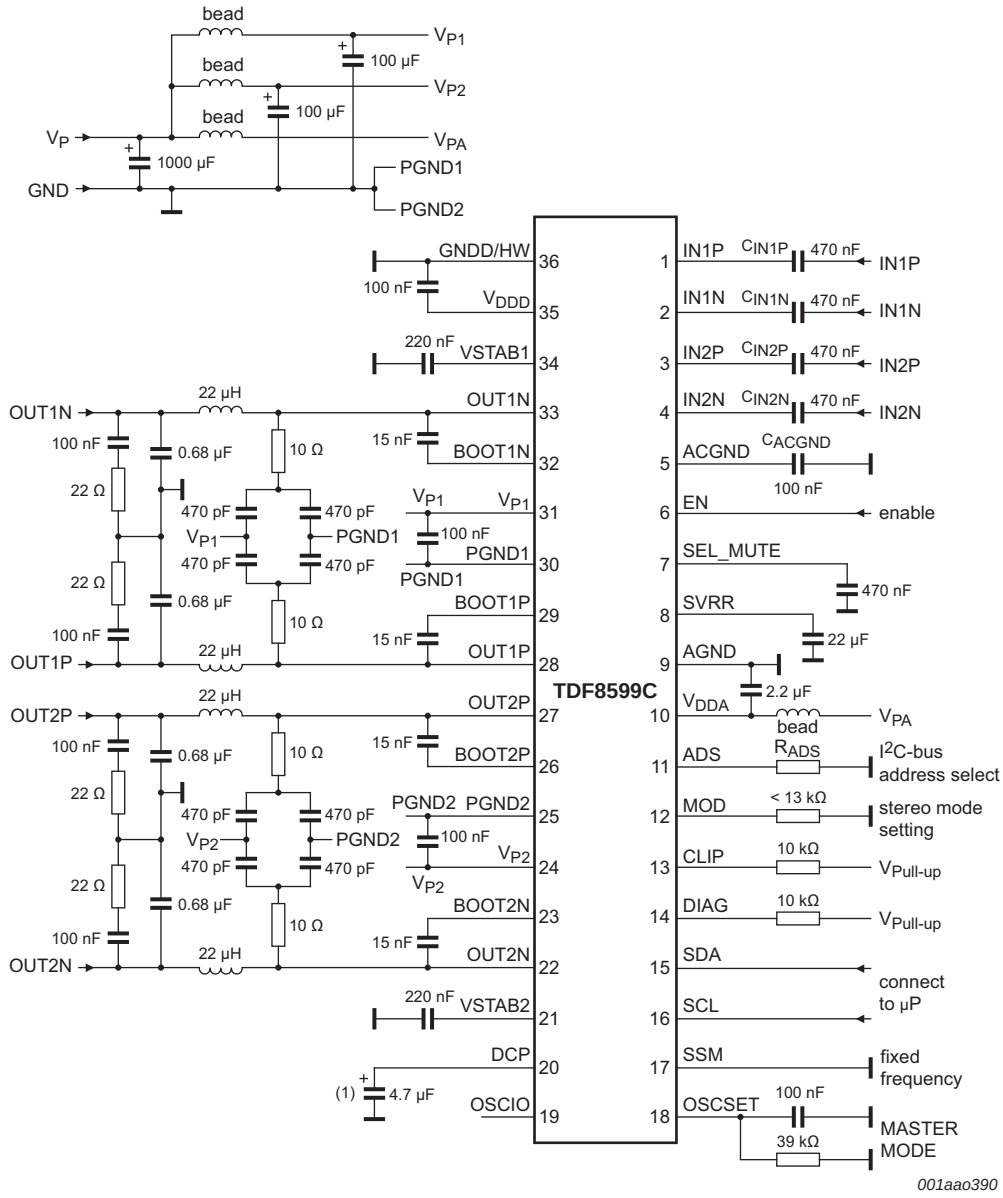
14.7 Typical application schematics



Dual BTL mode (stereo) in non-I²C-bus mode with DC offset protection disabled, Spread spectrum mode enabled BD modulation.

(1) See Section 8.3.5 on page 10 for detailed information on DC offset protection.

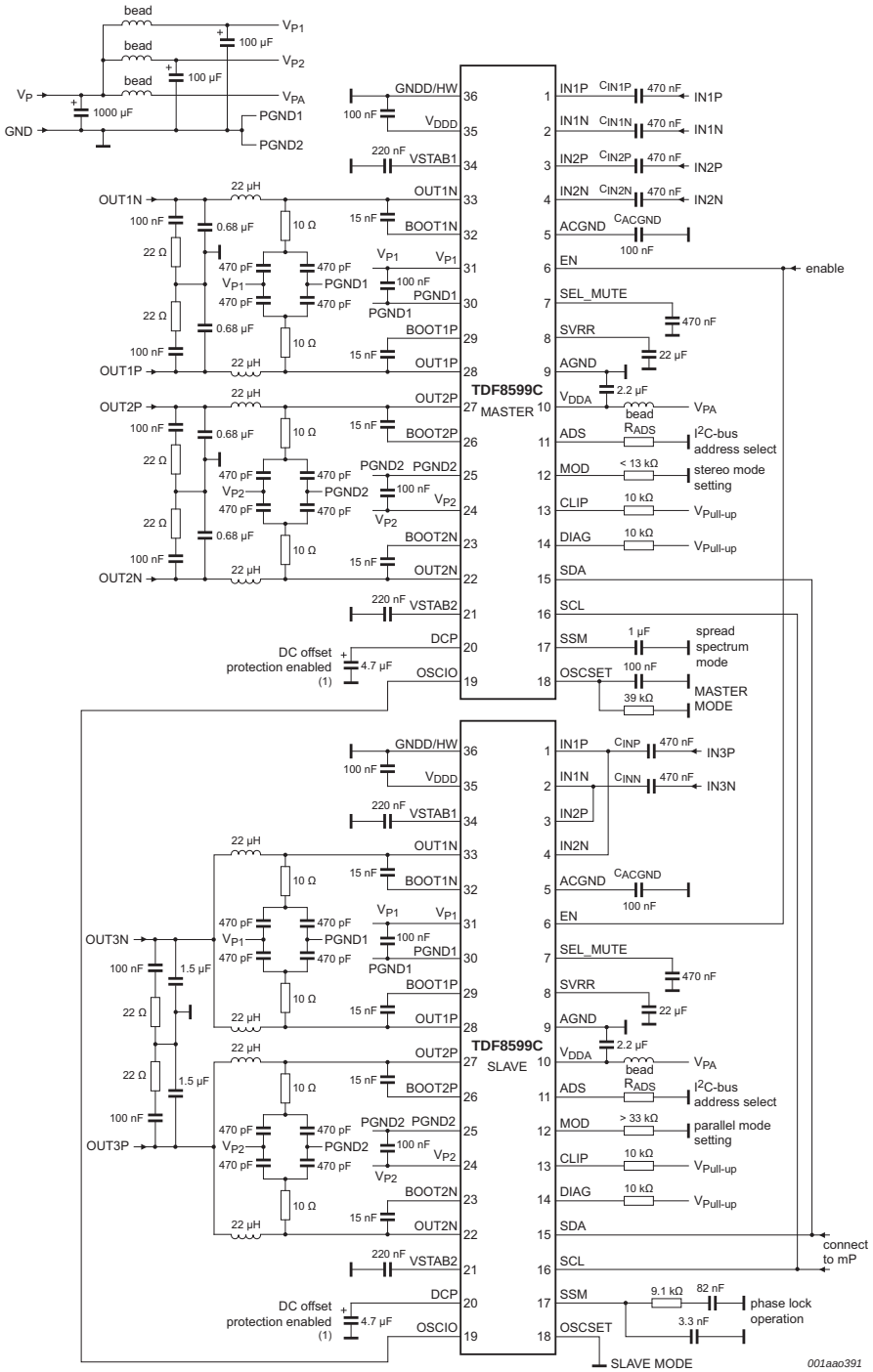
Fig 30. Example application diagram: dual BTL in non-I²C-bus mode



Dual BTL mode (stereo) in I²C-bus mode with DC offset protection enabled, Spread spectrum mode disabled.

(1) See Section 8.3.5 on page 10 for detailed information on DC offset protection.

Fig 31. Example application diagram: dual BTL in I²C-bus mode



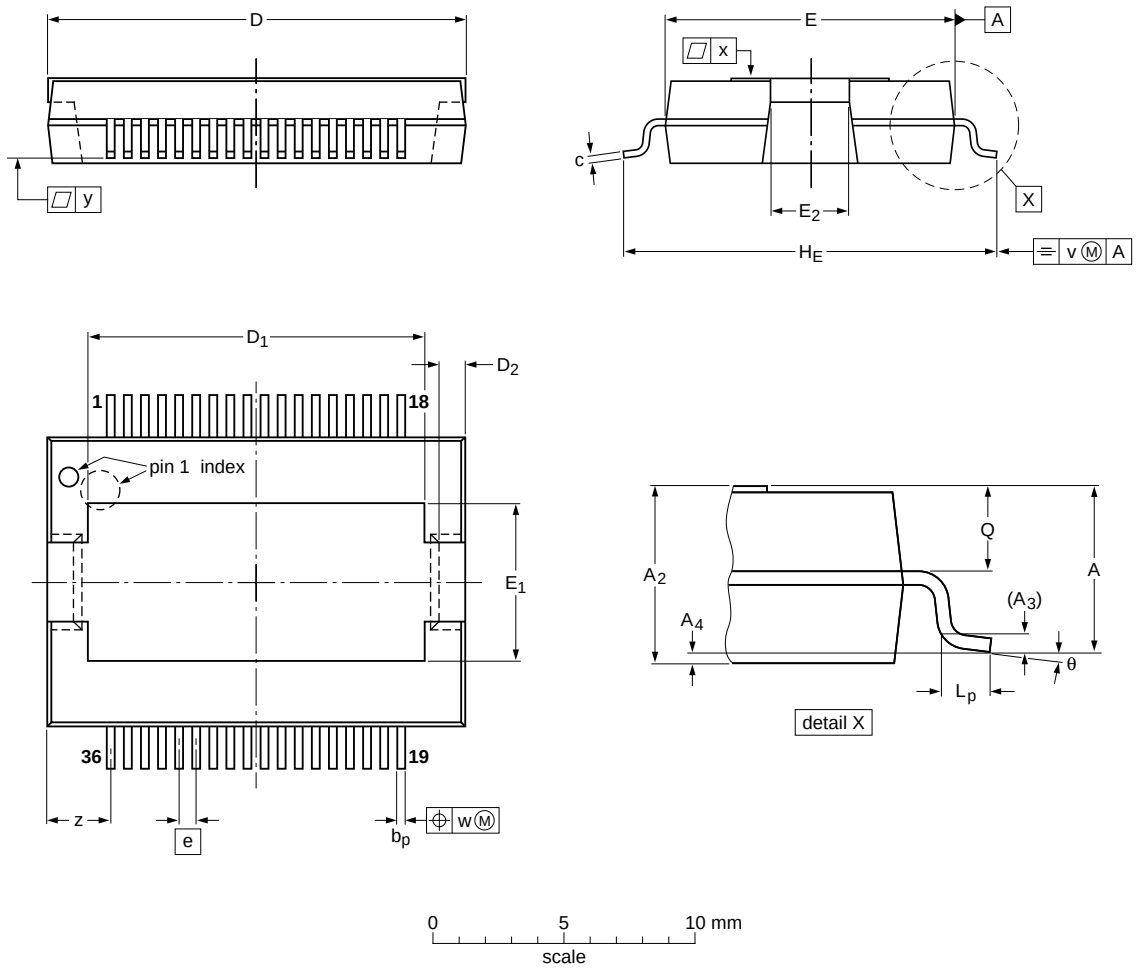
I²C-bus mode: dual BTL in Master mode, one BTL in Slave mode; DC offset protection enabled.

(1) See Section 8.3.5 on page 10 for detailed information on disabling DC offset protection.

Fig 32. Example application diagram: dual BTL master, single BTL slave in I²C-bus mode

15. Package outline

HSOP36: plastic, heatsink small outline package; 36 leads; low stand-off height **SOT851-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.38 0.25	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	0.65	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.12	0.03	0.07	2.55 2.20	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT851-2						04-05-04

Fig 33. Package outline SOT851-2 (HSOP36)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 34) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17 and 18

Table 17. SnPb eutectic process (from J-STD-020C)

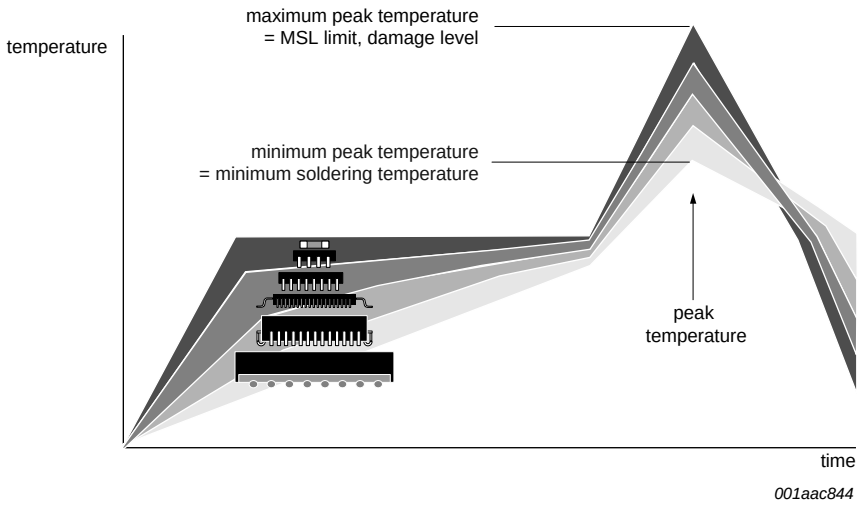
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 18. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.



MSL: Moisture Sensitivity Level

Fig 34. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 19. Abbreviations

Abbreviation	Description
BCDMOS	Bipolar Complementary and double Diffused Metal-Oxide Semiconductor
BTL	Bridge-Tied Load
DCP	DC offset Protection
DMOST	double Diffused Metal-Oxide Semiconductor Transistor
EMI	ElectroMagnetic Interference
I²C	Inter-Integrated Circuit
LSB	Least Significant Bit
Mμp	Master microprocessor
MSB	Most Significant Bit
NDMOST	N-type double Diffused Metal-Oxide Semiconductor Transistor
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse-Width Modulation
SOI	Silicon On Insulator

Table 19. Abbreviations *...continued*

Abbreviation	Description
TFP	Thermal Foldback Protection
UVP	UnderVoltage Protection
WP	Window Protection

18. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8599C_SDS v.1	20110805	Product short data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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