# ADC1413D series

## Dual 14-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps; serial JESD204A interface

Rev. 07 — 2 July 2012 Product data sheet

## 1. General description

The ADC1413D is a dual-channel 14-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1413D is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a 3 V source for analog and a 1.8 V source for the output driver, it embeds two serial outputs. Each lane is differential and complies with the JESD204A standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADCs. A set of IC configurations is also available via the binary level control pins taken, which are used at power-up. The device also includes a programmable full-scale SPI to allow a flexible input voltage range of 1 V to 2 V (peak-to-peak).

Excellent dynamic performance is maintained from the baseband to input frequencies of 170 MHz or more, making the ADC1413D ideal for use in communications, imaging, and medical applications.

## 2. Features and benefits

- SNR, 72 dBFS; SFDR, 86 dBc
- Sample rate up to 125 Msps
- Clock input divided by 2 for less jitter contribution
- 3 V, 1.8 V power supplies
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- Two configurable serial outputs
- Compliant with JESD204A serial transmission standard
- Pin compatible with the ADC1613D series, ADC1213D series, and ADC1113D125
- Input bandwidth, 600 MHz
- Power dissipation, 995 mW at 80 Msps
- SPI register programming
- Duty cycle stabilizer (DCS)
- High IF capability
- Offset binary, two’s complement, gray code
- Power-down mode and Sleep mode
- HVQFN56 package

## 3. Applications

- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems
- Software defined radio

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Sampling frequency (Msps) | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| ADC1413D125HN-C1 | 125 | HVQFN56 | plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm | SOT684-7 |
| ADC1413D105HN-C1 | 105 | HVQFN56 | plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm | SOT684-7 |
| ADC1413D080HN-C1 | 80 | HVQFN56 | plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm | SOT684-7 |
| ADC1413D065HN-C1 | 65 | HVQFN56 | plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm | SOT684-7 |

# 5. Block diagram

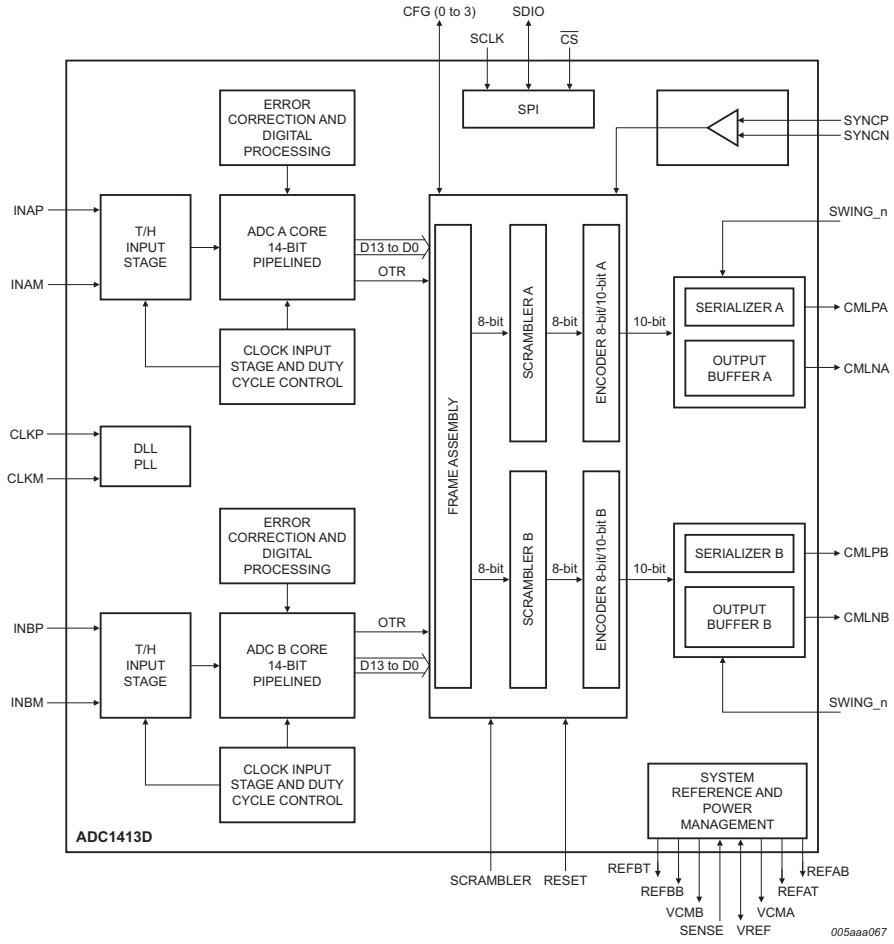



**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

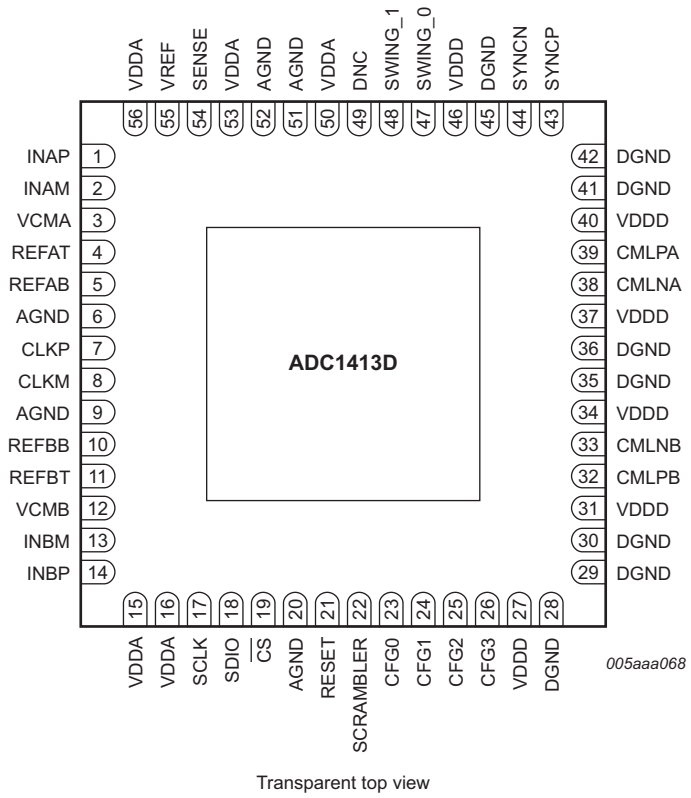



**Fig 2. Pinning diagram**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Type [1] | Description |
|---|---|---|---|
| INAP | 1 | I | channel A analog input |
| INAM | 2 | I | channel A complementary analog input |
| VCMA | 3 | O | channel A output common voltage |
| REFAT | 4 | O | channel A top reference |
| REFAB | 5 | O | channel A bottom reference |
| AGND | 6 | G | analog ground |
| CLKP | 7 | I | clock input |
| CLKM | 8 | I | complementary clock input |
| AGND | 9 | G | analog ground |
| REFBB | 10 | O | channel B bottom reference |
| REFBT | 11 | O | channel B top reference |
| VCMB | 12 | O | channel B output common voltage |
| INBM | 13 | I | channel B complementary analog input |

**Table 2. Pin description** *…continued*

| Symbol | Pin | Type [1] | Description |
|---|---|---|---|
| INBP | 14 | I | channel B analog input |
| VDDA | 15 | P | analog power supply 3 V |
| VDDA | 16 | P | analog power supply 3 V |
| SCLK | 17 | I | SPI clock |
| SDIO | 18 | I/O | SPI data input/output |
| $\overline{CS}$ | 19 | I | chip select |
| AGND | 20 | G | analog ground |
| RESET | 21 | I | JEDEC digital IP reset |
| SCRAMBLER | 22 | I | scrambler enable and disable |
| CFG0 | 23 | I/O | See Table 28 (input) or OTRA (output)[2] |
| CFG1 | 24 | I/O | See Table 28 (input) or OTRB (output)[2] |
| CFG2 | 25 | I/O | See Table 28 (input) |
| CFG3 | 26 | I/O | See Table 28 (input) |
| VDDD | 27 | P | digital power supply 1.8 V |
| DGND | 28 | G | digital ground |
| DGND | 29 | G | digital ground |
| DGND | 30 | G | digital ground |
| VDDD | 31 | P | digital power supply 1.8 V |
| CMLPB | 32 | O | channel B output |
| CMLNB | 33 | O | channel B complementary output |
| VDDD | 34 | P | digital power supply 1.8 V |
| DGND | 35 | G | digital ground |
| DGND | 36 | G | digital ground |
| VDDD | 37 | P | digital power supply 1.8 V |
| CMLNA | 38 | O | channel A complementary output |
| CMLPA | 39 | O | channel A output |
| VDDD | 40 | P | digital power supply 1.8 V |
| DGND | 41 | G | digital ground |
| DGND | 42 | G | digital ground |
| SYNCP | 43 | I | synchronization from FPGA |
| SYNCN | 44 | I | synchronization from FPGA |
| DGND | 45 | G | digital ground |
| VDDD | 46 | P | digital power supply 1.8 V |
| SWING_0 | 47 | I | JESD204 serial buffer programmable output swing |
| SWING_1 | 48 | I | JESD204 serial buffer programmable output swing |
| DNC | 49 | O | do not connect |
| VDDA | 50 | P | analog power supply 3 V |
| AGND | 51 | G | analog ground |
| AGND | 52 | G | analog ground |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Type [1] | Description |
|---|---|---|---|
| VDDA | 53 | P | analog power supply 3 V |
| SENSE | 54 | I | reference programming pin |
| VREF | 55 | I/O | voltage reference input/output |
| VDDA | 56 | P | analog power supply 3 V |

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

[2] OTRA stands for “OuT of Range A”. OTRB stands for “OuT of Range B”

# 7. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDA}$ | analog supply voltage | | −0.4 | +4.6 | V |
| $V_{DDD}$ | digital supply voltage | | −0.4 | +2.5 | V |
| $T_{stg}$ | storage temperature | | −55 | +125 | °C |
| $T_{amb}$ | ambient temperature | | −40 | +85 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |

# 8. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | [1] | 17.8 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | | [1] | 6.8 | K/W |

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

# 9. Static characteristics

**Table 5. Static characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DDA}$ | analog supply voltage | | 2.85 | 3.0 | 3.4 | V |
| $V_{DDD}$ | digital supply voltage | | 1.65 | 1.8 | 1.95 | V |
| $I_{DDA}$ | analog supply current | $f_{clk}$ = 125 Msps; $f_i$ = 70 MHz | - | 343 | - | mA |
| $I_{DDD}$ | digital supply current | $f_{clk}$ = 125 Msps; $f_i$ = 70 MHz | - | 150 | - | mA |
| $P_{tot}$ | total power dissipation | $f_{clk}$ = 125 Msps | - | 1270 | - | mW |
| | | $f_{clk}$ = 105 Msps | - | 1150 | - | mW |
| | | $f_{clk}$ = 80 Msps | - | 995 | - | mW |
| | | $f_{clk}$ = 65 Msps | - | 885 | - | mW |
| P | power dissipation | Power-down mode | - | 30 | - | mW |
| | | Standby mode | - | 200 | - | mW |
| **Clock inputs: pins CLKP and CLKM (AC-coupled)** | | | | | | |
| Low-Voltage Positive Emitter-Coupled Logic (LVPECL) | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak-to-peak | - | 1.6 | - | V |
| SINE | | | | | | |
| $V_{i(clk)dif}$ | differential clock input voltage | peak | - | ±3.0 | - | V |
| Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | - | $0.3V_{DDA}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDA}$ | - | - | V |
| **Logic inputs: Power-down: pins CFG0 to CFG3, SCRAMBLER, SWING_0, SWING_1, and RESET** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | 0 | - | V |
| $V_{IH}$ | HIGH-level input voltage | | - | $0.66V_{DDD}$ | - | V |
| $I_{IL}$ | LOW-level input current | | –6 | - | +6 | µA |
| $I_{IH}$ | HIGH-level input current | | –30 | - | +30 | µA |
| **SPI: pins $\overline{CS}$, SDIO, and SCLK** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | 0 | - | $0.3V_{DDA}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DDA}$ | - | $V_{DDA}$ | V |
| $I_{IL}$ | LOW-level input current | | –10 | - | +10 | µA |
| $I_{IH}$ | HIGH-level input current | | –50 | - | +50 | µA |
| $C_I$ | input capacitance | | - | 4 | - | pF |
| **Analog inputs: pins INAP, INAM, INBP, and INBM** | | | | | | |
| $I_I$ | input current | track mode | –5 | - | +5 | µA |
| $R_I$ | input resistance | track mode | - | 15 | - | Ω |
| $C_I$ | input capacitance | track mode | - | 5 | - | pF |
| $V_{I(cm)}$ | common-mode input voltage | track mode | 0.9 | 1.5 | 2 | V |

**Table 5. Static characteristics[1]** *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $B_i$ | input bandwidth | | - | 600 | - | MHz |
| $V_{I(dif)}$ | differential input voltage | peak-to-peak | 1 | - | 2 | V |
| **Voltage controlled regulator output: pins VCMA and VCMB** | | | | | | |
| $V_{O(cm)}$ | common-mode output voltage | | - | $V_{DDA}$ / 2 | - | V |
| $I_{O(cm)}$ | common-mode output current | | - | 4 | - | mA |
| **Reference voltage input/output: pin VREF** | | | | | | |
| $V_{VREF}$ | voltage on pin VREF | output | 0.5 | - | 1 | V |
| | | input | 0.5 | - | 1 | V |
| **Data outputs: pins CMLPA, CMLNA** | | | | | | |
| Output levels, $V_{DDD}$ = 1.8 V; SWING_SEL[2:0] = 000 | | | | | | |
| $V_{OL}$ | LOW-level output voltage | DC coupled; output | - | 1.5 | - | V |
| | | AC coupled | - | 1.35 | - | V |
| $V_{OH}$ | HIGH-level output voltage | DC coupled; output | - | 1.8 | - | V |
| | | AC coupled | - | 1.65 | - | V |
| Output levels, $V_{DDD}$ = 1.8 V; SWING_SEL[2:0] = 001 | | | | | | |
| $V_{OL}$ | LOW-level output voltage | DC coupled; output | - | 1.45 | - | V |
| | | AC coupled | - | 1.275 | - | V |
| $V_{OH}$ | HIGH-level output voltage | DC coupled; output | - | 1.8 | - | V |
| | | AC coupled | - | 1.625 | - | V |
| Output levels, $V_{DDD}$ = 1.8 V; SWING_SEL[2:0] = 010 | | | | | | |
| $V_{OL}$ | LOW-level output voltage | DC coupled; output | - | 1.4 | - | V |
| | | AC coupled | - | 1.2 | - | V |
| $V_{OH}$ | HIGH-level output voltage | DC coupled; output | - | 1.8 | - | V |
| | | AC coupled | - | 1.6 | - | V |
| Output levels, $V_{DDD}$ = 1.8 V; SWING_SEL[2:0] = 011 | | | | | | |
| $V_{OL}$ | LOW-level output voltage | DC coupled; output | - | 1.35 | - | V |
| | | AC coupled | - | 1.125 | - | V |
| $V_{OH}$ | HIGH-level output voltage | DC coupled; output | - | 1.8 | - | V |
| | | AC coupled | - | 1.575 | - | V |
| Output levels, $V_{DDD}$ = 1.8 V; SWING_SEL[2:0] = 100 | | | | | | |
| $V_{OL}$ | LOW-level output voltage | DC coupled; output | - | 1.3 | - | V |
| | | AC coupled | - | 1.05 | - | V |
| $V_{OH}$ | HIGH-level output voltage | DC coupled; output | - | 1.8 | - | V |
| | | AC coupled | - | 1.55 | - | V |
| **Serial configuration: pins SYNCCP, SYNCCN** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | differential; input | - | 0.95 | - | V |
| $V_{IH}$ | HIGH-level input voltage | differential; input | - | 1.47 | - | V |
| **Accuracy** | | | | | | |
| INL | integral non-linearity | | - | ±5 | - | LSB |

**Table 5. Static characteristics[1]** *…continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DNL | differential non-linearity | guaranteed no missing codes | −0.95 | ±0.5 | +0.95 | LSB |
| $E_{offset}$ | offset error | | - | ±2 | - | mV |
| $E_G$ | gain error | full-scale | - | ± 0.5 | - | % |
| $M_{G(CTC)}$ | channel-to-channel gain matching | | - | 1.1 | - | % |
| **Supply** | | | | | | |
| PSRR | power supply rejection ratio | 200 mV (p-p) on pin VDDA; $f_i$ = DC | - | −54 | - | dB |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V, $T_{amb}$ = 25 °C. Minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V; $V_I$ (INAP, INBP) − $V_I$ (INAM, INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

# 10. Dynamic characteristics

## 10.1 Dynamic characteristics

**Table 6. Dynamic characteristics[1]**

| Symbol | Parameter | Conditions | ADC1413D065 | | | ADC1413D080 | | | ADC1413D105 | | | ADC1413D125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Analog signal processing** | | | | | | | | | | | | | | | |
| $\alpha_{2H}$ | second harmonic level | $f_i$ = 3 MHz | - | 87 | - | - | 87 | - | - | 86 | - | - | 88 | - | dBc |
| | | $f_i$ = 30 MHz | - | 86 | - | - | 86 | - | - | 86 | - | - | 87 | - | dBc |
| | | $f_i$ = 70 MHz | - | 85 | - | - | 85 | - | - | 84 | - | - | 85 | - | dBc |
| | | $f_i$ = 170 MHz | - | 82 | - | - | 82 | - | - | 81 | - | - | 83 | - | dBc |
| $\alpha_{3H}$ | third harmonic level | $f_i$ = 3 MHz | - | 86 | - | - | 86 | - | - | 85 | - | - | 87 | - | dBc |
| | | $f_i$ = 30 MHz | - | 85 | - | - | 85 | - | - | 85 | - | - | 86 | - | dBc |
| | | $f_i$ = 70 MHz | - | 84 | - | - | 84 | - | - | 83 | - | - | 84 | - | dBc |
| | | $f_i$ = 170 MHz | - | 81 | - | - | 81 | - | - | 80 | - | - | 82 | - | dBc |
| THD | total harmonic distortion | $f_i$ = 3 MHz | - | 83 | - | - | 83 | - | - | 82 | - | - | 84 | - | dBc |
| | | $f_i$ = 30 MHz | - | 82 | - | - | 82 | - | - | 82 | - | - | 83 | - | dBc |
| | | $f_i$ = 70 MHz | - | 81 | - | - | 81 | - | - | 80 | - | - | 81 | - | dBc |
| | | $f_i$ = 170 MHz | - | 78 | - | - | 78 | - | - | 77 | - | - | 79 | - | dBc |
| ENOB | effective number of bits | $f_i$ = 3 MHz | - | 11.7 | - | - | 11.7 | - | - | 11.6 | - | - | 11.6 | - | bits |
| | | $f_i$ = 30 MHz | - | 11.6 | - | - | 11.5 | - | - | 11.5 | - | - | 11.5 | - | bits |
| | | $f_i$ = 70 MHz | - | 11.5 | - | - | 11.5 | - | - | 11.4 | - | - | 11.4 | - | bits |
| | | $f_i$ = 170 MHz | - | 11.4 | - | - | 11.4 | - | - | 11.3 | - | - | 11.3 | - | bits |
| SNR | signal-to-noise ratio | $f_i$ = 3 MHz | - | 72.1 | - | - | 72.0 | - | - | 71.8 | - | - | 71.4 | - | dBFS |
| | | $f_i$ = 30 MHz | - | 71.3 | - | - | 71.2 | - | - | 71.2 | - | - | 71.1 | - | dBFS |
| | | $f_i$ = 70 MHz | - | 70.7 | - | - | 70.7 | - | - | 70.6 | - | - | 70.5 | - | dBFS |
| | | $f_i$ = 170 MHz | - | 70.2 | - | - | 70.1 | - | - | 70.0 | - | - | 69.9 | - | dBFS |
| SFDR | spurious-free dynamic range | $f_i$ = 3 MHz | - | 86 | - | - | 86 | - | - | 85 | - | - | 87 | - | dBc |
| | | $f_i$ = 30 MHz | - | 85 | - | - | 85 | - | - | 85 | - | - | 86 | - | dBc |
| | | $f_i$ = 70 MHz | - | 84 | - | - | 84 | - | - | 83 | - | - | 84 | - | dBc |
| | | $f_i$ = 170 MHz | - | 81 | - | - | 81 | - | - | 80 | - | - | 82 | - | dBc |

**Table 6. Dynamic characteristics[1]** *…continued*

| Symbol | Parameter | Conditions | ADC1413D065 | | | ADC1413D080 | | | ADC1413D105 | | | ADC1413D125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| IMD | intermodulation distortion | $f_i$ = 3 MHz | - | 89 | - | - | 89 | - | - | 88 | - | - | 89 | - | dBc |
| | | $f_i$ = 30 MHz | - | 88 | - | - | 88 | - | - | 88 | - | - | 88 | - | dBc |
| | | $f_i$ = 70 MHz | - | 87 | - | - | 87 | - | - | 86 | - | - | 86 | - | dBc |
| | | $f_i$ = 170 MHz | - | 84 | - | - | 85 | - | - | 83 | - | - | 84 | - | dBc |
| $\alpha_{ct(ch)}$ | channel crosstalk | $f_i$ = 70 MHz | - | 100 | - | - | 100 | - | - | 100 | - | - | 100 | - | dBc |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V, $T_{amb}$ = 25 °C. Minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V; $V_I$ (INAP, INBP) − $V_I$ (INAM, INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

## 10.2 Clock and digital output timing

**Table 7. Clock and digital output characteristics[1]**

| Symbol | Parameter | Conditions | ADC1413D065 | | | ADC1413D080 | | | ADC1413D105 | | | ADC1413D125 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Clock timing input: pins CLKP and CLKM** | | | | | | | | | | | | | | | |
| $f_{clk}$ | clock frequency | | 45 | - | 65 | 60 | - | 80 | 75 | - | 105 | 100 | - | 125 | Msps |
| $t_{lat(data)}$ | data latency time | clock cycles | 307 | - | 850 | 250 | - | 283 | 190 | - | 226 | 160 | - | 170 | ns |
| $\delta_{clk}$ | clock duty cycle | DCS_EN = logic 1 | 30 | 50 | 70 | 30 | 50 | 70 | 30 | 50 | 70 | 30 | 50 | 70 | % |
| $t_{d(s)}$ | sampling delay time | | - | 0.8 | - | - | 0.8 | - | - | 0.8 | - | - | 0.8 | - | ns |
| $t_{wake}$ | wake-up time | | - | 76 | - | - | 76 | - | - | 76 | - | - | 76 | - | µs |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V, $T_{amb}$ = 25 °C. Minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V; $V_I$ (INAP, INBP) − $V_I$ (INAM, INBM) = −1 dBFS; internal reference mode; 100 W differential applied to serial outputs; unless otherwise specified.

## 10.3 Serial output timing

The eye diagram of the serial output is shown in Figure 3 and Figure 4. Test conditions are:

- 3.125 Gbps data rate
- $T_{amb}$ = 25 °C
- DC coupling with two different receiver common-mode voltages

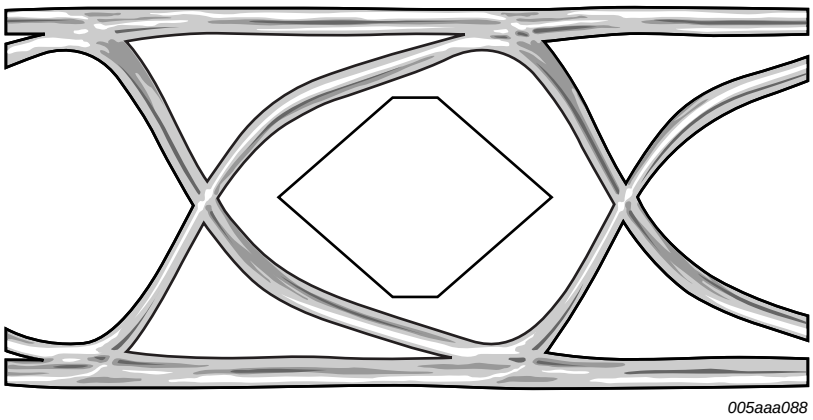



**Fig 3. Eye diagram at 1 V receiver common-mode**

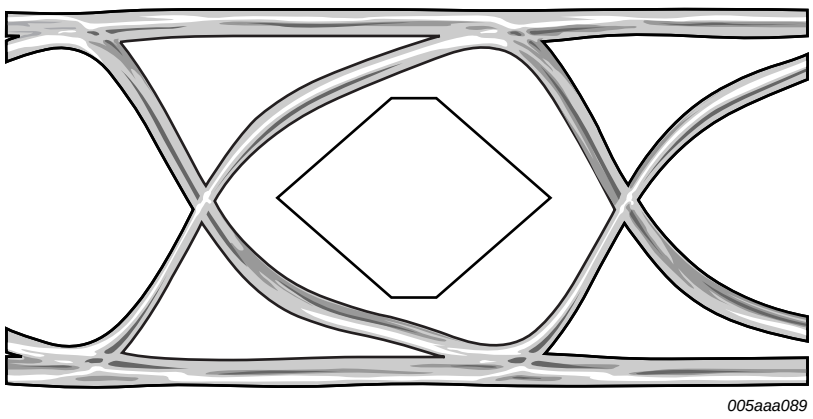



**Fig 4. Eye diagram at 2 V receiver common-mode**

## 10.4 SPI timing

**Table 8. SPI timing characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(SCLK)}$ | SCLK pulse width | | - | 40 | - | ns |
| $t_{w(SCLKH)}$ | SCLK HIGH pulse width | | - | 16 | - | ns |
| $t_{w(SCLKL)}$ | SCLK LOW pulse width | | - | 16 | - | ns |
| $t_{su}$ | set-up time | data to SCLKH | - | 5 | - | ns |
| | | $\overline{CS}$ to SCLKH | - | 5 | - | ns |
| $t_h$ | hold time | data to SCLKH | - | 2 | - | ns |
| | | $\overline{CS}$ to SCLKH | - | 2 | - | ns |
| $f_{clk(max)}$ | maximum clock frequency | | - | 25 | - | MHz |

[1] Typical values measured at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V, $T_{amb}$ = 25 °C. Minimum and maximum values are across the full temperature range $T_{amb}$ = −40 °C to +85 °C at $V_{DDA}$ = 3 V, $V_{DDD}$ = 1.8 V; $V_I$ (INAP, INBP) − $V_I$ (INAM,INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

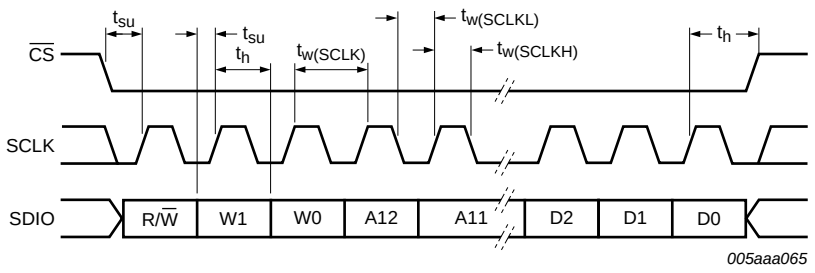



**Fig 5. SPI timing**

# 11. Application information

## 11.1 Analog inputs

### 11.1.1 Input stage description

The analog input of the ADC1413D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INxP and INxM set to $0.5V_{DDA}$.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.2 and Table 21).

Figure 6 shows the equivalent circuit of the sample-and-hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics.

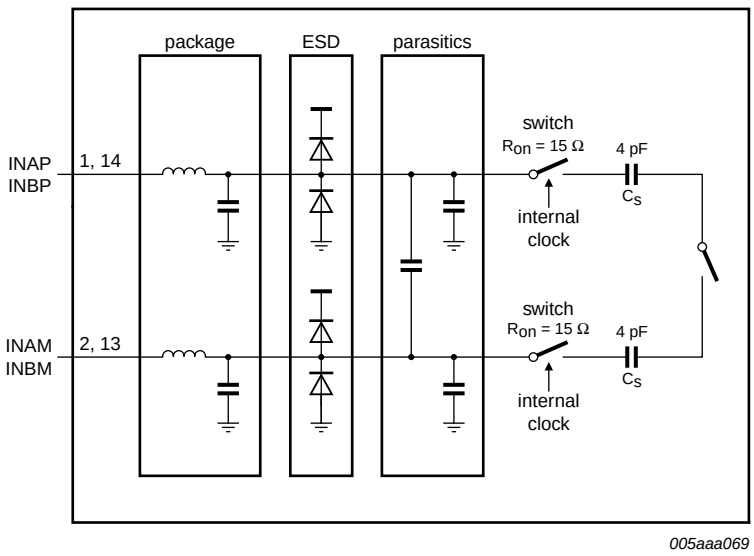



**Fig 6. Input sampling circuit**

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

### 11.1.2 Anti-kickback circuitry

Anti-kickback circuitry (RC filter in Figure 7) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

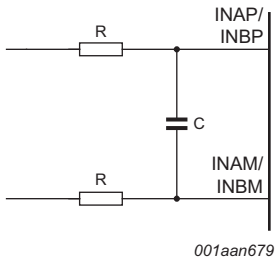



**Fig 7. Anti-kickback circuit**

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

**Table 9. RC coupling versus input frequency, typical values**

| Input frequency (MHz) | Resistance (Ω) | Capacitance (pF) |
|---|---|---|
| 3 | 25 | 12 |
| 70 | 12 | 8 |
| 170 | 12 | 8 |

### 11.1.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 8 would be suitable for a baseband application.

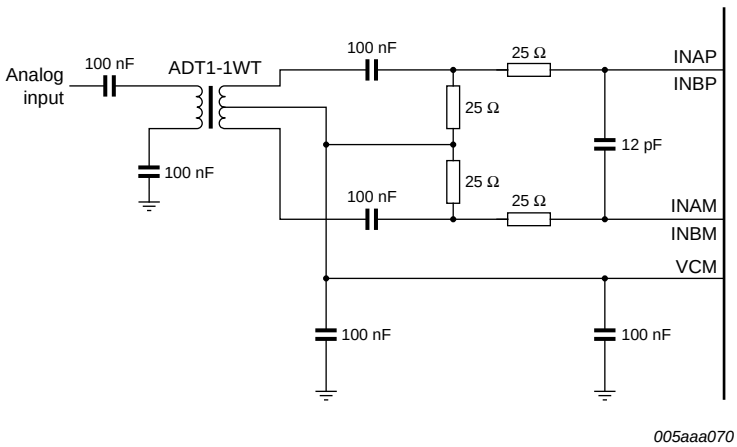



**Fig 8. Single transformer configuration**

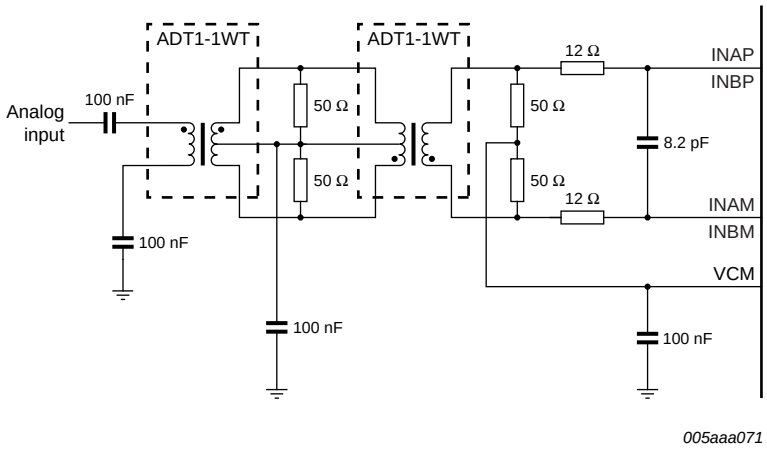



**Fig 9. Dual transformer configuration**

The configuration shown in Figure 9 is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

## 11.2 System reference and power management

### 11.2.1 Internal/external reference

The ADC1413D has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (see Figure 11 to Figure 14), in 1 dB steps between 0 dB and −6 dB, via SPI control bits INTREF[2:0] (when bit INTREF_EN = logic 1; see Table 21). The equivalent reference circuit is shown in Figure 10. An external reference is also possible by providing a voltage on pin VREF as described in Figure 13.

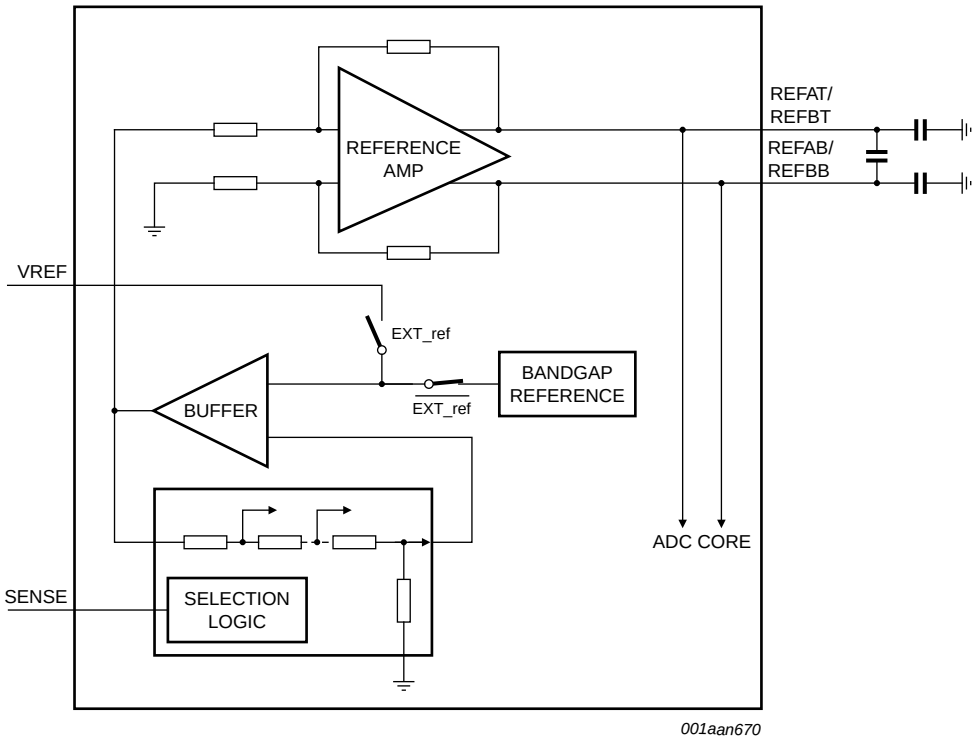



**Fig 10. Reference equivalent schematic**

If bit INTREF_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 10.

**Table 10. Reference modes**

| Mode | SPI bit, "Internal reference" | SENSE pin | VREF pin | Full-scale (V (p-p)) |
|---|---|---|---|---|
| Internal (Figure 11) | 0 | GND | 330 pF capacitor to GND | 2 |
| Internal (Figure 12) | 0 | VREF pin = SENSE pin and 330 pF capacitor to GND | | 1 |
| External (Figure 13) | 0 | $V_{DDA}$ | external voltage from 0.5 V to 1 V | 1 to 2 |
| Internal, SPI mode (Figure 14) | 1 | VREF pin = SENSE pin and 330 pF capacitor to GND | | 1 to 2 |

Figure 11 to Figure 14 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

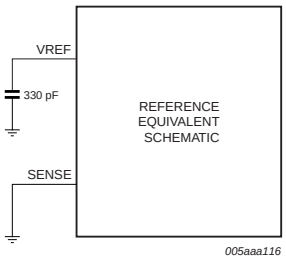



Fig 11. Internal reference, 2 V (p-p) full-scale

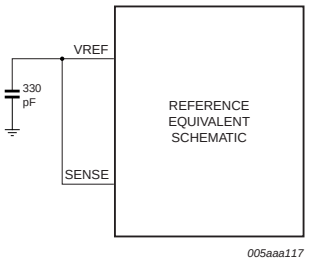



Fig 12. Internal reference, 1 V (p-p) full-scale

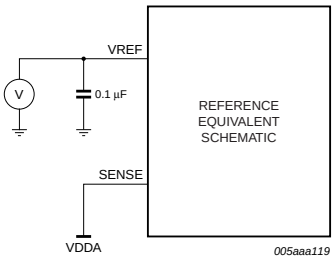



Fig 13. External reference, 1 V (p-p) to 2 V (p-p) full-scale

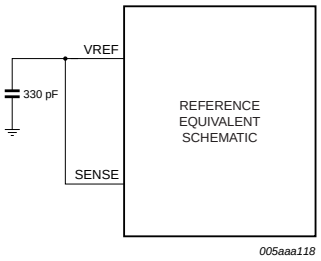



Fig 14. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale

### 11.2.2 Programmable full-scale

The full-scale is programmable between 1 V (p-p) to 2 V (p-p) (see Table 11).

Table 11. Programmable full-scale

| INTREF[2:0] | Level (dB) | Full-scale (V (p-p)) |
|---|---|---|
| 000 | 0 | 2 |
| 001 | −1 | 1.78 |
| 010 | −2 | 1.59 |
| 011 | −3 | 1.42 |
| 100 | −4 | 1.26 |
| 101 | −5 | 1.12 |
| 110 | −6 | 1 |
| 111 | not used | x |

### 11.2.3 Common-mode output voltage ($V_{O(cm)}$)

An 0.1 μF filter capacitor should be connected between pins VCMA and VCMB and ground to ensure a low-noise common-mode output voltage. When AC-coupled, these pins can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

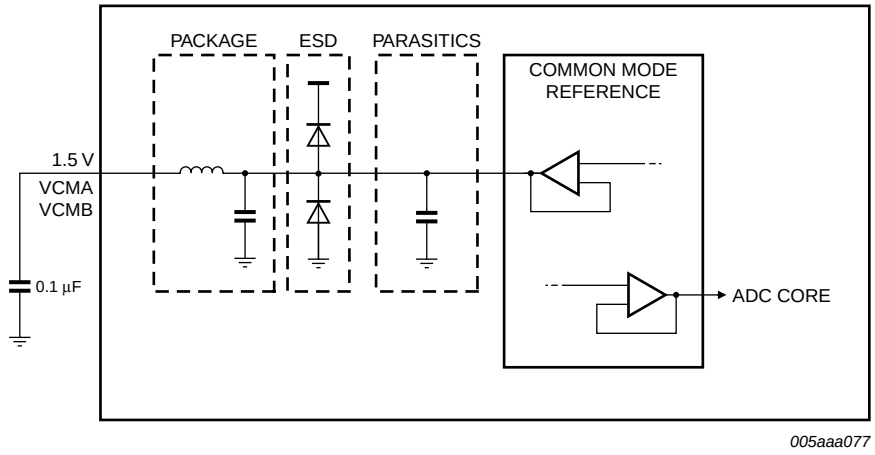



**Fig 15. Reference equivalent schematic**

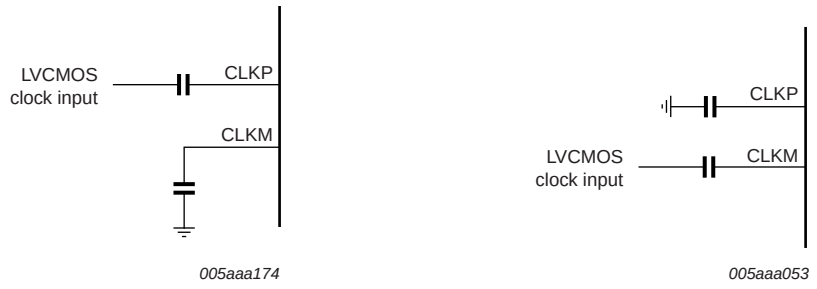
### 11.2.4 Biasing

The common-mode input voltage, $V_{I(cm)}$, at the inputs to the sample-and-hold stage (pins INAM, INBM, INAP, and INBP) must be between 0.9 V and 2 V for optimal performance.

## 11.3 Clock input

### 11.3.1 Drive modes

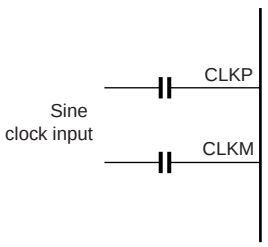
The ADC1413D can be driven differentially (LVPECL). It can also be driven by a single-ended Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or pin CLKM (pin CLKP should be connected to ground via a capacitor).



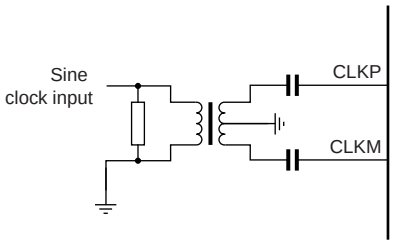

a. Rising edge LVCMOS

b. Falling edge LVCMOS

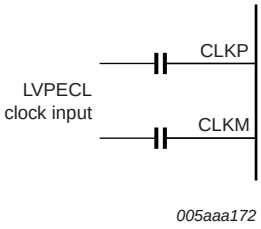
**Fig 16. LVCMOS single-ended clock input**




a. Sine clock input




b. Sine clock input (with transformer)

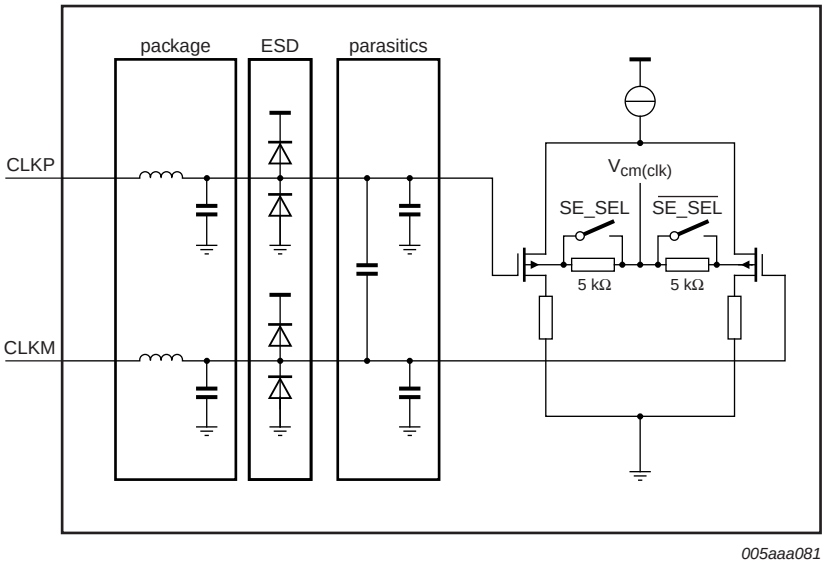



c. LVPECL clock input

**Fig 17. Differential clock input**

### 11.3.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 18. The common-mode voltage of the differential input stage is set via 5 kΩ internal resistors.




$V_{cm(clk)}$ = common-mode voltage of the differential input stage.

**Fig 18. Equivalent input circuit**

Single-ended or differential clock inputs can be selected via the SPI (see Table 20). If single-ended is selected, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting bit SE_SEL accordingly, the unused pin should be connected to ground via a capacitor.

### 11.3.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performance of the ADC by compensating the input clock signal duty cycle. When the duty cycle stabilizer is active (bit DCS_EN = logic 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

**Table 12. Duty cycle stabilizer**

| Bit DCS_EN | Description |
|---|---|
| 0 | duty cycle stabilizer disable |
| 1 | duty cycle stabilizer enable |

### 11.3.4 Clock input divider

The ADC1413D contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV2_SEL = logic 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

## 11.4 Digital outputs

### 11.4.1 Serial output equivalent circuit

The JESD204A standard specifies that if the receiver and the transmitter are DC-coupled, both must be fed from the same supply.

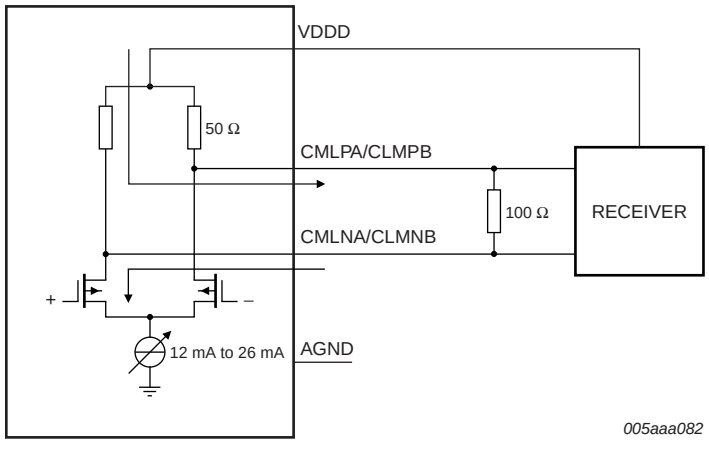



**Fig 19. CML output connection to the receiver (DC-coupled)**

The output should be terminated when 100 Ω (typical) is reached at the receiver side.

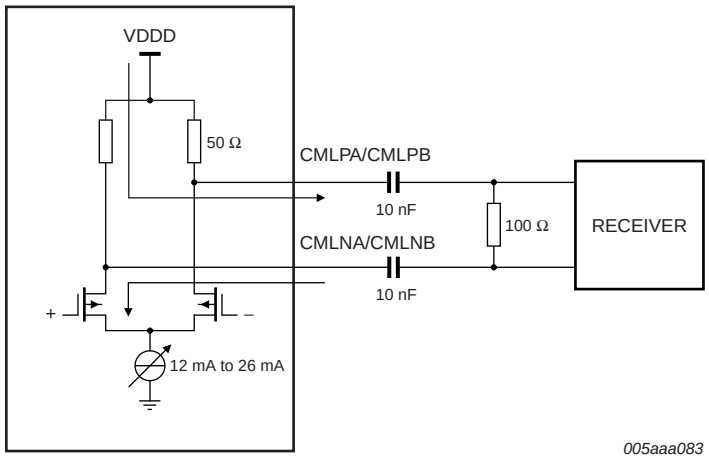



**Fig 20. CML output connection to the receiver (AC-coupled)**

## 11.5 JESD204A serializer

For more information about the JESD204A standard refer to the JEDEC web site.

### 11.5.1 Digital JESD204A formatter

The block placed after the ADC cores is used to implement all functionalities of the JESD204A standard. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly parameterized and can be configured in various ways depending on the sampling frequency and the number of lanes used.

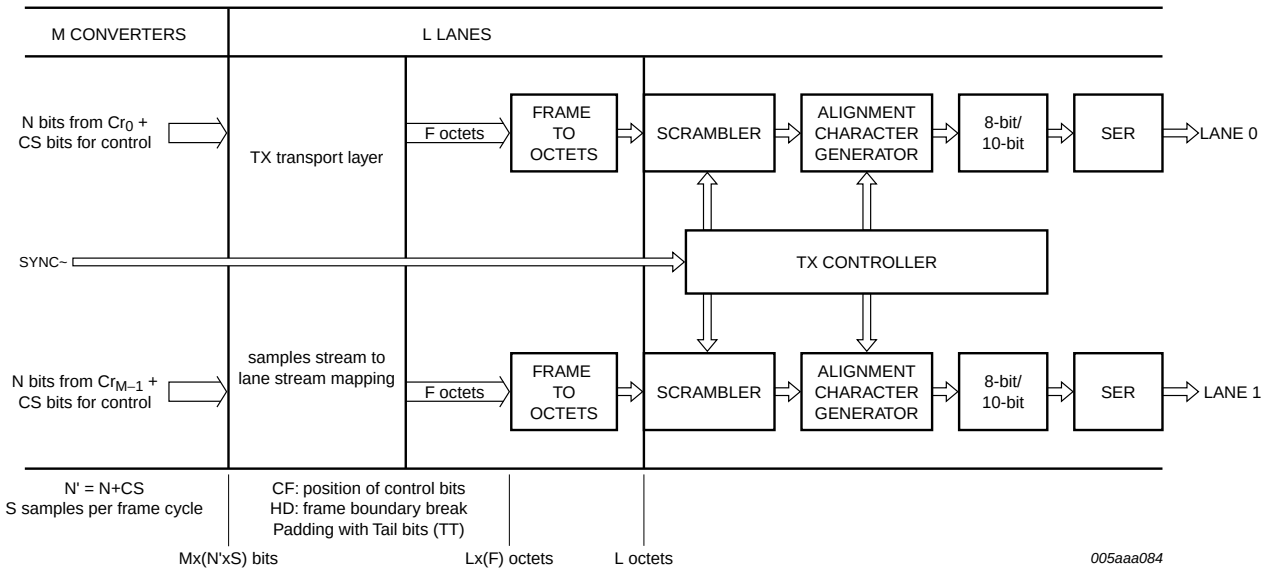



**Fig 21. General overview of the JESD204A serializer**

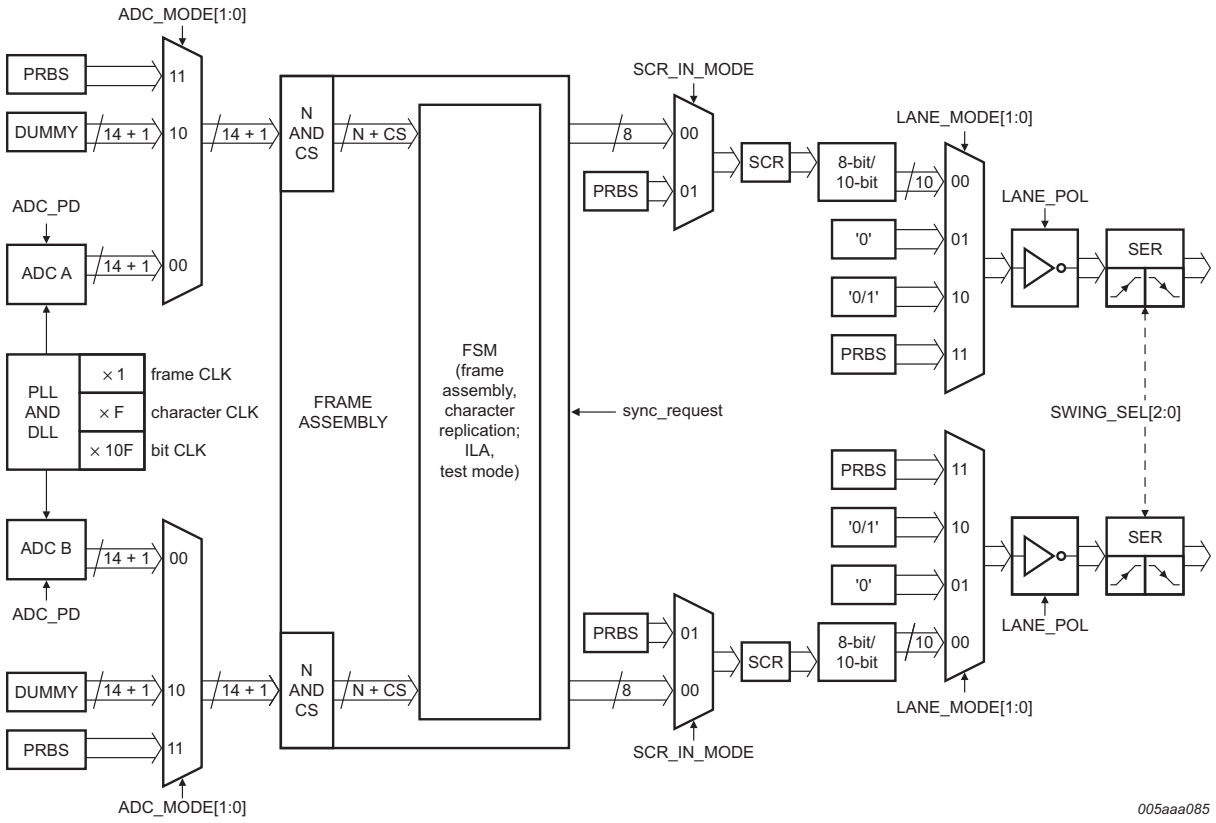



Fig 22. Detailed view of the JESD204A serializer with debug functionality

### 11.5.2 ADC core output codes versus input voltage

Table 13 shows the data output codes for a given analog input voltage.

Table 13. Output codes versus input voltage

| INP − INM (V) | Offset binary | Two's complement | OTR |
|---|---|---|---|
| < −1 | 00 0000 0000 0000 | 10 0000 0000 0000 | 1 |
| −1 | 00 0000 0000 0000 | 10 0000 0000 0000 | 0 |
| −0.9998779 | 00 0000 0000 0001 | 10 0000 0000 0001 | 0 |
| −0.9997559 | 00 0000 0000 0010 | 10 0000 0000 0010 | 0 |
| −0.9996338 | 00 0000 0000 0011 | 10 0000 0000 0011 | 0 |
| −0.9995117 | 00 0000 0000 0100 | 10 0000 0000 0100 | 0 |
| .... | .... | .... | 0 |
| −0.0002441 | 01 1111 1111 1110 | 11 1111 1111 1110 | 0 |
| −0.0001221 | 01 1111 1111 1111 | 11 1111 1111 1111 | 0 |
| 0 | 10 0000 0000 0000 | 00 0000 0000 0000 | 0 |
| +0.0001221 | 10 0000 0000 0001 | 00 0000 0000 0001 | 0 |
| +0.0002441 | 10 0000 0000 0010 | 00 0000 0000 0010 | 0 |
| .... | .... | .... | 0 |
| +0.9995117 | 11 1111 1111 1011 | 01 1111 1111 1011 | 0 |

**Table 13. Output codes versus input voltage** *...continued*

| INP – INM (V) | Offset binary | Two's complement | OTR |
|---|---|---|---|
| +0.9996338 | 11 1111 1111 1100 | 01 1111 1111 1100 | 0 |
| +0.9997559 | 11 1111 1111 1101 | 01 1111 1111 1101 | 0 |
| +0.9998779 | 11 1111 1111 1110 | 01 1111 1111 1110 | 0 |
| +1 | 11 1111 1111 1111 | 01 1111 1111 1111 | 0 |
| > +1 | 11 1111 1111 1111 | 01 1111 1111 1111 | 1 |

## 11.6 Serial Peripheral Interface (SPI)

### 11.6.1 Register description

The ADC1413D serial interface is a synchronous serial communications port allowing easy interfacing with many industry microprocessors. It provides access to the registers that control the operation of the chip in both read and write modes.

This interface is configured as a 3-wire type (SDIO as bidirectional pin).

SCLK acts as the serial clock, and pin $\overline{CS}$ acts as the serial chip select.

Each read/write operation is sequenced by the $\overline{CS}$ signal and enabled by a LOW level to to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte (see Table 14).

**Table 14. SPI instruction bytes**

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Description | R/W[1] | W1 | W0 | A12 | A11 | A10 | A9 | A8 |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

[1] R/W indicates whether a read (logic 1) or write (logic 0) transfer occurs after the instruction byte.

**Table 15. Read or Write mode access description**

| R/W[1] | Description |
|---|---|
| 0 | Write mode operation |
| 1 | Read mode operation |

[1] Bits W1 and W0 indicate the number of bytes transferred after the instruction byte.

**Table 16. Number of bytes to be transferred**

| W1 | W0 | Number of bytes transferred |
|---|---|---|
| 0 | 0 | 1 byte |
| 0 | 1 | 2 bytes |
| 1 | 0 | 3 bytes |
| 1 | 1 | 4 or more bytes |

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is incremented to access subsequent addresses.

The steps for a data transfer:

1. The falling edge on pin $\overline{CS}$ in combination with a rising edge on pin SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but is always a multiple of 8 bits. The Most Significant Bit (MSB) is always sent first (for instruction and data bytes).
4. A rising edge on pin $\overline{CS}$ indicates the end of data transmission.

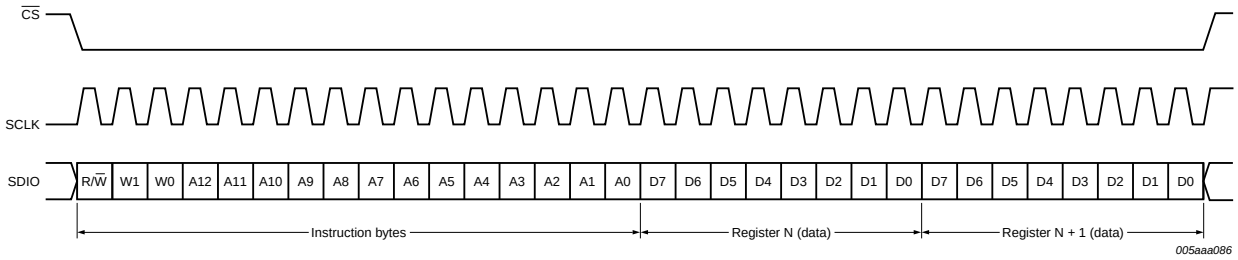



**Fig 23. Transfer diagram for two data bytes (3-wire type)**

### 11.6.2 Channel control

The two ADC channels can be configured at the same time or separately. By using the register “Channel index”, the user can choose which ADC channel receives the next SPI-instruction. By default the channel A and B receives the same instructions in write mode. In read mode only A is active.

**Table 17. Register allocation map**

| Address (hex) | Register name | Access[1] | Bit definition | | | | | | | | Default (bin) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| **ADC control register** | | | | | | | | | | | |
| 0003 | Channel index | R/W | - | - | - | - | - | - | ADCB | ADCA | 1111 1111 |
| 0005 | Reset and Power-down modes | R/W | SW_RST | - | - | - | - | - | PD[1:0] | | 0000 0000 |
| 0006 | Clock | R/W | - | - | - | SE_SEL | DIFF_SE | - | CLKDIV2_SEL | DCS_EN | 0000 0001 |
| 0008 | Vref | R/W | - | - | - | - | INTREF_EN | INTREF[2:0] | | | 0000 0000 |
| 0013 | Offset | R/W | - | - | DIG_OFFSET[5:0] | | | | | | 0000 0000 |
| 0014 | Test pattern 1 | R/W | - | - | - | - | - | TESTPAT_1[2:0] | | | 0000 0000 |
| 0015 | Test pattern 2 | R/W | TESTPAT_2[13:6] | | | | | | | | 0000 0000 |
| 0016 | Test pattern 3 | R/W | TESTPAT_3[5:0] | | | | | | - | - | 0000 0000 |
| **JESD204A control** | | | | | | | | | | | |
| 0801 | Ser_Status | R | RXSYNC_ERROR | RESERVED[2:0] | | | 0 | 0 | POR_TST | RESERVED | 0100 0000 |
| 0802 | Ser_Reset | R/W | SW_RST | 0 | 0 | 0 | FSM_SW_RST | 0 | 0 | 0 | 0000 0000 |
| 0803 | Ser_Cfg_Setup | R/W | 0 | 0 | 0 | 0 | CFG_SETUP[3:0] | | | | 0000 1000 |
| 0805 | Ser_Control1 | R/W | 0 | TRISTATE_CFG_PINS | SYNC_POL | SYNC_SINGLE_ENDED | 1 | REV_SCR | REV_ENCODER | REV_SERIAL | 0100 1001 |
| 0806 | Ser_Control2 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | SWAP_LANE_1_2 | SWAP_ADC_0_1 | 0000 0011 |
| 0808 | Ser_Analog_Ctrl | R/W | 0 | 0 | 0 | 0 | 0 | SWING_SEL[2:0] | | | 0000 0011 |
| 0809 | Ser_ScramblerA | R/W | 0 | LSB_INIT[6:0] | | | | | | | 0000 0000 |
| 080A | Ser_ScramblerB | R/W | MSB_INIT[7:0] | | | | | | | | 1111 1111 |
| 080B | Ser_PRBS_Ctrl | R/W | 0 | 0 | 0 | 0 | 0 | 0 | PRBS_TYPE[1:0] | | 0000 0000 |
| 0820 | Cfg_0_DID | R* | DID[7:0] | | | | | | | | 1110 1101 |
| 0821 | Cfg_1_BID | R/W* | 0 | 0 | 0 | 0 | BID[3:0] | | | | 0000 1010 |
| 0822 | Cfg_3_SCR_L | R/W* | SCR | 0 | 0 | 0 | 0 | 0 | 0 | L | 0000 0000 |
| 0823 | Cfg_4_F | R/W* | 0 | 0 | 0 | 0 | 0 | F[2:0] | | | 0000 0001 |
| 0824 | Cfg_5_K | R/W* | 0 | 0 | 0 | K[4:0] | | | | | 0000 1000 |
| 0825 | Cfg_6_M | R/W* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M | 0000 0000 |

**Table 17. Register allocation map** *...continued*

| Address (hex) | Register name | Access[1] | Bit definition | | | | | | | | Default (bin) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0826 | Cfg_7_CS_N | R/W* | 0 | CS[0] | 0 | 0 | N[3:0] | | | | 0100 0100 |
| 0827 | Cfg_8_Np | R/W | 0 | 0 | 0 | NP[4:0] | | | | | 0000 1111 |
| 0828 | Cfg_9_S | R/W* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | S | 0000 0000 |
| 0829 | Cfg_10_HD_CF | R/W* | HD | 0 | 0 | 0 | 0 | 0 | CF[1:0] | | 0000 0000 |
| 082C | Cfg_01_2_LID | R/W* | 0 | 0 | 0 | LID[4:0] | | | | | 0001 1011 |
| 082D | Cfg_02_2_LID | R/W* | 0 | 0 | 0 | LID[4:0] | | | | | 0001 1100 |
| 084C | Cfg01_13_FCHK | R | FCHK[7:0] | | | | | | | | 0000 0000 |
| 084D | Cfg02_13_FCHK | R | FCHK[7:0] | | | | | | | | 0000 0000 |
| 0870 | Lane0_0_Ctrl | R/W | 0 | SCR_IN_MODE | LANE_MODE[1:0] | | 0 | LANE_POL | LANE_CLK_POS_EDGE | LANE_PD | 0000 0001 |
| 0871 | Lane1_0_Ctrl | R/W | 0 | SCR_IN_MODE | LANE_MODE[1:0] | | 0 | LANE_POL | LANE_CLK_POS_EDGE | LANE_PD | 0000 0000 |
| 0890 | ADCA_0_Ctrl | R/W | 0 | 0 | ADC_MODE[1:0] | | 0 | 0 | 0 | ADC_PD | 0000 0001 |
| 0891 | ADCB_0_Ctrl | R/W | 0 | 0 | ADC_MODE[1:0] | | 0 | 0 | 0 | ADC_PD | 0000 0000 |

[1] an "*" in the Access column means that this register is subject to control access conditions in Write mode.

### 11.6.3 Register description

#### 11.6.3.1 ADC control registers

**Table 18. Register Channel index (address 0003h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 2 | - | - | 111111 | not used |
| 1 | ADCB | R/W | | ADC B gets the next SPI command: |
| | | | 0 | ADC B not selected |
| | | | **1** | **ADC B selected** |
| 0 | ADCA | R/W | | ADC A gets the next SPI command: |
| | | | 0 | ADC A not selected |
| | | | **1** | **ADC A selected** |

**Table 19. Register Reset and Power-down mode (address 0005h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | SW_RST | R/W | | reset digital part: |
| | | | **0** | **no reset** |
| | | | 1 | performs a reset of the digital part |
| 6 to 2 | - | - | 00000 | not used |
| 1 to 0 | PD[1:0] | R/W | | Power-down mode: |
| | | | **00** | **normal (power-up)** |
| | | | 01 | full power-down |
| | | | 10 | sleep |
| | | | 11 | normal (power-up) |

**Table 20. Register Clock (address 0006h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | - | 000 | not used |
| 4 | SE_SEL | R/W | | select SE clock input pin: |
| | | | **0** | **select CLKM input** |
| | | | 1 | select CLKP input |
| 3 | DIFF_SE | R/W | | differential/single-ended clock input select: |
| | | | **0** | **fully differential** |
| | | | 1 | single-ended |
| 2 | - | - | 0 | not used |
| 1 | CLKDIV2_SEL | R/W | | select clock input divider by 2: |
| | | | **0** | **disable** |
| | | | 1 | active |
| 0 | DCS_EN | R/W | | duty cycle stabilizer enable: |
| | | | 0 | disable |
| | | | **1** | **active** |

**Table 21. Register Vref (address 0008h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | - | 0000 | not used |
| 3 | INTREF_EN | R/W | | enable internal programmable VREF mode: |
| | | | **0** | **disable** |
| | | | 1 | active |
| 2 to 0 | INTREF[2:0] | R/W | | programmable internal reference: |
| | | | **000** | **0 dB (FS=2 V)** |
| | | | 001 | −1 dB (FS=1.78 V) |
| | | | 010 | −2 dB (FS=1.59 V) |
| | | | 011 | −3 dB (FS=1.42 V) |
| | | | 100 | −4 dB (FS=1.26 V) |
| | | | 101 | −5 dB (FS=1.12 V) |
| | | | 110 | −6 dB (FS=1 V) |
| | | | 111 | not used |

**Table 22. Digital Offset adjustment (address 0013h)**
*Default values are highlighted.*

| Register Offset | | |
|---|---|---|
| **Decimal** | **DIG_OFFSET[5:0]** | |
| +31 | 011111 | +31 LSB |
| ... | ... | ... |
| 0 | **000000** | 0 |
| ... | ... | ... |
| −32 | 100000 | −32 LSB |

**Table 23. Register Test pattern 1 (address 0014h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 3 | - | - | 00000 | not used |
| 2 to 0 | TESTPAT_1[2:0] | R/W | | digital test pattern: |
| | | | **000** | **off** |
| | | | 001 | mid-scale |
| | | | 010 | − FS |
| | | | 011 | + FS |
| | | | 100 | toggle ‘1111..1111’/’0000..0000’ |
| | | | 101 | custom test pattern, to be written in register 0015h and 0016h |
| | | | 110 | ‘010101...’ |
| | | | 111 | ‘101010...’ |

**Table 24. Register Test pattern 2 (address 0015h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | TESTPAT_2[13:6] | R/W | **00000000** | **custom digital test pattern (bit 13 to 6)** |

**Table 25. Register Test pattern 3 (address 0016h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 2 | TESTPAT_3[5:0] | R/W | **000000** | **custom digital test pattern (bit 5 to 0)** |
| 1 to 0 | - | - | 00 | not used |

### 11.6.4 JESD204A digital control registers

**Table 26. Ser_Status (address 0801h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | RXSYNC_ERROR | R | 0 | set to 1 when a synchronization error occurs |
| 6 to 4 | RESERVED[2:0] | - | **100** | **reserved** |
| 3 to 2 | - | - | 00 | not used |
| 1 | POR_TST | R | **0** | **power-on-reset** |
| 0 | RESERVED | - | 0 | reserved |

**Table 27. Ser_Reset (address 0802h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | SW_RST | R/W | **0** | **initiates a software reset of the JESD204A unit** |
| 6 to 4 | - | - | 000 | not used |
| 3 | FSM_SW_RST | R/W | **0** | **initiates a software reset of the internal state machine of JESD204A unit** |
| 2 to 0 | - | - | 000 | not used |

**Table 28. Ser_Cfg_Setup (address 0803h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | - | 0000 | not used |
| 3 to 0 | CFG_SETUP[3:0] | R/W | | quick configuration of JESD204A. These settings overrule the configuration of pins CFG3 to CFG0 (see Table 29). |

**Table 29. JESD204A configuration table**

| CFG_SETUP[3:0] | | ADC A | ADC B | Lane 0 | Lane 1 | F[1] | HD[1] | K[1] | M[1] | L[1] | Comment | CS[1] | CF[1] | S[1] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0000 | **ON** | **ON** | **ON** | **ON** | 2 | 0 | 9 | 2 | 2 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 1 | 0001 | **ON** | **ON** | **ON** | OFF | 4 | 0 | 5 | 2 | 1 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 2 | 0010 | **ON** | **ON** | OFF | **ON** | 4 | 0 | 5 | 2 | 1 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 3 | 0011 | **ON** | OFF | **ON** | **ON** | 1 | 1 | 17 | 1 | 2 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 4 | 0100 | OFF | **ON** | **ON** | **ON** | 1 | 1 | 17 | 1 | 2 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 5 | 0101 | **ON** | OFF | **ON** | OFF | 2 | 0 | 9 | 1 | 1 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 6 | 0110 | **ON** | OFF | OFF | **ON** | 2 | 0 | 9 | 1 | 1 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 7 | 0111 | OFF | **ON** | **ON** | OFF | 2 | 0 | 9 | 1 | 1 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 8 | 1000 | OFF | **ON** | OFF | **ON** | 2 | 0 | 9 | 1 | 1 | (F × K) ≥ 17 | 1 | 0 | 1 |
| 9 | 1001 | reserved | | | | | | | | | | | | |
| 10 | 1010 | reserved | | | | | | | | | | | | |
| 11 | 1011 | reserved | | | | | | | | | | | | |
| 12 | 1100 | reserved | | | | | | | | | | | | |
| 13 | 1101 | reserved | | | | | | | | | | | | |
| 14 | 1110 | **ON** | **ON** | **ON** | **ON** | 2 | 0 | 9 | 2 | 2 | test: loop alignment | 1 | 0 | 1 |
| 15 | 1111 | OFF | OFF | OFF | OFF | 2 | 0 | 9 | 2 | 2 | chip power-down | 1 | 0 | 1 |

[1] F: Octets per frame clock cycle
HD: High-density mode
K: Frame per multi-frame
M: Converters per device
L: Lane per converter device
CS: Number of control bits per conversion sample
CF: Control words per frame clock cycle and link
S: Number of samples transmitted per single converter per frame cycle

**Table 30. Ser_Control1 (address 0805h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | - | - | 0 | not used |
| 6 | TRISTATE_CFG_PINS | R/W | **1** | **pins CFG3 to CFG0 are set to high-impedance. Switch to 0 automatically after start-up or reset.** |
| 5 | SYNC_POL | R/W | | defines the sync signal polarity: |
| | | | **0** | **synchronization signal is active LOW** |
| | | | 1 | synchronization signal is active HIGH |
| 4 | SYNC_SINGLE_ENDED | R/W | | defines the input mode of the sync signal: |
| | | | **0** | **synchronization input mode is set in Differential mode** |
| | | | 1 | synchronization input mode is set in Single-ended mode |
| 3 | - | - | 1 | not used |
| 2 | REV_SCR | - | | LSBs are swapped with MSBs at the scrambler input: |
| | | | **0** | disable |
| | | | 1 | enable |
| 1 | REV_ENCODER | - | | LSBs are swapped with MSBs at the 8-bit/10-bit encoder input: |
| | | | **0** | disable |
| | | | 1 | enable |
| 0 | REV_SERIAL | - | | LSBs are swapped with MSBs at the lane input: |
| | | | 0 | disable |
| | | | **1** | **enable** |

**Table 31. Ser_Control2 (address 0806h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 2 | - | - | 000000 | not used |
| 1 | SWAP_LANE_0_1 | R/W | | swaps the outputs of the JESD204A unit. (output buffer A is connected to Lane 1, output buffer B is connected to Lane 0): |
| | | | 0 | disable |
| | | | **1** | **enable** |
| 0 | SWAP_ADC_A_B | R/W | | swaps the inputs of the JESD204A unit. (ADC A output is connected to input B, ADC B is connected to input A): |
| | | | 0 | disable |
| | | | **1** | **enable** |

**Table 32. Ser_Analog_Ctrl (address 0808h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 3 | - | - | 00000 | not used |
| 2 to 0 | SWING_SEL[2:0] | R/W | **011** | **defines the swing output for the lane pads** |

**Table 33. Ser_ScramblerA (address 0809h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | - | - | 0 | not used |
| 6 to 0 | LSB_INIT[6:0] | R/W | **0000000** | **defines the initialization vector for the scrambler polynomial (lower)** |

**Table 34. Ser_ScramblerB (address 080Ah)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | MSB_INIT[7:0] | R/W | **11111111** | **defines the initialization vector for the scrambler polynomial (upper)** |

**Table 35. Ser_PRBS_Ctrl (address 080Bh)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 2 | - | - | 000000 | not used |
| 1 to 0 | PRBS_TYPE[1:0] | R/W | | defines the type of Pseudo-Random Binary Sequence (PRBS) generator to be used: |
| | | | **00** (reset) | **PRBS-7** |
| | | | 01 | PRBS-7 |
| | | | 10 | PRBS-23 |
| | | | 11 | PRBS-31 |

**Table 36. Cfg_0_DID (address 0820h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | DID[7:0] | R | **11101101** | **defines the device (= link) identification number** |

**Table 37. Cfg_1_BID (address 0821h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 4 | - | - | 0000 | not used |
| 3 to 0 | BID[3:0] | R/W | **1010** | **defines the bank ID – extension to DID** |

**Table 38. Cfg_3_SCR_L (address 0822h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | SCR | R/W | 0 | scrambling enabled |
| 6 to 1 | - | - | 000000 | not used |
| 0 | L | R/W | 0 | defines the number of lanes per converter device, minus 1 |

**Table 39. Cfg_4_F (address 0823h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 3 | - | - | 00000 | not used |
| 2 to 0 | F[2:0] | R/W | 001 | defines the number of octets per frame, minus 1 |

**Table 40. Cfg_5_K (address 0824h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | K[4:0] | R/W | 01000 | defines the number of frames per multiframe, minus 1 |

**Table 41. Cfg_6_M (address 0825h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 1 | - | - | 0000000 | not used |
| 0 | M | R/W | 0 | defines the number of converters per device, minus 1 |

**Table 42. Cfg_7_CS_N (address 0826h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | - | - | 0 | not used |
| 6 | CS[0] | R/W | 1 | defines the number of control bits per sample, minus 1 |
| 5 to 4 | - | R | 00 | not used |
| 3 to 0 | N[3:0] | R/W | 0100 | defines the converter resolution |

**Table 43. Cfg_8_Np (address 0827h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | NP[4:0] | R/W | 01111 | defines the total number of bits per sample, minus 1 |

**Table 44. Cfg_9_S (address 0828h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 1 | - | - | 0000000 | not used |
| 0 | S | R/W | **0** | **defines number of samples per converter per frame cycle** |

**Table 45. Cfg_10_HD_CF (address 0829h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | HD | R/W | 0 | defines high density format |
| 6 to 2 | - | - | 00000 | not used |
| 1 to 0 | CF[1:0] | R/W | 00 | defines number of control words per frame clock cycle per link. |

**Table 46. Cfg_01_2_LID (address 082Ch)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | LID[4:0] | R/W | **11011** | **defines lane 0 identification number** |

**Table 47. Cfg_02_2_LID (address 082Dh)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 5 | - | - | 000 | not used |
| 4 to 0 | LID[4:0] | R/W | **11100** | **defines lane 1 identification number** |

**Table 48. Cfg01_13_FCHK (address 084Ch)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | FCHK[7:0] | R | 00000000 | defines the checksum value for lane 0<br>checksum corresponds to the sum of all the link configuration parameters modulo 256 (as defined in JEDEC Standard No.204A) |

**Table 49. Cfg02_13_FCHK (address 084Dh)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 0 | FCHK[7:0] | R | 00000000 | defines the checksum value for lane 1<br>checksum corresponds to the sum of all the link configuration parameters module 256 (as defined in JEDEC Standard No.204A) |

**Table 50. Lane0_0_Ctrl (address 0870h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | - | - | 0 | not used |
| 6 | SCR_IN_MODE | R/W | | defines the input type for scrambler and 8-bit/10-bit units: |
| | | | **0** (reset) | **(normal mode) = input of the scrambler and 8-bit/10-bit units is the output of the frame assembly unit.** |
| | | | 1 | input of the scrambler and 8-bit/10-bit units is the PRBS generator (PRBS type is defined with “PRBS_TYPE[1:0]” (Ser_PRBS_Ctrl register) |
| 5 to 4 | LANE_MODE[1:0] | R/W | | defines output type of lane output unit: |
| | | | **00** (reset) | **normal mode: lane output is the 8-bit/10-bit output unit** |
| | | | 01 | constant mode: lane output is set to a constant ($0 \times 0$) |
| | | | 10 | toggle mode: lane output is toggling between $0 \times 0$ and $0 \times 1$ |
| | | | 11 | PRBS mode: lane output is the PRBS generator (PRBS type is defined with “PRBS_TYPE[1:0]” (Ser_PRBS_Ctrl register) |
| 3 | - | - | 0 | not used |
| 2 | LANE_POL | R/W | | defines lane polarity: |
| | | | **0** | **lane polarity is normal** |
| | | | 1 | lane polarity is inverted |
| 1 | LANE_CLK_POS_EDGE | R/W | | defines lane clock polarity: |
| | | | **0** | **lane clock provided to the serializer is active on positive edge** |
| | | | 1 | lane clock provided to the serializer is active on negative edge |

**Table 50. Lane0_0_Ctrl (address 0870h)** *…continued*

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 0 | LANE_PD | R/W | | lane power-down control: |
| | | | 0 | lane is operational |
| | | | **1** | **lane is in Power-down mode** |

**Table 51. Lane1_0_Ctrl (address 0871h)**

*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | - | - | 0 | not used |
| 6 | SCR_IN_MODE | R/W | | defines the input type for scrambler and 8-bit/10-bit units: |
| | | | **0** (reset) | **(normal mode) = input of the scrambler and 8-bit/10-bit units is the output of the frame assembly unit.** |
| | | | 1 | input of the scrambler and 8-bit/10-bit units is the PRBS generator (PRBS type is defined with “PRBS_TYPE[1:0]” (Ser_PRBS_Ctrl register) |
| 5 to 4 | LANE_MODE[1:0] | R/W | | defines output type of lane output unit: |
| | | | **00** (reset) | **normal mode: lane output is the 8-bit/10-bit output unit** |
| | | | 01 | constant mode: lane output is set to a constant (0x0) |
| | | | 10 | toggle mode: lane output is toggling between 0x0 and 0x1 |
| | | | 11 | PRBS mode: lane output is the PRSB generator (PRBS type is defined with “PRBS_TYPE[1:0]” (Ser_PRBS_Ctrl register) |
| 3 | - | - | 0 | not used |
| 2 | LANE_POL | R/W | | defines lane polarity: |
| | | | **0** | **lane polarity is normal** |
| | | | 1 | lane polarity is inverted |
| 1 | LANE_CLK_POS_EDGE | R/W | | defines lane clock polarity: |
| | | | **0** | **lane clock provided to the serializer is active on positive edge** |
| | | | 1 | lane clock provided to the serializer is active on negative edge |
| 0 | LANE_PD | R/W | | lane power-down control: |
| | | | **0** | **lane is operational** |
| | | | 1 | lane is in Power-down mode |

**Table 52. ADCA_0_Ctrl (address 0890h)**
*Default values are highlighted.*

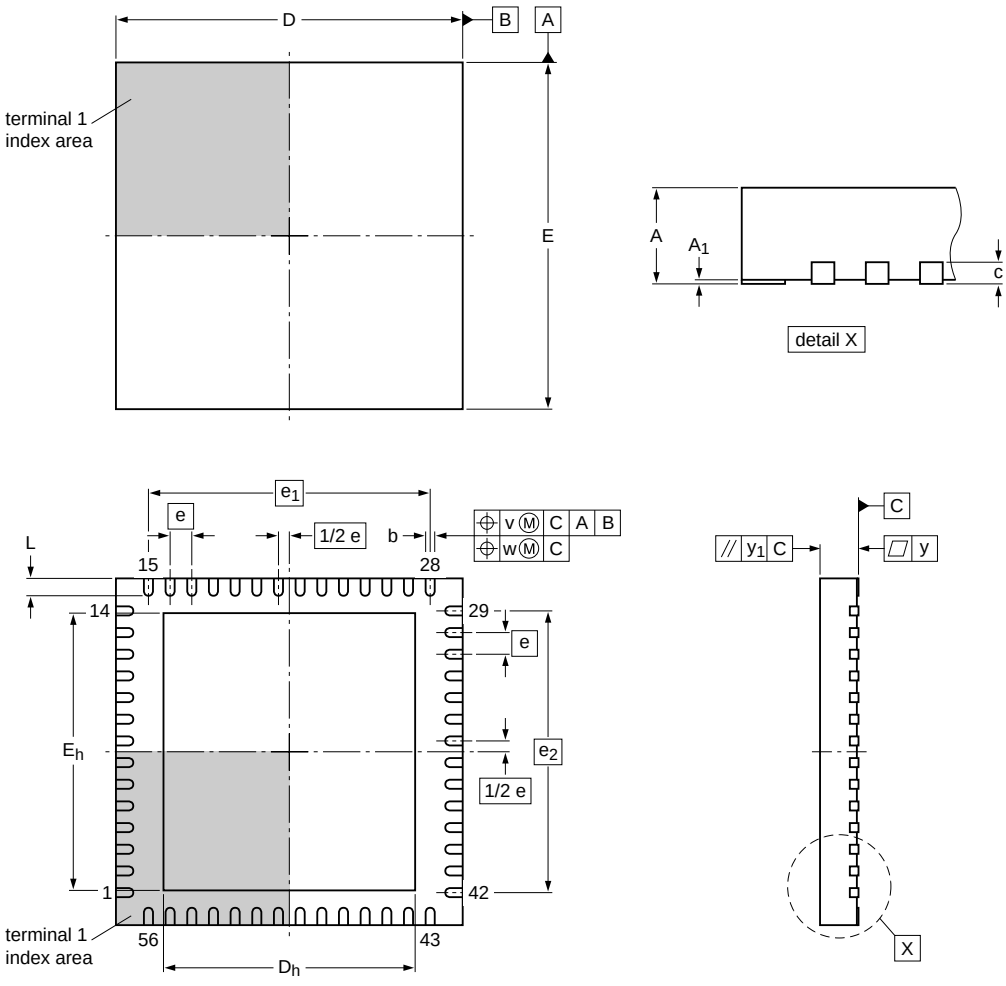
| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 6 | - | - | 00 | not used |
| 5 to 4 | ADC_MODE[1:0] | R/W | | defines input type of JESD204A unit: |
| | | | **00** (reset) | **ADC output is connected to the JESD204A input** |
| | | | 01 | not used |
| | | | 10 | JESD204A input is fed with a dummy constant, set to: OTR = 0 and ADC[13:0] = “10011011101010” |
| | | | 11 | JESD204A is fed with a PRBS generator (PRBS type is defined with “PRBS_TYPE[1:0]” (Ser_PRBS_Ctrl register) |
| 3 to 1 | - | - | 000 | not used |
| 0 | ADC_PD | R/W | | ADC power-down control: |
| | | | 0 | ADC is operational |
| | | | **1** | **ADC is in Power-down mode** |

**Table 53. ADCB_0_Ctrl (address 0891h)**
*Default values are highlighted.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 to 6 | - | - | 00 | not used |
| 5 to 4 | ADC_MODE[1:0] | R/W | | defines input type of JESD204A unit |
| | | | **00** (reset) | **ADC output is connected to the JESD204A input** |
| | | | 01 | not used |
| | | | 10 | JESD204A input is fed with a dummy constant, set to: OTR = 0 and ADC[13:0] = “10011011101010” |
| | | | 11 | JESD204A is fed with a PRBS generator (PRBS type is defined with “PRBS_TYPE[1:0]” (Ser_PRBS_Ctrl register) |
| 3 to 1 | - | - | 000 | not used |
| 0 | ADC_PD | R/W | | ADC power-down control: |
| | | | **0** | **ADC is operational** |
| | | | 1 | ADC is in Power-down mode |

## 12. Package outline

**HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm** **SOT684-7**




Dimensions

| Unit | | A(1) | A1 | b | c | D(1) | Dh | E(1) | Eh | e | e1 | e2 | L | v | w | y | y1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.30 | | 8.1 | 5.95 | 8.1 | 6.55 | | | | 0.5 | | | | |
| mm | nom | 0.85 | 0.02 | 0.21 | 0.2 | 8.0 | 5.80 | 8.0 | 6.40 | 0.5 | 6.5 | 6.5 | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.18 | | 7.9 | 5.65 | 7.9 | 6.25 | | | | 0.3 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot684-7_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT684-7 | - - - | MO-220 | - - - | | | ~~08-11-19~~ 09-03-04 |

**Fig 24. Package outline SOT684-7 (HVQFN56)**

# 13. Abbreviations

**Table 54. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| DCS | Duty Cycle Stabilizer |
| ESD | ElectroStatic Discharge |
| IF | Intermediate Frequency |
| IMD | InterModulation Distortion |
| LSB | Least Significant Bit |
| LVCMOS | Low Voltage Complementary Metal Oxide Semiconductor |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic |
| MSB | Most Significant Bit |
| OTR | OuT-of-Range |
| PRBS | Pseudo-Random Binary Sequence |
| SFDR | Spurious-Free Dynamic Range |
| SNR | Signal-to-Noise Ratio |
| SPI | Serial Peripheral Interface |
| TX | Transmitter |

## 14. Revision history

**Table 55. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| ADC1413D_SER v.7 | 20120702 | Product data sheet | - | ADC1413D_SER v.6 |
| ADC1413D_SER v.6 | 20110608 | Product data sheet | - | ADC1413D_SER v.5 |
| Modifications: | • Section 10.2 “Clock and digital output timing” has been updated. | | | |
| ADC1413D_SER v.5 | 20110209 | Product data sheet | - | ADC1413D_SER v.4 |
| ADC1413D_SER v.4 | 20100423 | Preliminary data sheet | - | ADC1413D_SER v.3 |
| ADC1413D_SER v.3 | 20100412 | Objective data sheet | - | ADC1413D065_080_105_125_2 |
| ADC1413D065_080_105_125_2 | 20090604 | Objective data sheet | - | ADC1413D065_080_105_125_1 |
| ADC1413D065_080_105_125_1 | 20090528 | Objective data sheet | - | - |

## 15. Contact information

For more information or sales office addresses, please visit: http://www.idt.com

## 16. Contents


**1 General description . . . . . 1**
**2 Features and benefits . . . . . 1**
**3 Applications . . . . . 2**
**4 Ordering information . . . . . 2**
**5 Block diagram . . . . . 3**
**6 Pinning information . . . . . 4**
6.1 Pinning . . . . . 4
6.2 Pin description . . . . . 4
**7 Limiting values . . . . . 6**
**8 Thermal characteristics . . . . . 6**
**9 Static characteristics . . . . . 7**
**10 Dynamic characteristics . . . . . 10**
10.1 Dynamic characteristics . . . . . 10
10.2 Clock and digital output timing . . . . . 11
10.3 Serial output timing . . . . . 12
10.4 SPI timing . . . . . 13
**11 Application information . . . . . 14**
11.1 Analog inputs . . . . . 14
11.1.1 Input stage description . . . . . 14
11.1.2 Anti-kickback circuitry . . . . . 15
11.1.3 Transformer . . . . . 15
11.2 System reference and power management . . 16
11.2.1 Internal/external reference . . . . . 16
11.2.2 Programmable full-scale . . . . . 18
11.2.3 Common-mode output voltage ($V_{O(cm)}$) . . . . . 19
11.2.4 Biasing . . . . . 19
11.3 Clock input . . . . . 19
11.3.1 Drive modes . . . . . 19
11.3.2 Equivalent input circuit . . . . . 20
11.3.3 Duty cycle stabilizer . . . . . 21
11.3.4 Clock input divider . . . . . 21
11.4 Digital outputs . . . . . 21
11.4.1 Serial output equivalent circuit . . . . . 21
11.5 JESD204A serializer . . . . . 22
11.5.1 Digital JESD204A formatter . . . . . 22
11.5.2 ADC core output codes versus input voltage . 23
11.6 Serial Peripheral Interface (SPI) . . . . . 24
11.6.1 Register description . . . . . 24
11.6.2 Channel control . . . . . 25
11.6.3 Register description . . . . . 28
11.6.3.1 ADC control registers . . . . . 28
11.6.4 JESD204A digital control registers . . . . . 30
**12 Package outline . . . . . 38**
**13 Abbreviations . . . . . 39**
**14 Revision history . . . . . 40**
**15 Contact information . . . . . 40**
**16 Contents . . . . . 41**