TDA8941P

1.5 W mono Bridge Tied Load (BTL) audio amplifier

14 April 1999 **Preliminary specification**

1. Description

The TDA8941P is a single-channel audio power amplifier for an output power of 1.5 W at a 16 Ω load and a 9 V supply. The circuit contains a Bridge Tied Load (BTL) amplifier with an all-NPN output stage and standby/mute logic. The TDA8941P comes in an 8-pin dual in-line (DIP8) package.The TDA8941P is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

2. Features

- Few external components
- Fixed gain
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Printed-circuit board compatible, see Table 3 “Product family overview”.

3. Applications

- Mains fed applications (e.g. TV sound)
- PC audio
- Portable audio.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		6	9	18	V
I_q	quiescent supply current	V_{CC} = 9 V; R_L = ∞	-	14	20	mA
I_{stb}	standby supply current		-	-	10	µA

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Table 1: Quick reference data...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	THD = 10%; R_L = 16 Ω; V_{CC} = 9 V	1.2	1.5	-	W
THD	total harmonic distortion	P_o = 0.5 W	-	0.03	0.1	%
G_v	voltage gain		31	32	33	dB
SVRR	supply voltage ripple rejection		50	-	-	dB

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8941P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

5.1 Ordering options

Table 3: Product family overview

Type number	Package	Description
TDA8941P	DIP8	1.5 W mono Bridge Tied Load (BTL) audio amplifier
TDA8942P	DIP16	2 x 1.5 W stereo Bridge Tied Load (BTL) audio amplifier
TDA8943SF	SIL9MPF	7 W mono Bridge Tied Load (BTL) audio amplifier
TDA8944J	DBS17P	2 x 7 W stereo Bridge Tied Load (BTL) audio amplifier
TDA8945S	SIL9P	15 W mono Bridge Tied Load (BTL) audio amplifier
TDA8946J	DBS17P	2 x 15 W stereo Bridge Tied Load (BTL) audio amplifier

6. Block diagram

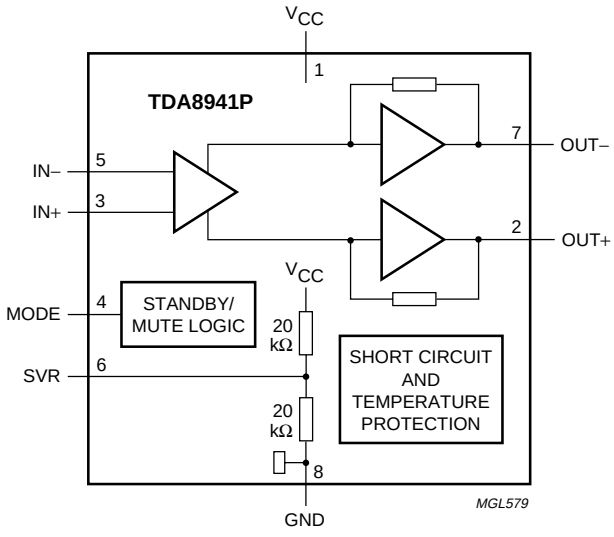


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

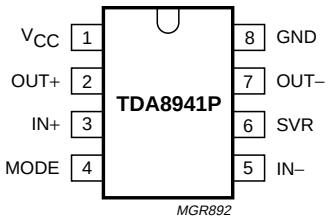


Fig 2. Pin configuration.

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
OUT+	2	positive loudspeaker terminal
IN+	3	positive input
MODE	4	mode selection input (standby, mute, operating)
IN–	5	negative input
SVR	6	half supply voltage decoupling (ripple rejection)
OUT–	7	negative loudspeaker terminal
GND	8	ground

8. Functional description

The TDA8941P is a mono BTL audio power amplifier capable of delivering 1.5 W output power to a 16 Ω load at THD = 10%, using a 9 V power supply. The voltage gain is fixed at 32 dB.

With the three-level MODE input the device can be switched from ‘standby’ to ‘mute’ and to ‘operating’ mode.

The TDA8941P outputs are protected by an internal thermal shutdown protection mechanism and a short-circuit protection.

8.1 Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with an all-NPN output stage, capable of delivering 1.5 A peak output current.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The ripple frequency on the supply voltage is twice the signal frequency

- No expensive DC-blocking capacitors
- Good low frequency performance.

8.2 Mode selection

The TDA8941P has three functional modes, which can be selected by applying the proper DC voltage to pin MODE.

Standby — In this mode the current consumption is very low and the outputs are floating. The device is in standby mode when $V_{MODE} > (V_{CC} - 0.5\ V)$, or when the MODE pin is left floating.

Mute — In this mode the amplifier is DC-biased but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when $2.5\ V < V_{MODE} < (V_{CC} - 1.5\ V)$.

Operating — In this mode the amplifier is operating normally. The operating mode is activated at $V_{MODE} < 0.5\ V$.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	operating		–0.3	+18	V
		no signal	[1]	–0.3	+25	V
V_I	input voltage			–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current			-	2	A
T_{stg}	storage temperature	non-operating		–55	+150	°C
T_{amb}	operating ambient temperature			–40	+85	°C
P_{tot}	total power dissipation			-	<tbf>	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection			-	<tbf>	V

[1] Applies to all functional modes.

10. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	100	K/W

11. Static characteristics

Table 7: Static characteristics

V_{CC} = 9 V; T_{amb} = 25 °C; R_L = 16 Ω; V_{MODE} = 0 V; V_i = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		6	9	18	V
I_q	quiescent supply current	R_L = ∞	[1]	-	14	20	mA
I_{stb}	standby supply current	V_{MODE} = V_{CC}		-	-	10	µA
V_O	DC output voltage		[2]	-	4.5	-	V
ΔV_{OUT} [3]	differential output voltage offset			-	-	200	mV
V_{MODE}	input voltage mode select	operating mode		0	-	0.5	V
		mute mode		2.5	-	V_{CC} – 1.5	V
		standby mode		V_{CC} – 0.5	-	V_{CC}	V
I_{MODE}	input current mode select	0 < V_{MODE} < V_{CC}		-	-	20	µA

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the differential output voltage offset (ΔV_{OUT}) divided by the load resistance (R_L).

[2] The DC output voltage with respect to ground is approximately 0.5V_{CC}.

[3] $\Delta V_{OUT} = | V_{OUT+} - V_{OUT-} |$.

12. Dynamic characteristics

Table 8: Dynamic characteristics

V_{CC} = 9 V; T_{amb} = 25 °C; R_L = 16 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10%		1.2	1.5	-	W
		THD = 0.5%		0.8	1	-	W
THD	total harmonic distortion	P_o = 0.5 W		-	0.03	0.1	%
G_v	voltage gain			31	32	33	dB
$Z_{i(dif)}$	differential input impedance			70	90	110	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	90	120	µV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	50	-	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	<tbf>	-	dB
$V_{o(mute)}$	output voltage	mute mode	[3]	-	-	50	µV

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input. The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, so including noise.

13. Application information

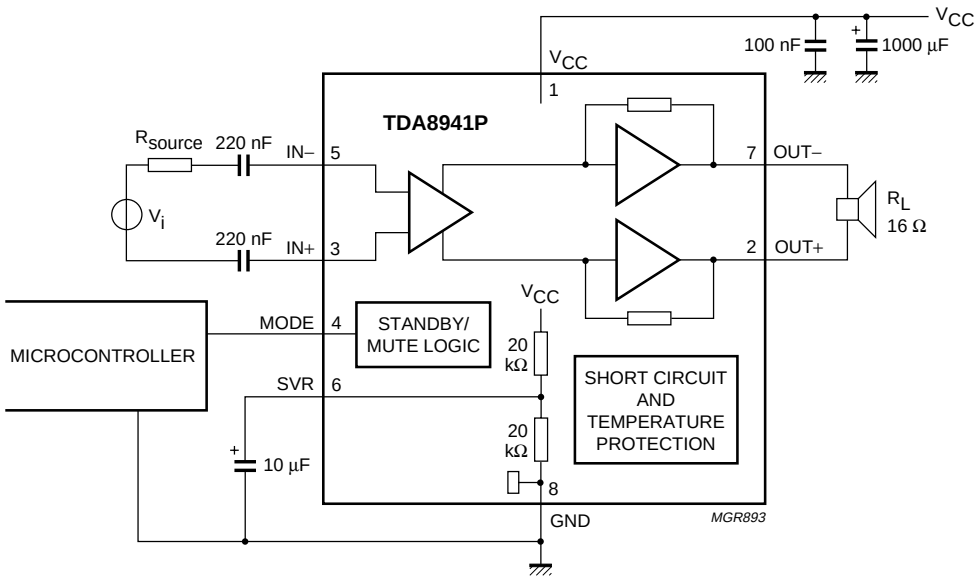


Fig 3. Application diagram.

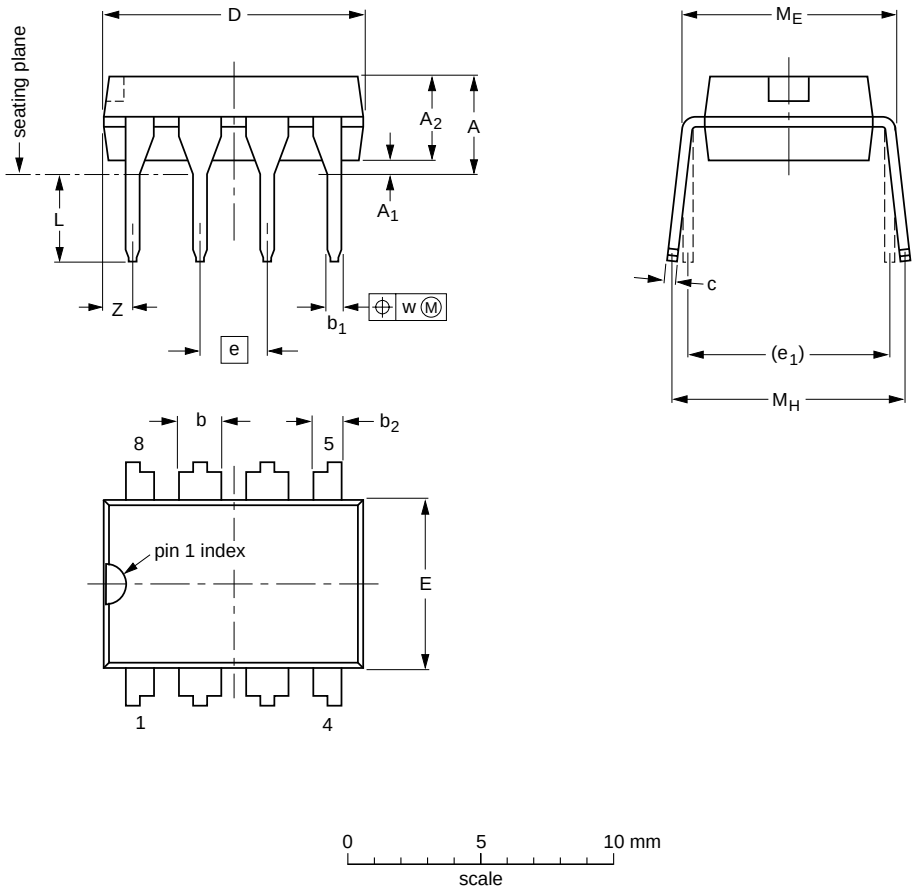
14. Test information

14.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611-part E* is applicable and reference can be found in the *Quality Reference Handbook, chapter Quality standards for customers*. The handbook can be ordered using the code 9397 750 00192.

15. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Fig 4. DIP8 package outline.

16. Soldering

16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

16.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.4 Package related soldering information

Table 9: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable [1]

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

17. Revision history

Rev	Date	CPCN	Description
01	990414	-	Preliminary specification; initial version.

18. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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