PCF8576C

Universal LCD driver for low multiplex rates

Rev. 09 — 9 July 2009 Product data sheet

1. General description

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing.

2. Features

- Single-chip LCD controller and driver
- 40 segment drives:
  - Up to twenty 7-segment numeric characters
  - Up to ten 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- Versatile blinking modes
- No external components required (even in multiple device applications)
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 40 $\times$ 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Wide logic LCD supply range:
  - From 2 V for low-threshold LCDs
  - Up to 6 V for guest-host LCDs and high-threshold twisted nematic LCDs
- Low power consumption
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with 24-segment LCD driver PCF8566
- No external components
- Compatible with chip-on-glass technology
- Separate or combined LCD and logic supplies
- Optimized pinning for plane wiring in both and multiple PCF8576C applications
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8576CH	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
PCF8576CT	VSO56	plastic very small outline package, 56 leads	SOT190-1
PCF8576CTT	HTSSOP56	plastic thermal enhanced thin shrink small outline package, 56 leads; body width 6.1 mm; exposed die pad	SOT793-1
PCF8576CU/10	PCF8576CU/10	wire bond die; 56 bonding pads; 3.0 × 2.82 × 0.38 mm[1]	PCF8576CU/10
PCF8576CU	PCF8576CU	wire bond die; 56 bonding pads; 3.0 × 2.82 × 0.38 mm[2]	PCF8576CU
PCF8576CU/2	PCF8576CU/2	bare die; 56 bumps; 3.0 × 2.82 × 0.40 mm[2]	PCF8576CU/2

[1] Delivery form: chip on FFC.

[2] Delivery form: chip in tray.

4. Marking

Table 2. Marking codes

Type number	Marking code
PCF8576CH	PCF8576CH
PCF8576CT	PCF8576CT
PCF8576CTT	PCF8576CTT
PCF8576CU/10	PC8576C-1
PCF8576CU	PC8576C-1
PCF8576CU/2	PC8576C-2

5. Block diagram

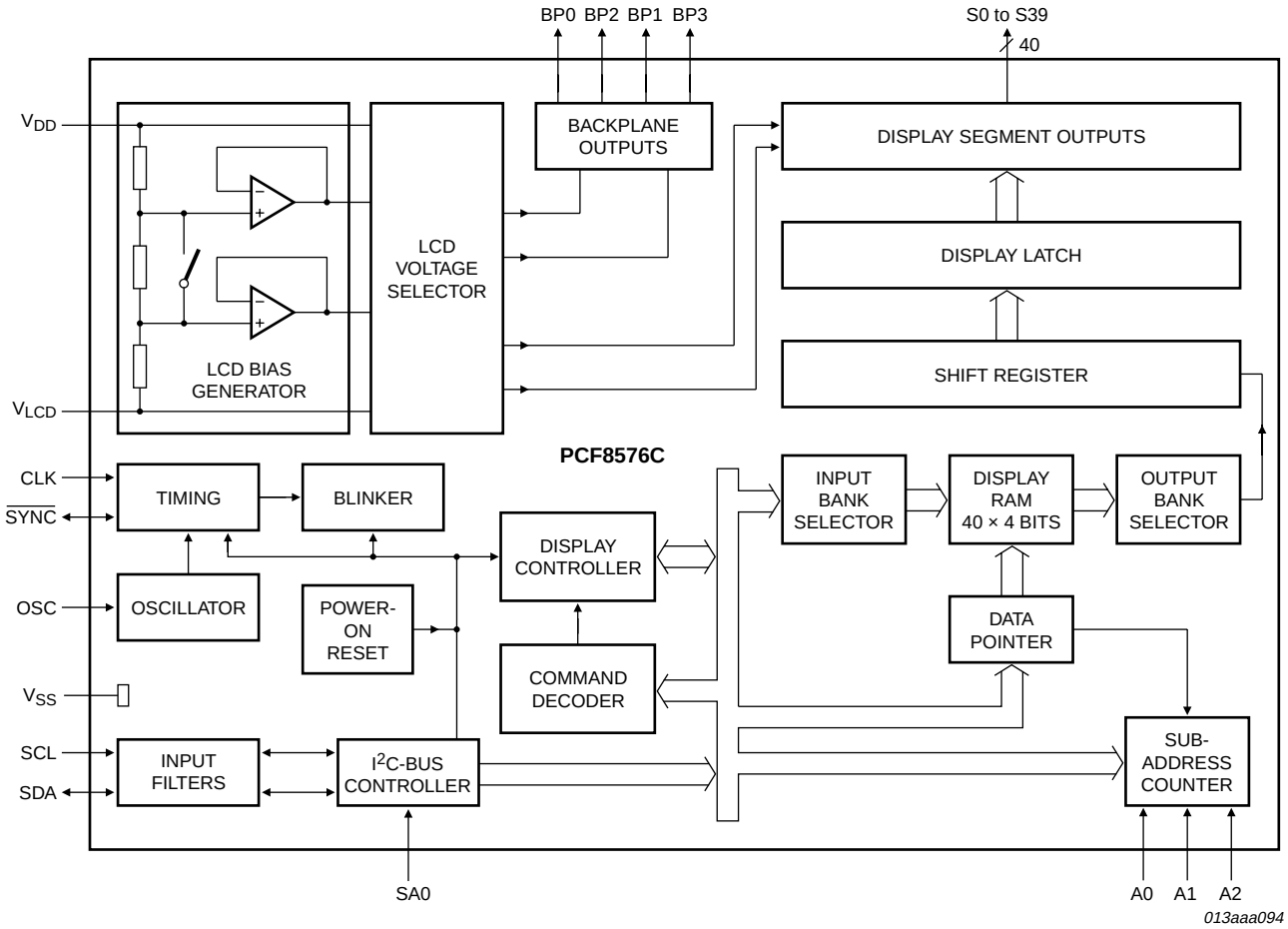
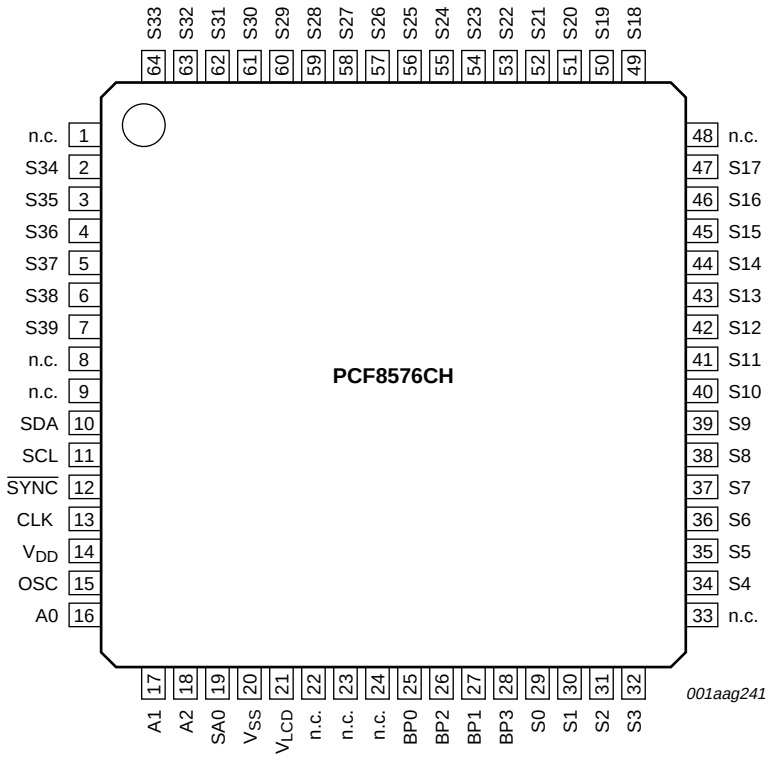


Fig 1. Block diagram of PCF8576C

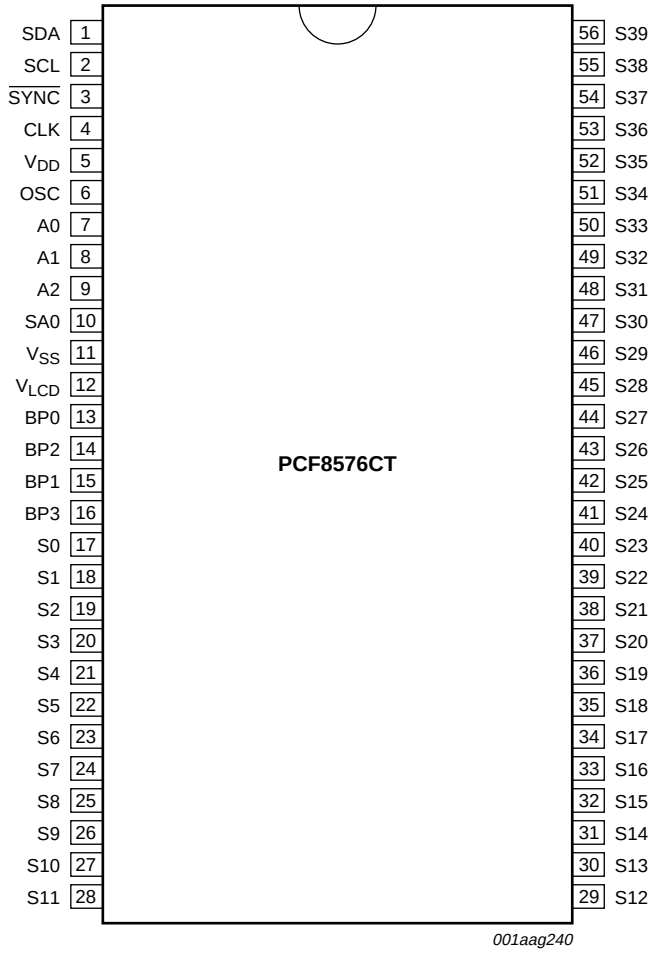
6. Pinning information

6.1 Pinning



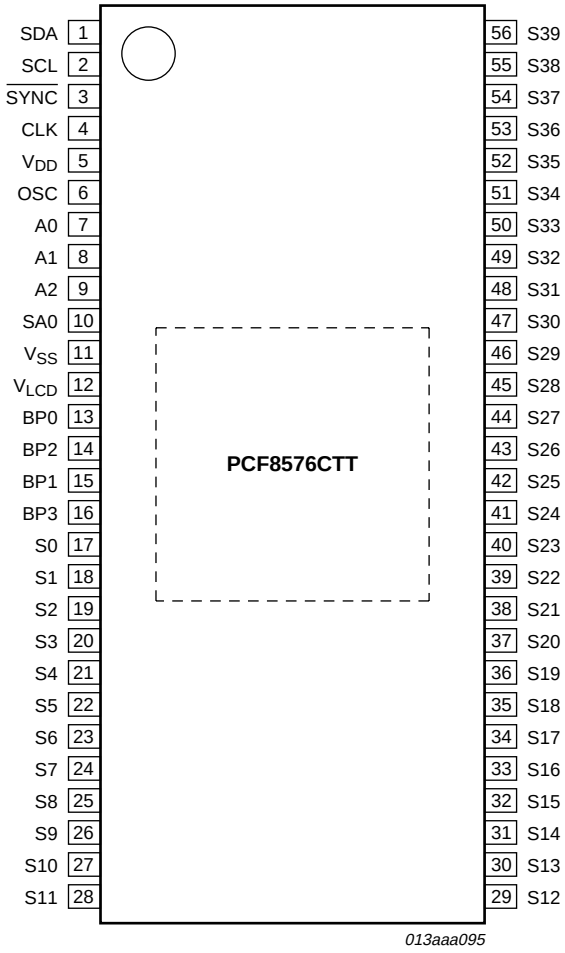
Top view. For mechanical details, see Figure 32.

Fig 2. Pin configuration of PCF8576CH (LQFP64)



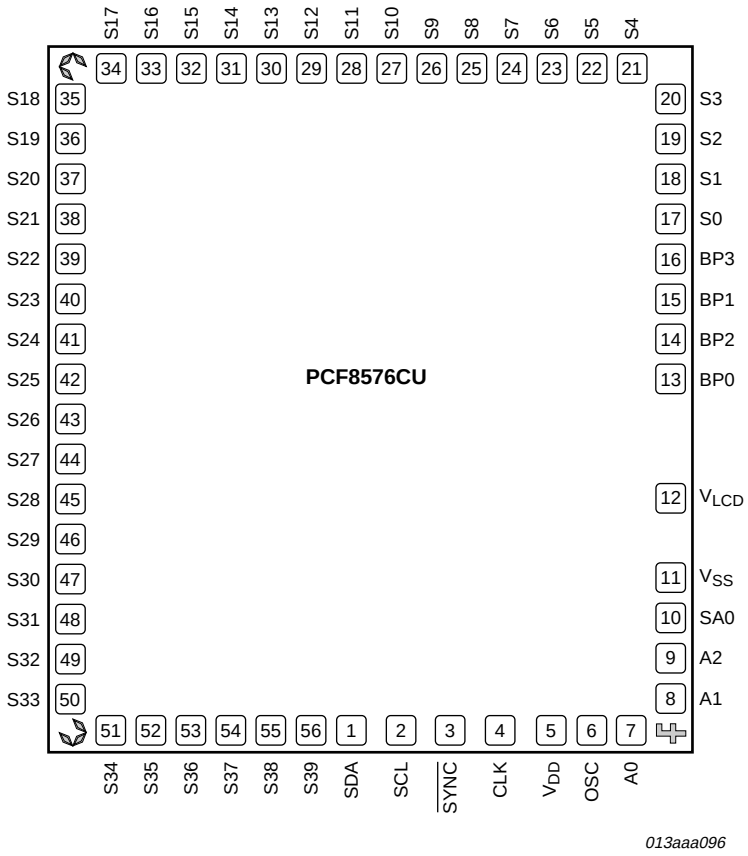
Top view. For mechanical details, see Figure 33.

Fig 3. Pin configuration of PCF8576CT (VSO56)



Top view. For mechanical details, see Figure 34.

Fig 4. Pin configuration of PCF8576CTT (HTSSOP56)



Top view. For mechanical details, see Figure 35, Figure 36 and Figure 37.

Fig 5. Pin locations of PCF8576CU

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	PCF8576CH	PCF8576CT PCF8576CTT	PCF8576CU	
SDA	10	1	1	I^2C-bus serial data input and output
SCL	11	2	2	I^2C-bus serial clock input
$\overline{SYNC}$	12	3	3	cascade synchronization input and output
CLK	13	4	4	external clock input/output
V_{DD}	14	5	5[1]	supply voltage
OSC	15	6	6	internal oscillator enable input
A0 to A2	16 to 18	7 to 9	7 to 9	subaddress inputs
SA0	19	10	10	I^2C-bus address input; bit 0
V_{SS}	20	11	11	logic ground
V_{LCD}	21	12	12	LCD supply voltage
BP0, BP2, BP1, BP3	25 to 28	13 to 16	13 to 16	LCD backplane outputs
S0 to S39	2 to 7, 29 to 32, 34 to 47, 49 to 64	17 to 56	17 to 56	LCD segment outputs
n.c.	1, 8, 9, 22 to 24, 33, 48	-	-	not connected

[1] The substrate (rear side of the die) is wired to V_{DD} but should not be electrically connected.

7. Functional description

The PCF8576C is a versatile peripheral device designed to interface any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 40 segments.

The display configurations possible with the PCF8576C depend on the number of active backplane outputs required. Display configuration selection is shown in Table 4. All of the display configurations given in Table 4 can be implemented in the typical system shown in Figure 6.

Table 4. Display configurations

Number of:		7 segment numeric		14-segment numeric		Dot matrix
Backplanes	Elements	Digits	Indicator symbols	Characters	Indicator symbols	
4	160	20	20	10	20	160 (4 × 40)
3	120	15	15	8	8	120 (3 × 40)
2	80	10	10	5	10	80 (2 × 40)
1	40	5	5	2	12	40 (1 × 40)

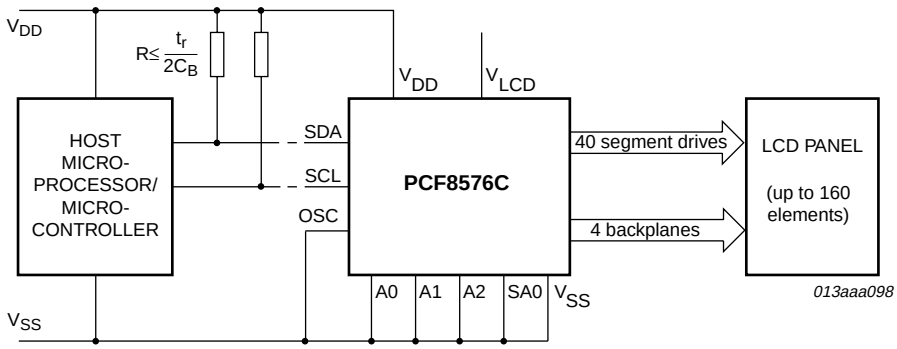


Fig 6. Typical system configuration

The host microprocessor or microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576C.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (pins V_{DD}, V_{SS} and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-on-reset

At power-on the PCF8576C resets to the following starting conditions:

- All backplane and segment outputs are set to V_{DD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset (as defined in Table 8)

- The I²C-bus interface is initialized
- The data pointer and the subaddress counter are cleared

Remark: Do not transfer data on the I²C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

The full-scale LCD voltage (V_{oper}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin V_{LCD}.

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three series resistors connected between V_{DD} and V_{LCD}. The center resistor can be switched out of the circuit to provide a ½ bias voltage level for the 1:2 multiplex configuration.

7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 5.

Table 5. Preferred LCD drive modes: summary of characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Bias levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} < 3 \times V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{1}{n} + \frac{(n-1)}{n} \times \left(\frac{1}{1+a}\right)^2} \quad (1)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

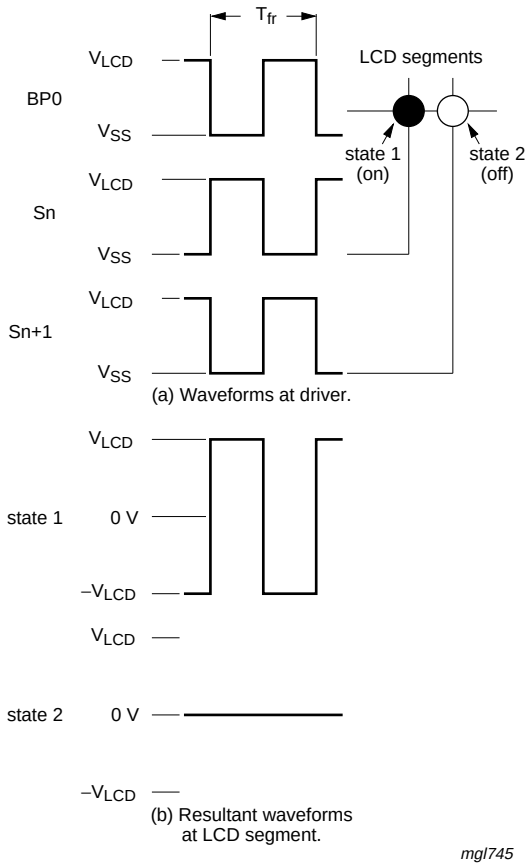
These compare with $V_{LCD} = 3 V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 7.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

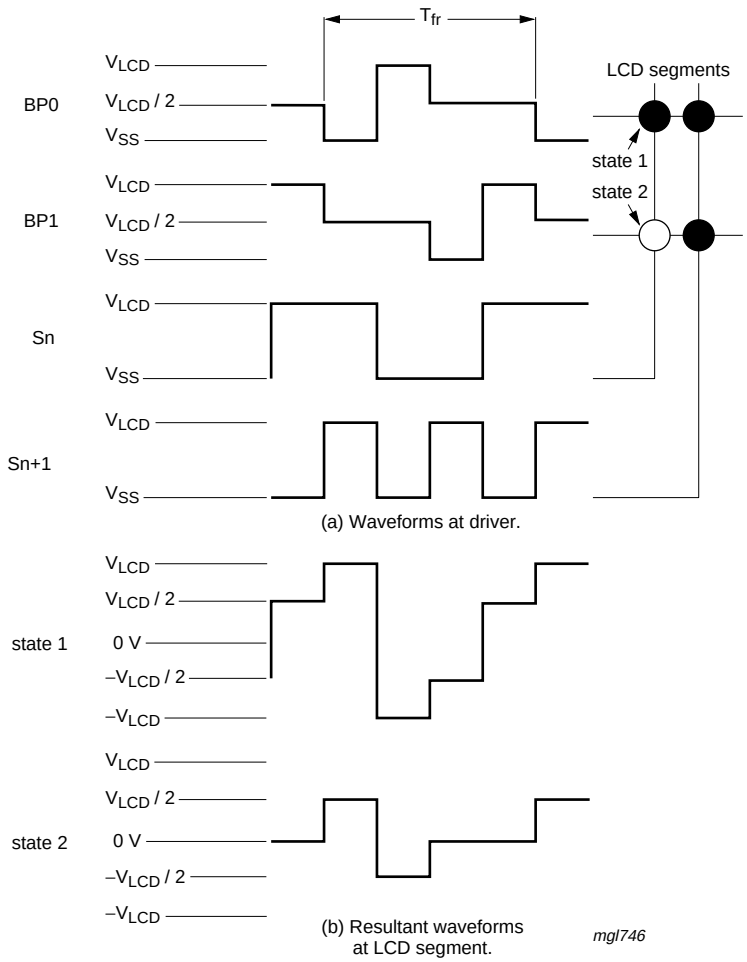
$V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 7. Static drive mode waveforms

7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8576C allows the use of ½ bias or ⅓ bias (see Figure 8 and Figure 9).



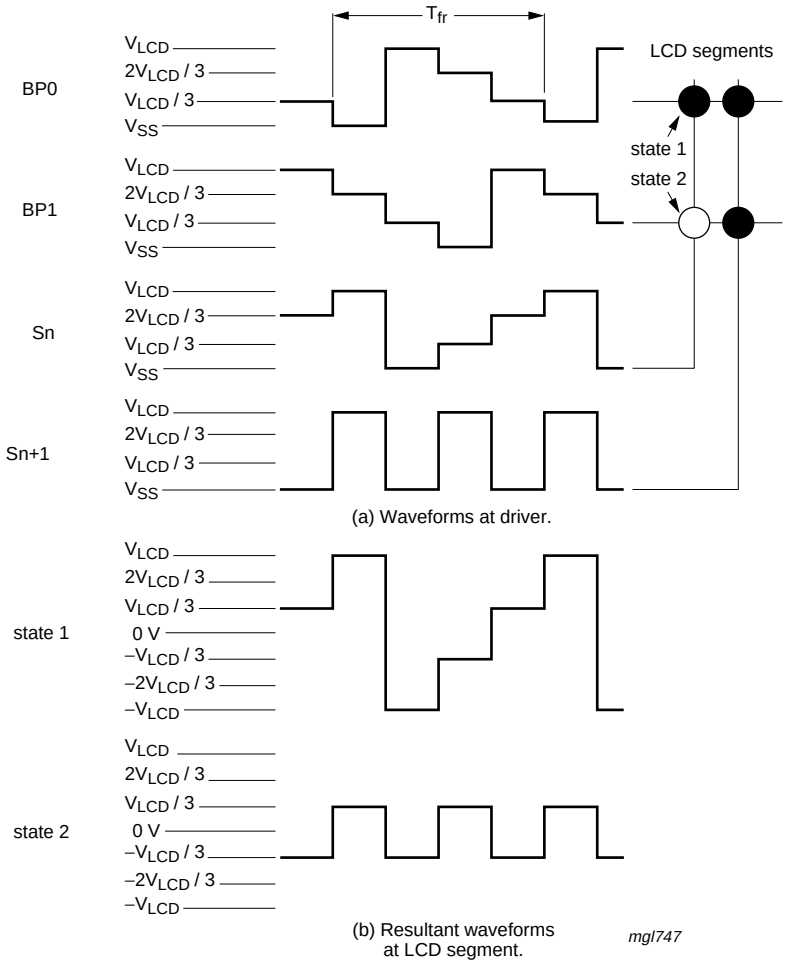
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$

Fig 8. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$

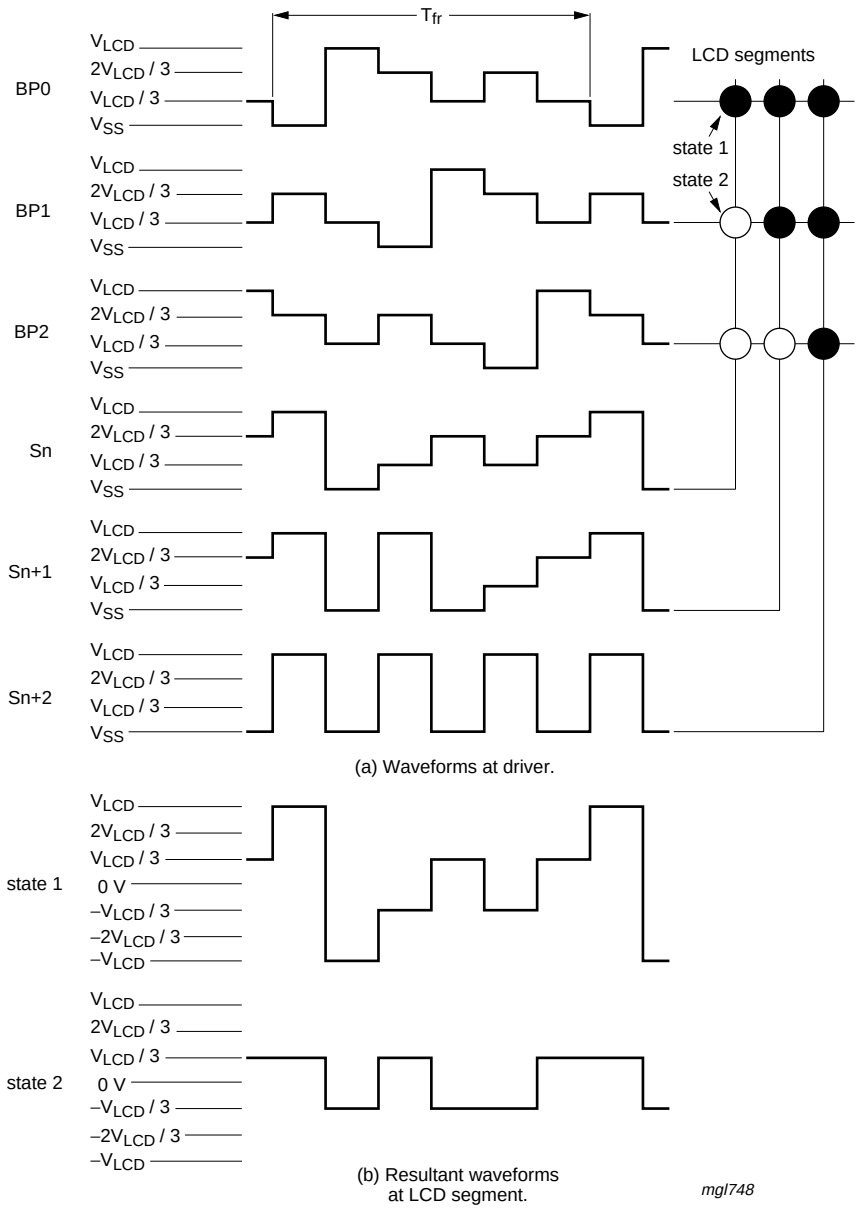
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:2 multiplex drive mode with $^1/_3$ bias

7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 10.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

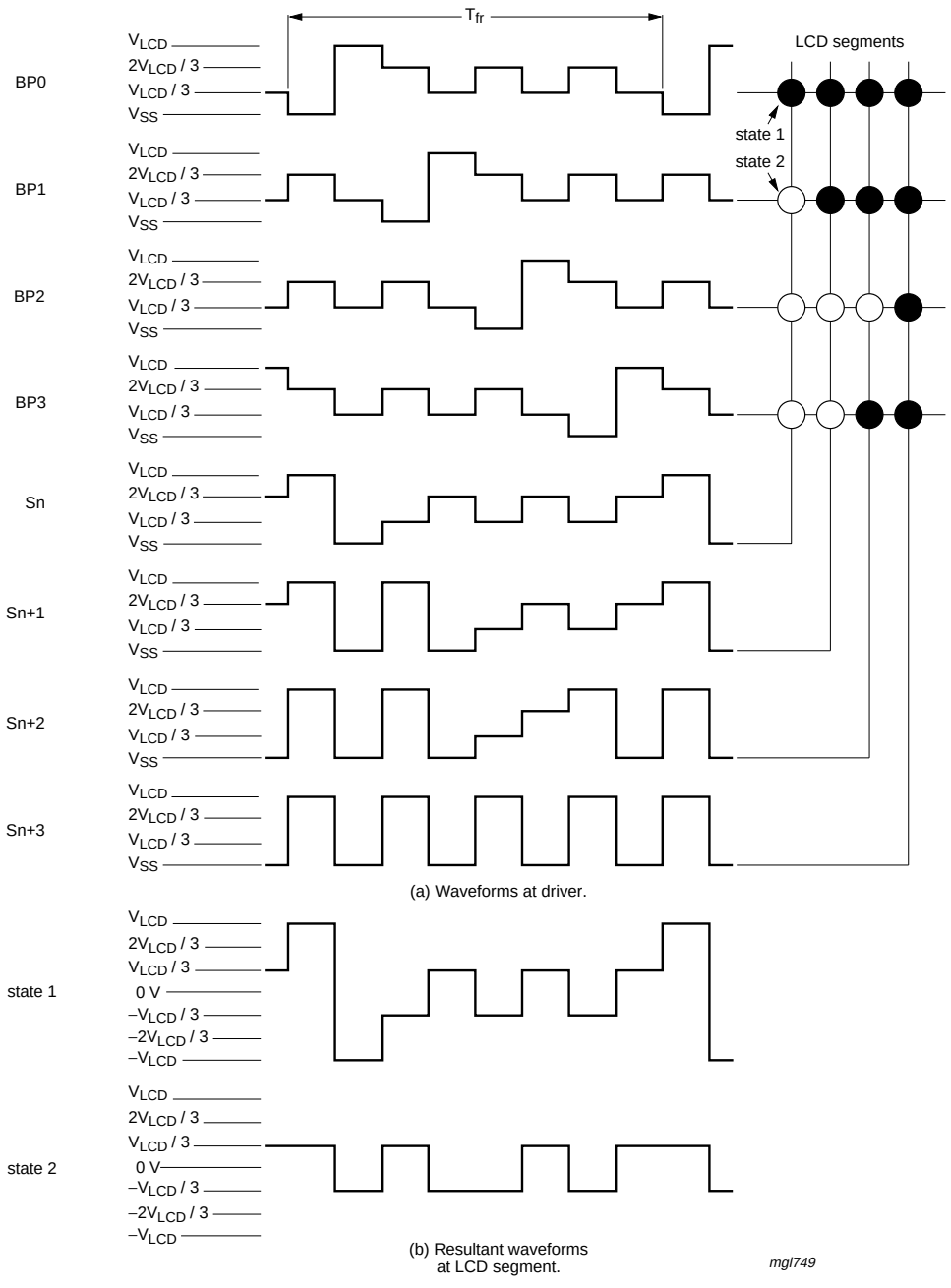
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 11.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 11. Waveforms for the 1:4 multiplex mode with ⅓ bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCF8576C are timed by the frequency f_{clk}, which equals either the built-in oscillator frequency f_{osc} or the external clock frequency $f_{clk(ext)}$.

The clock frequency (f_{clk}) determines the LCD frame frequency (f_{fr}) and the maximum rate for data reception from the I^2C-bus. To allow I^2C-bus transmissions at their maximum data rate of 100 kHz, f_{clk} should be chosen to be above 125 kHz.

7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case, the output from pin CLK is the clock signal for any cascaded PCF8576s or PCF8566s in the system.

Remark: The PCF8576C is backwards compatible with the PCF8576 (V_{oper} up to 9 V). Where resistor R_{ext} (on pin OSC) to V_{SS} is present, the internal oscillator is selected.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.

Remark: A clock signal must always be supplied to the device. Removing the clock, freezes the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing

The timing of the PCF8576C sequences the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between the PCF8576Cs in the system. The timing also generates the LCD frame frequency which is derived as an integer division of the clock frequency (see Table 6). The frame frequency is set by the mode set commands when an internal clock is used or by the frequency applied to the pin CLK when an external clock is used.

Table 6. LCD frame frequencies [1]

PCF8576C mode	Frame frequency	Nominal frame frequency (Hz)
Normal mode	$f_{fr} = \frac{f_{clk}}{2880}$	69 [2]
Power saving mode	$f_{fr} = \frac{f_{clk}}{480}$	65 [3]

[1] The possible values for f_{clk} see Table 20.

[2] For f_{clk} = 200 kHz.

[3] For f_{clk} = 31 kHz.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power consumption.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C-bus. When a device is unable to process a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C-bus but no data loss occurs.

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs and one column of the display RAM.

7.8 Shift register

The shift register transfers display information from the display RAM to the display register while previous data is displayed.

7.9 Segment outputs

The LCD drive section includes 40 segment outputs, S0 to S39, which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

7.10 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

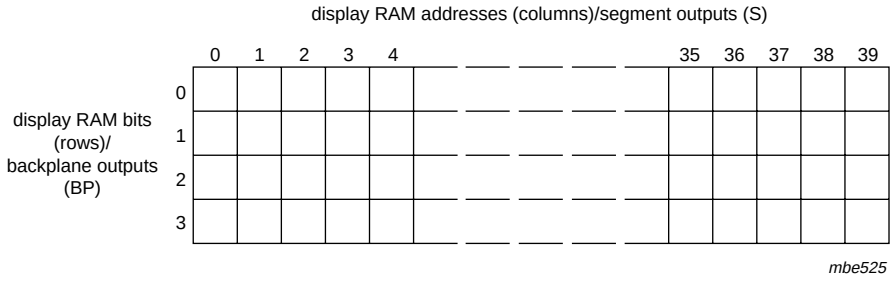
- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.11 Display RAM

The display RAM is a static 40 $\times$ 4-bit RAM which stores LCD data. A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state. There is a direct relationship between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The display RAM bit map Figure 12 shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3 respectively.



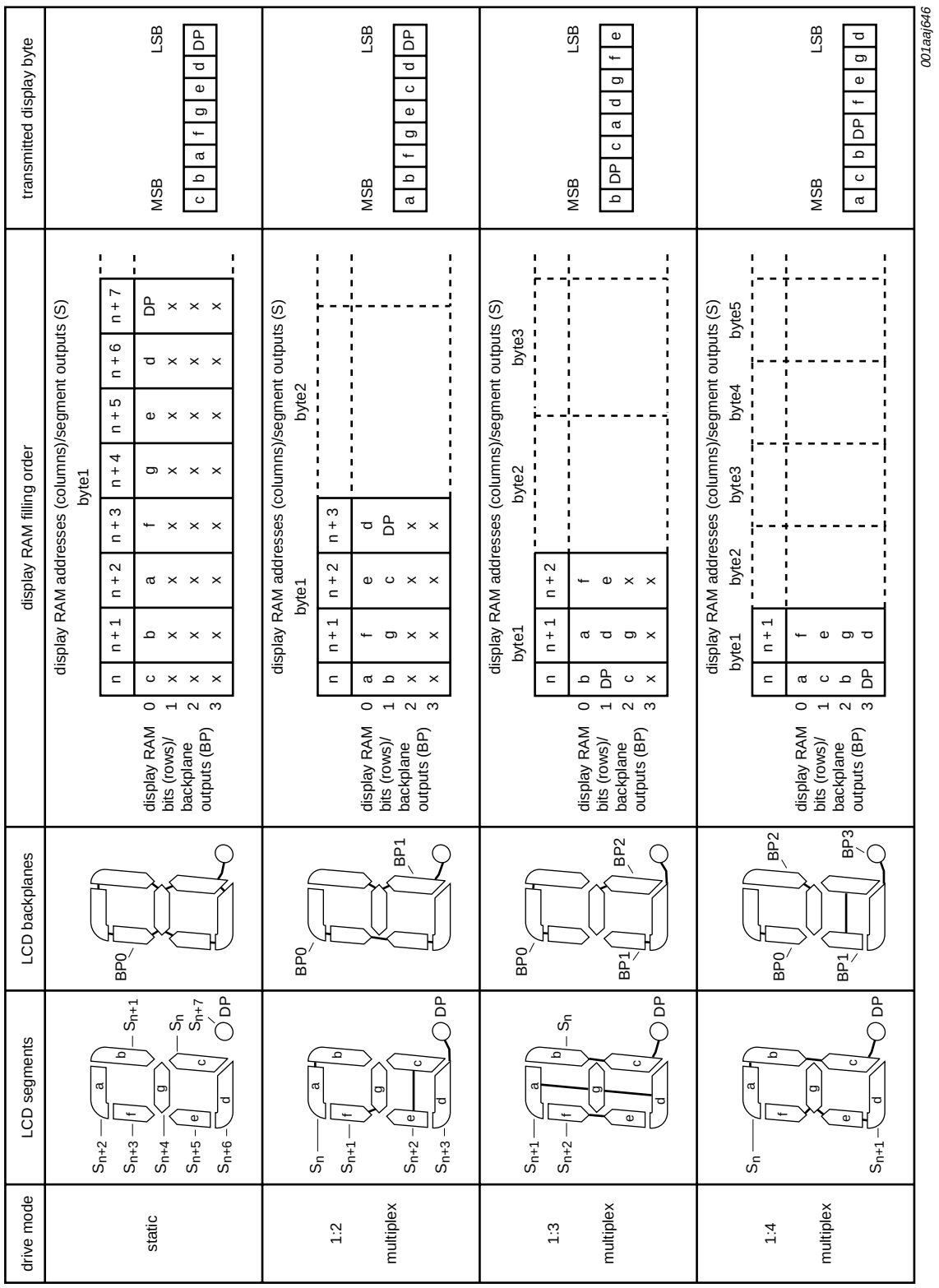
Display RAM bit map showing direct relationship between RAM addresses and segment outputs; also between bits in a RAM word and the backplane outputs.

Fig 12. Display RAM bit map

When display data is transmitted to the PCF8576C, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for an acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triplets or quadruplets. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 13; the RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 13:

- In the static drive mode, the eight transmitted data bits are placed in row 0 of eight successive 4-bit RAM words.
- In the 1:2 multiplex mode, the eight transmitted data bits are placed in pairs into row 0 and 1 of four successive 4-bit RAM words.
- In the 1:3 multiplex mode, the eight bits are placed in triples into row 0, 1 and 2 to three successive 4-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.
- In the 1:4 multiplex mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2 and 3 of two successive 4-bit RAM words.



x = data bit unchanged.

Fig 13. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

7.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load data pointer command (see Table 13). After this, the data byte is stored starting at the display RAM address indicated by the data pointer (see Figure 13). Once each byte is stored, the data pointer is automatically incremented based on the selected LCD configuration.

The contents of the data pointer are incremented as follows:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^2C-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.

7.13 Sub-address counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device select command (see Table 14). If the contents of the subaddress counter and the hardware subaddress do not match then data storage is blocked but the data pointer will be incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1:3 multiplex mode).

7.14 Bank selector

7.14.1 Output bank selector

The output bank selector (see Table 15), selects one of the four bits per display RAM address for transfer to the display register. The actual bit selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of bit 0 are selected, followed sequentially by the contents of bit 1, bit 2 and then bit 3.
- In 1:3 multiplex mode: bits 0, 1 and 2 are selected sequentially.
- In 1:2 multiplex mode: bits 0 and 1 are selected.
- In the static mode: bit 0 is selected.

The PCF8576C includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank select command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 multiplex drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

7.14.2 Input bank selector

The input bank selector (see Table 15) loads display data into the display RAM based on the selected LCD drive configuration. Using the bank select command, display data can be loaded in bit 2 into static drive mode or in bits 2 and 3 into 1:2 multiplex drive mode. The input bank selector functions independently of the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCF8576C are very versatile. The whole display can be blinked at frequencies selected by the blink command. The blinking frequencies are integer fractions of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see Table 7).

Table 7. Blink frequencies

Blinking mode	Normal operating mode ratio	Power saving mode ratio	Blink frequency
off	-	-	blinking off
1	$f_{blink} = \frac{f_{clk}}{92160}$	$f_{blink} = \frac{f_{clk}}{15360}$	2 Hz
2	$f_{blink} = \frac{f_{clk}}{184320}$	$f_{blink} = \frac{f_{clk}}{30720}$	1 Hz
3	$f_{blink} = \frac{f_{clk}}{368640}$	$f_{blink} = \frac{f_{clk}}{61440}$	0.5 Hz

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink command (see Table 16).

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display needs to be blinked at a frequency other than the nominal blink frequency, this can be done using the mode set command to set and reset the display enable bit E at the required rate (see Table 9).

8. Basic architecture

8.1 Characteristics of the I²C-bus

The I²C-bus provides bidirectional, two-line communication between different IC or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). When connected to the output stages of a device, both lines must be connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 14.

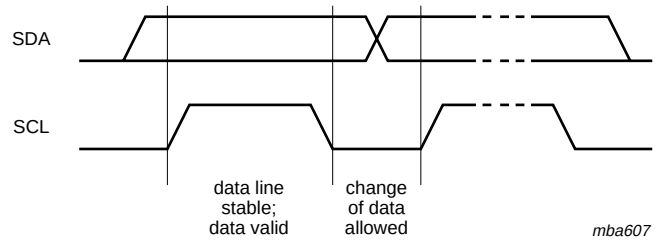


Fig 14. Bit transfer

8.1.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 15.

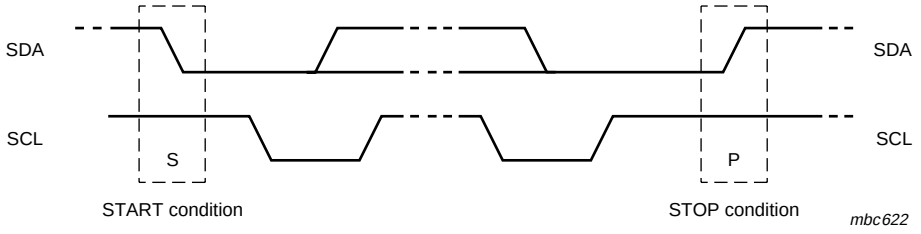


Fig 15. Definition of START and STOP conditions

8.1.2 System configuration

A device generating a message is a transmitter and a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is illustrated in Figure 16.

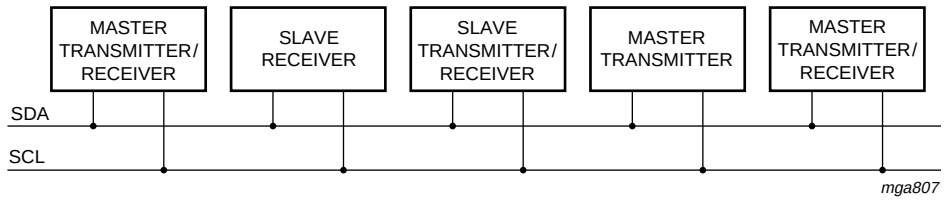


Fig 16. System configuration

8.1.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

Acknowledgement on the I^2C-bus is illustrated in Figure 17.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the master receiver must leave the data line HIGH during the 9th pulse to not acknowledge. The master will now generate a STOP condition.

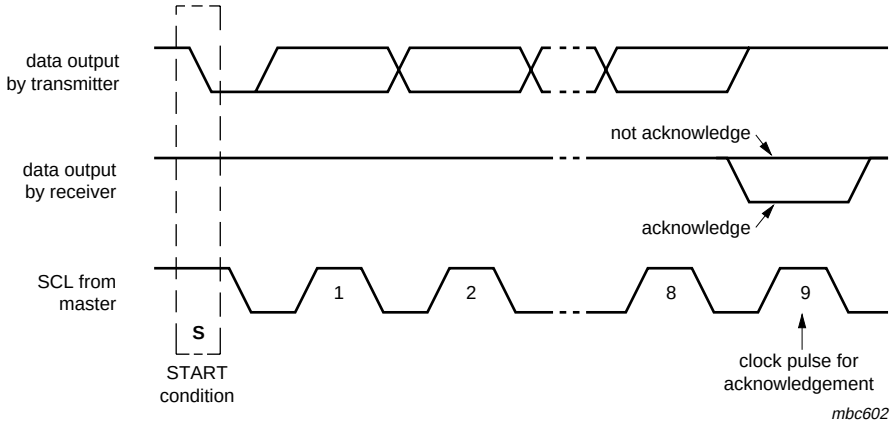


Fig 17. Acknowledgement on the I^2C-bus

8.1.4 PCF8576C I²C-bus controller

The PCF8576C acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8576C are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, the transferred command data and the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} using a binary coding scheme so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576C forces the SCL line LOW until its internal operations are completed. This is known as the clock synchronization feature of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

8.1.5 Input filter

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.2 I²C-bus protocol

Two I²C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576C. The least significant bit of the slave address that a PCF8576C responds to is defined by the level tied at its input SA0. Therefore, two types of PCF8576C can be distinguished on the same I²C-bus which allows:

- Up to 16 PCF8576Cs on the same I²C-bus for very large LCD applications.
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Figure 18. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8576C slave addresses available. All PCF8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576Cs with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576Cs.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576Cs on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576C device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576C. After the last display byte, the I²C-bus master issues a STOP condition (P).

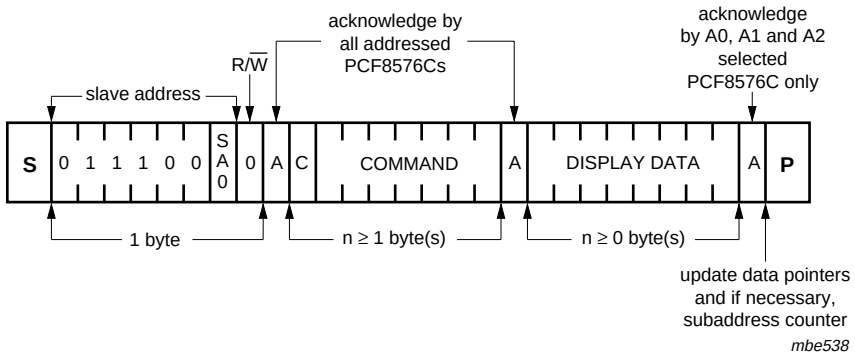
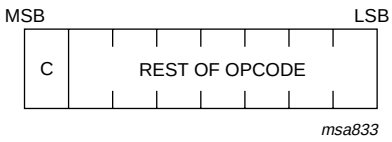


Fig 18. I²C-bus protocol

8.3 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position as shown in Figure 19. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576C are defined in Table 8.



(1) C = 0; last command

(2) C = 1; commands continue

Fig 19. General format of byte command

Table 8. Definition of PCF8576C commands

Command	OPCODE								Reference	Description
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
mode set	C	1	0	LP	E	B	M1	M0	Section 8.3.1	defines LCD drive mode, LCD bias configuration, display status and power dissipation mode
load data pointer	C	0	P5	P4	P3	P2	P1	P0	Section 8.3.2	data pointer to define one of 40 display RAM addresses
device select	C	1	1	0	0	A2	A1	A0	Section 8.3.3	define one of eight hardware subaddresses
bank select	C	1	1	1	1	0	I	O	Section 8.3.4	bit I: defines input bank selection (storage of arriving display data); bit O: defines output bank selection (retrieval of LCD display data)
blink	C	1	1	1	0	A	BF1	BF0	Section 8.3.5	defines the blink frequency and blink mode

8.3.1 Mode set command

Table 9. LCD drive mode command bit description

LCD drive mode		Bit	
Drive mode	**Backplane**	**M1**	**M0**
static	BP0	0	1
1:2	BP0, BP1	1	0
1:3	BP0, BP1, BP2	1	1
1:4	BP0, BP1, BP2, BP3	0	0

Table 10. LCD bias configuration command bit description

LCD bias	Bit B
$^1/_3$ bias	0
$^1/_2$ bias	1

Table 11. Display status command bit description[1]

Display status	Bit E
disabled (blank)	0
enabled	1

[1] The possibility to disable the display allows implementation of blinking under external control.

Table 12. Power dissipation mode command bit description

Display status	Bit LP
normal mode	0
power saving mode	1

8.3.2 Load data pointer command

Table 13. Load data pointer command bit description

Description	Bits					
6 bit binary value, 0 to 39	P5	P4	P3	P2	P1	P0

8.3.3 Device select command

Table 14. Device select command bit description

Description	Bits		
3 bit binary value, 0 to 7	A2	A1	A0

8.3.4 Bank select command

Table 15. Bank select command[1]

Bank	Mode		Bit	Value
	Static	1:2 multiplex drive mode		
Input bank				
	RAM bit 0	RAM bits 0 and 1	I	0
	RAM bit 2	RAM bits 2 and 3		1
Output bank				
	RAM bit 0	RAM bits 0 and 1	O	0
	RAM bit 2	RAM bits 2 and 3		1

[1] The bank select command has no effect in 1:3 or 1:4 multiplex drive modes.

8.3.5 Blink command

Table 16. Blink frequency command bit description

Blink frequency	Bit	
	BF1	BF0
off	0	0
1	0	1
2	1	0
3	1	1

Table 17. Blink mode command bit description

Blink mode	Bit A
normal blinking	0
alternate RAM bank blinking	1

8.4 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576C and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

9. Internal circuitry

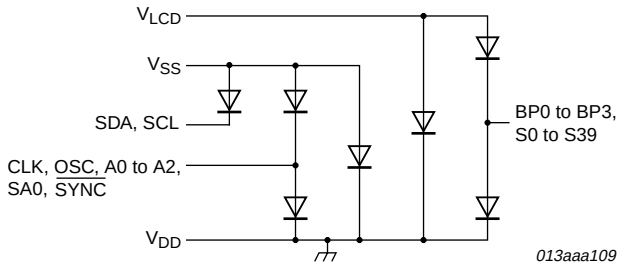


Fig 20. Device protection diagram

10. Limiting values

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	8.0	V
V_{LCD}	LCD supply voltage		[1]	V_{DD} – 8.0	V_{DD}	V
V_I	input voltage	on each of the pins SCL, SDA, CLK, $\overline{SYNC}$, SA0, OSC and A0 to A2		–0.5	8.0	V
V_O	output voltage	on each of the pins S0 to S39 and BP0 to BP3	[1]	–0.5	8.0	V
I_I	input current			–20	+20	mA
I_O	output current			–25	+25	mA
I_{DD}	supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P_o	output power			-	100	mW
T_{stg}	storage temperature		[2]	–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	±4000	V
		MM	[4]	-	±200	V
I_{lu}	latch-up current		[5]	-	100	mA

[1] Values with respect to V_{DD}.

[2] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

[3] Pass level; Human Body Model (HBM) according to JESD22-A114.

[4] Pass level; Machine Model (MM), according to JESD22-A115.

[5] Pass level; latch-up testing, according to JESD78.

11. Static characteristics

Table 19. Static characteristics

V_{DD} = 2.0 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 6.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.0	-	6.0	V
V_{LCD}	LCD supply voltage		[1]	V_{DD} − 6.0	-	V_{DD} − 2.0	V
I_{DD}	supply current:	f_{clk} = 200 kHz	[2]	-	-	120	µA
$I_{DD(lp)}$	low-power mode supply current	V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{clk} = 35 kHz; A0, A1 and A2 connected to V_{SS}		-	-	60	µA
Logic							
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		V_{SS}	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0 to A2 and SA0		0.7V_{DD}	-	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 0 mA		-	-	0.05	V
V_{OH}	HIGH-level output voltage	I_{OH} = 0 mA		V_{DD} − 0.05	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 1.0 V; V_{DD} = 5.0 V; on pins CLK and $\overline{SYNC}$		1	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins CLK, SCL, SDA, A0 to A2 and SA0		−1	-	+1	µA
$I_{L(OSC)}$	leakage current on pin OSC	V_I = V_{DD}		−1	-	+1	µA
I_{pd}	pull-down current	V_I = 1.0 V; V_{DD} = 5.0 V; on pins A0 to A2 and OSC		15	50	150	µA
R_{SYNC_N}	$\overline{SYNC}$ resistance			20	50	150	kΩ
V_{POR}	power-on reset voltage		[3]	-	1.0	1.6	V
C_I	input capacitance		[4]	-	-	7	pF
I²C-bus; pins SDA and SCL							
V_{IL}	LOW-level input voltage			V_{SS}	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	6.0	V
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	V_{OH} = 4.0 V; V_{DD} = 5.0 V		−1	-	-	mA
$I_{OL(SDA)}$	LOW-level output current on pin SDA	V_{OL} = 0.4 V; V_{DD} = 5.0 V		3	-	-	mA
LCD outputs							
V_{BP}	voltage on pin BP	C_{bpl} = 35 nF; on pins BP0 to BP3		−20	-	+20	mV
V_S	voltage on pin S	C_{sgm} = 5 nF; on pins S0 to S39		−20	-	+20	mV
R_{BP}	resistance on pin BP	V_{LCD} = V_{DD} − 5 V; on pins BP0 to BP3	[5]	-	-	5	kΩ
R_S	resistance on pin S	V_{LCD} = V_{DD} − 5 V; on pins S0 to S39	[5]	-	-	7.5	kΩ

[1] $V_{LCD} \leq V_{DD}$ − 3 V for ⅓ bias.

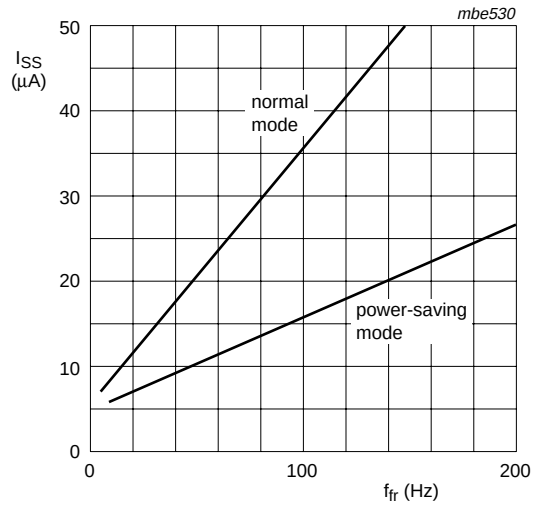
[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I²C-bus inactive.

[3] Resets all logic when $V_{DD} < V_{POR}$.

[4] Periodically sampled, not 100 % tested.

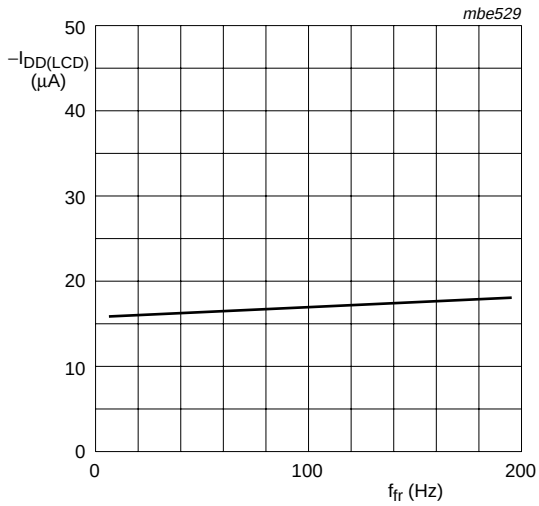
[5] Outputs measured one at a time.

11.1 Typical supply current characteristics



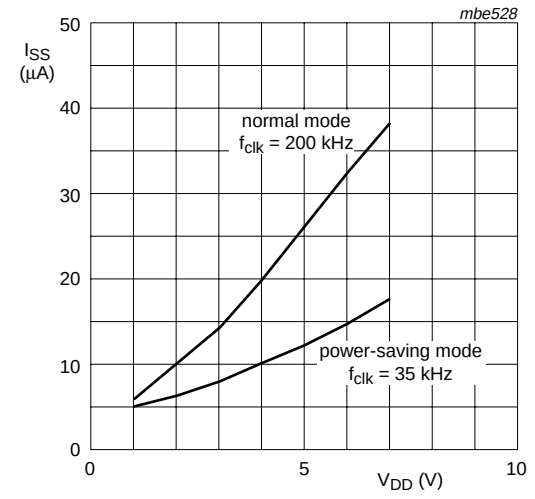
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C

Fig 21. I_{SS} as a function of f_{fr}



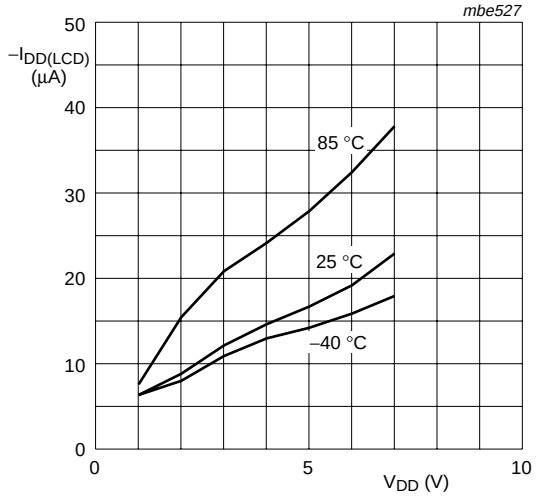
V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C

Fig 22. $-I_{DD(LCD)}$ as a function of f_{fr}



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C

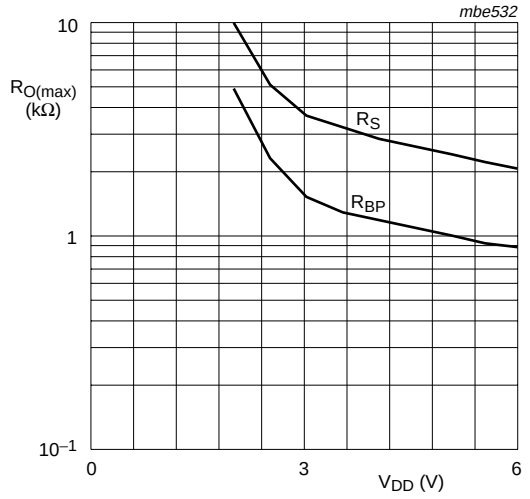
Fig 23. I_{SS} as a function of V_{DD}



V_{LCD} = 0 V; external clock; T_{amb} = 25 °C

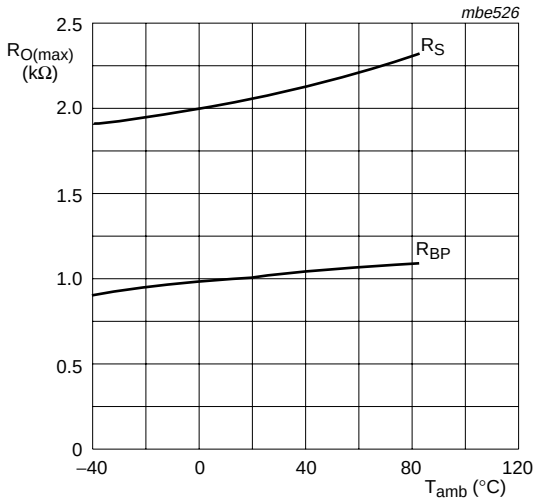
Fig 24. $-I_{DD(LCD)}$ as a function of V_{DD}

11.2 Typical LCD output characteristics



V_{LCD} = 0 V; T_{amb} = 25 °C

Fig 25. $R_{O(max)}$ as a function of V_{DD}



V_{DD} = 5 V; V_{LCD} = 0 V

Fig 26. $R_{O(max)}$ as a function of T_{amb}

12. Dynamic characteristics

Table 20. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 6.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing characteristics: driver timing waveforms (see Figure 27)						
f_{clk}	clock frequency	[1]				
		normal mode; V_{DD} = 5 V	125	200	315	kHz
		power saving mode; V_{DD} = 3 V	21	31	48	kHz
$t_{clk(H)}$	clock HIGH time		1	-	-	µs
$t_{clk(L)}$	clock LOW time		1	-	-	µs
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay		-	-	400	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time		1	-	-	µs
$t_{PD(drv)}$	driver propagation delay	$V_{LCD} = V_{DD} - 5$ V	-	-	30	µs
Timing characteristics: I²C-bus (see Figure 28)		[2]				
t_{BUF}	bus free time between a STOP and START condition		4.7	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	-	µs
t_r	rise time of both SDA and SCL signals		-	-	1	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	-	µs

[1] f_{clk} < 125 kHz, I²C-bus maximum transmission speed is derated.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

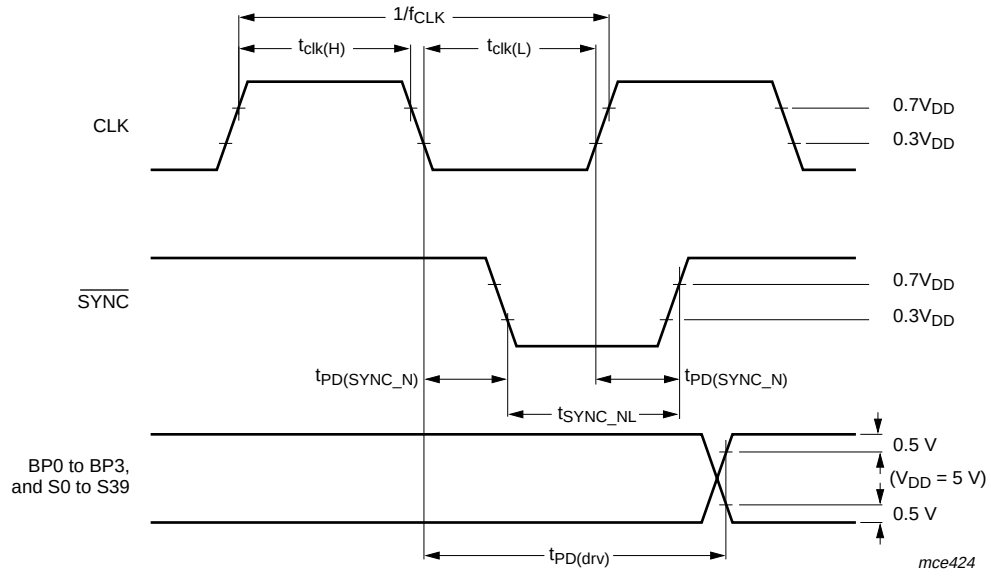


Fig 27. Driver timing waveforms

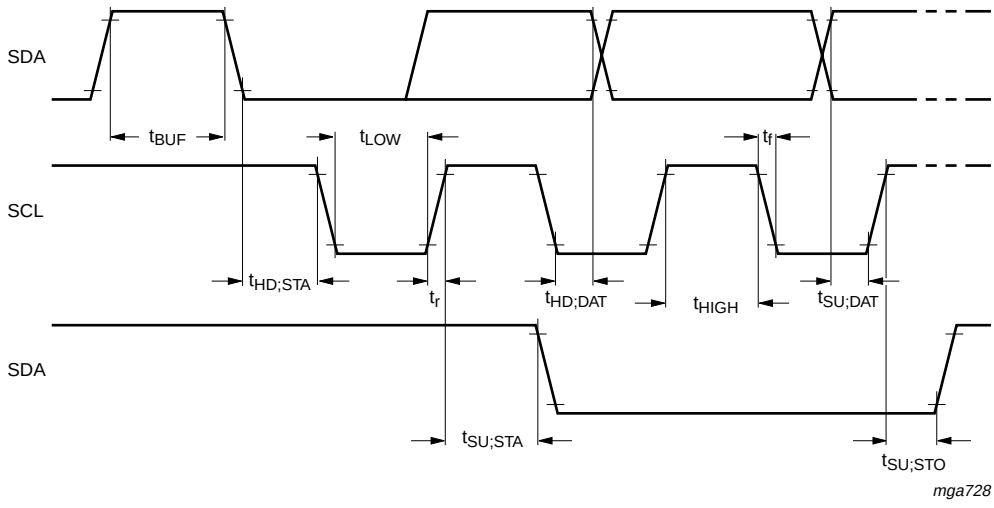


Fig 28. I²C-bus timing waveforms

13. Application information

13.1 Cascaded operation

In large display configurations, up to 16 PCF8576Cs can be recognized on the same I^2C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I^2C-bus slave address (SA0).

Table 21. Addressing cascaded PCF8576C

Cluster	Bit SA0	Pin A2	Pin A1	Pin A0	Device
1	0	0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	5
		1	1	0	6
		1	1	1	7
2	1	0	0	0	8
		0	0	1	9
		0	1	0	10
		0	1	1	11
		1	0	0	12
		1	0	1	13
		1	1	0	14
		1	1	1	15

Cascaded PCF8576Cs are synchronized. They can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576Cs of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 29).

The PCF8576C can also be cascaded with the PCF8566. The connections are identical to the PCF8576C cascade.

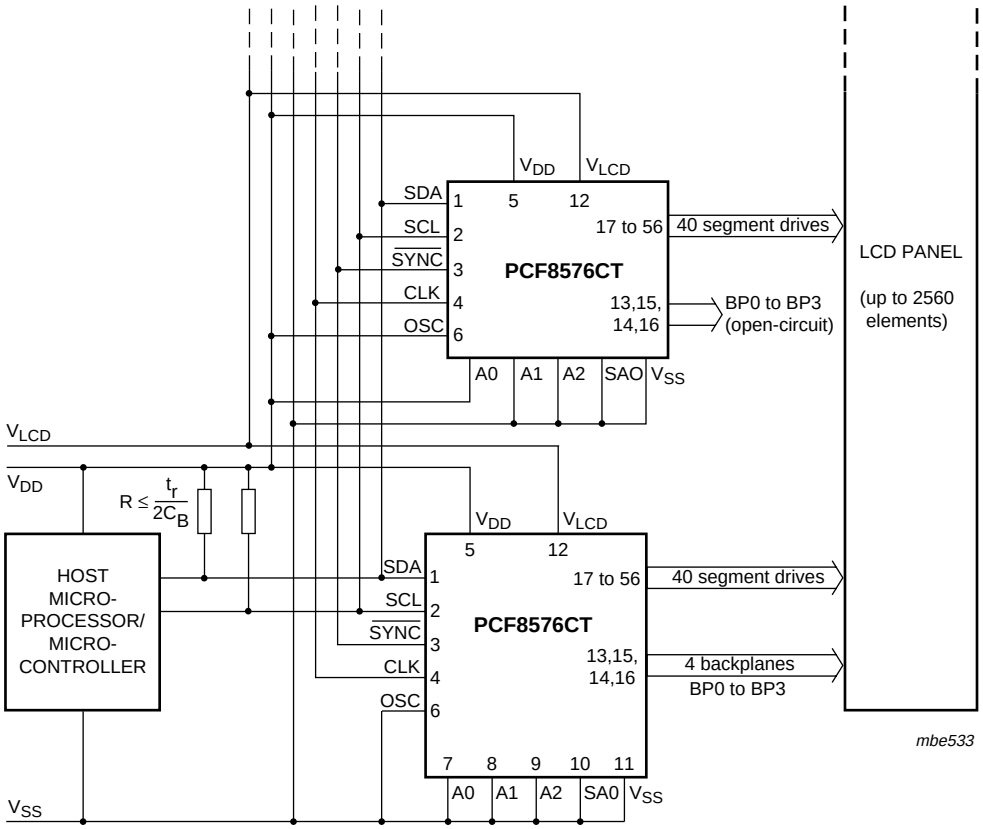


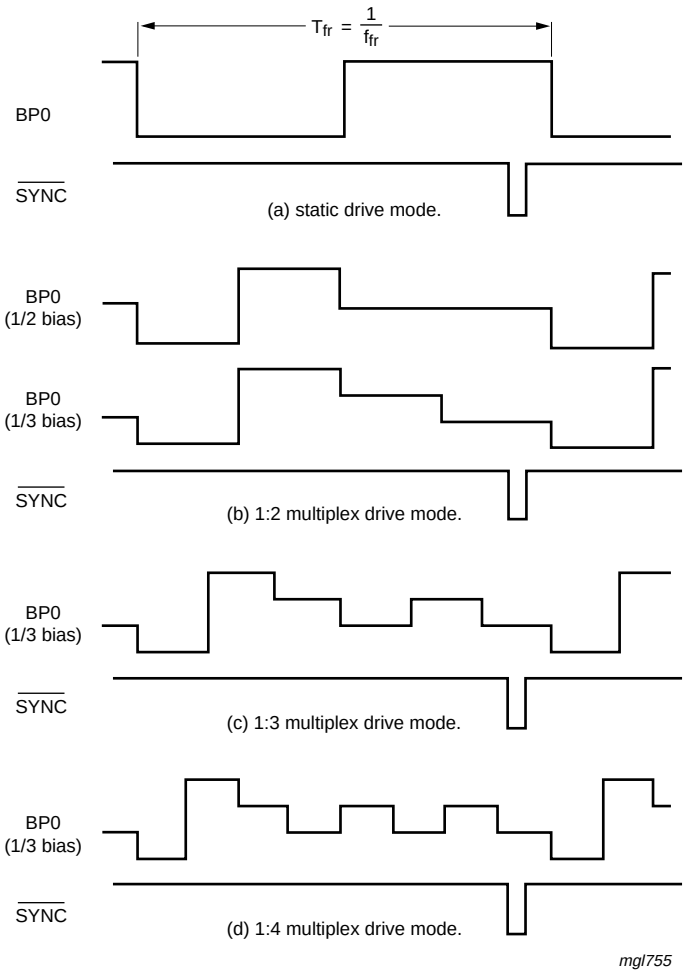
Fig 29. Cascaded PCF8576C configuration

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576Cs. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the defining a multiplex mode when PCF8576Cs with differing SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8576C asserts the $\overline{\text{SYNC}}$ line and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF8576C to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576C are shown in Figure 30.

For single plane wiring of packaged PCF8576Cs and chip-on-glass cascading, see Figure 31.

.



Excessive capacitive coupling between SCL or CLK and $\overline{SYNC}$ will cause erroneous synchronization. If this is a problem you can increase the capacitance of the $\overline{SYNC}$ line (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}.) Degradation of the positive edge of the $\overline{SYNC}$ pulse can be countered by an external pull-up resistor.

Fig 30. Synchronization of the cascade for the various PCF8576C drive modes

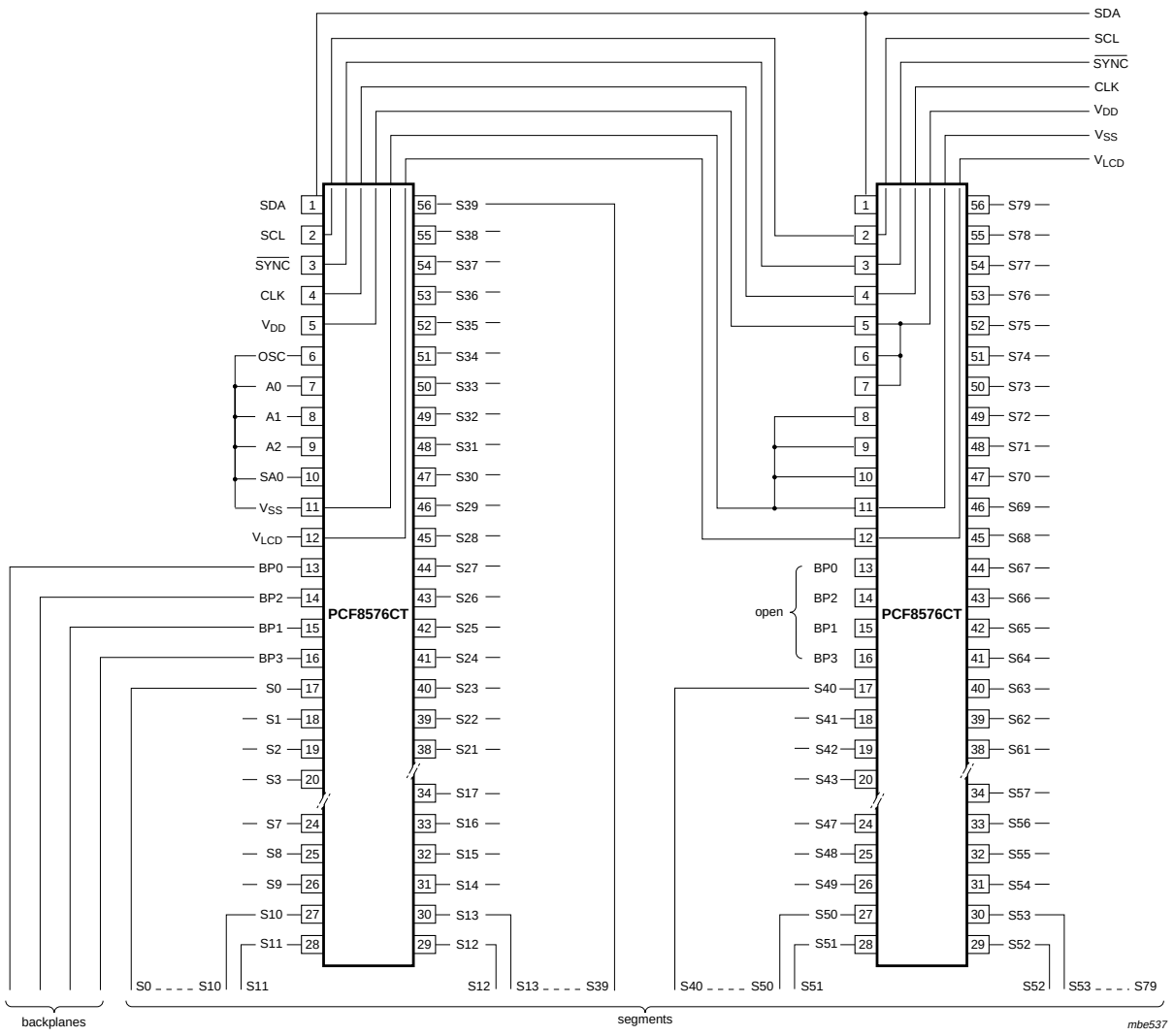
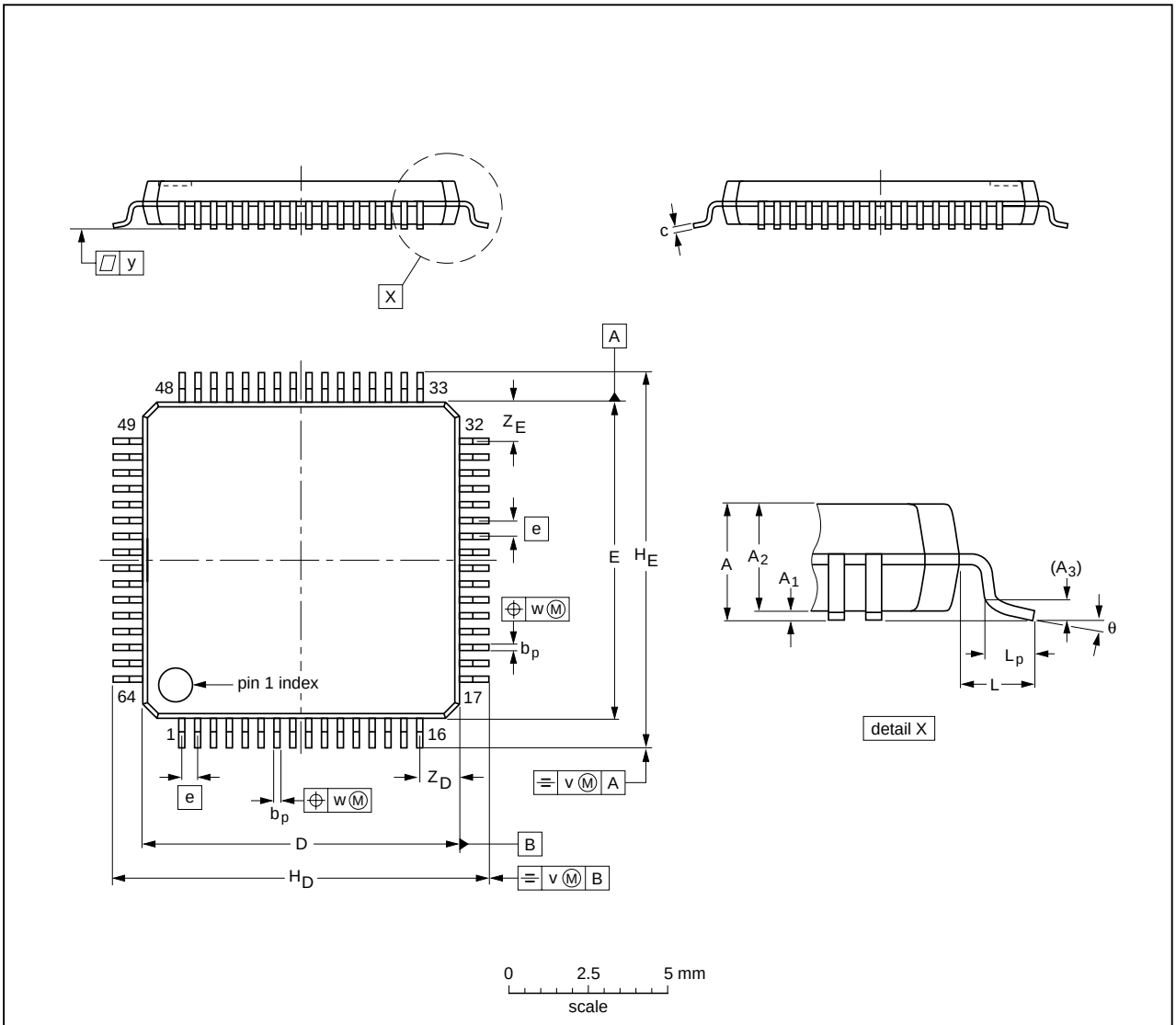


Fig 31. Single plane wiring of packaged PCF8576CTs

14. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

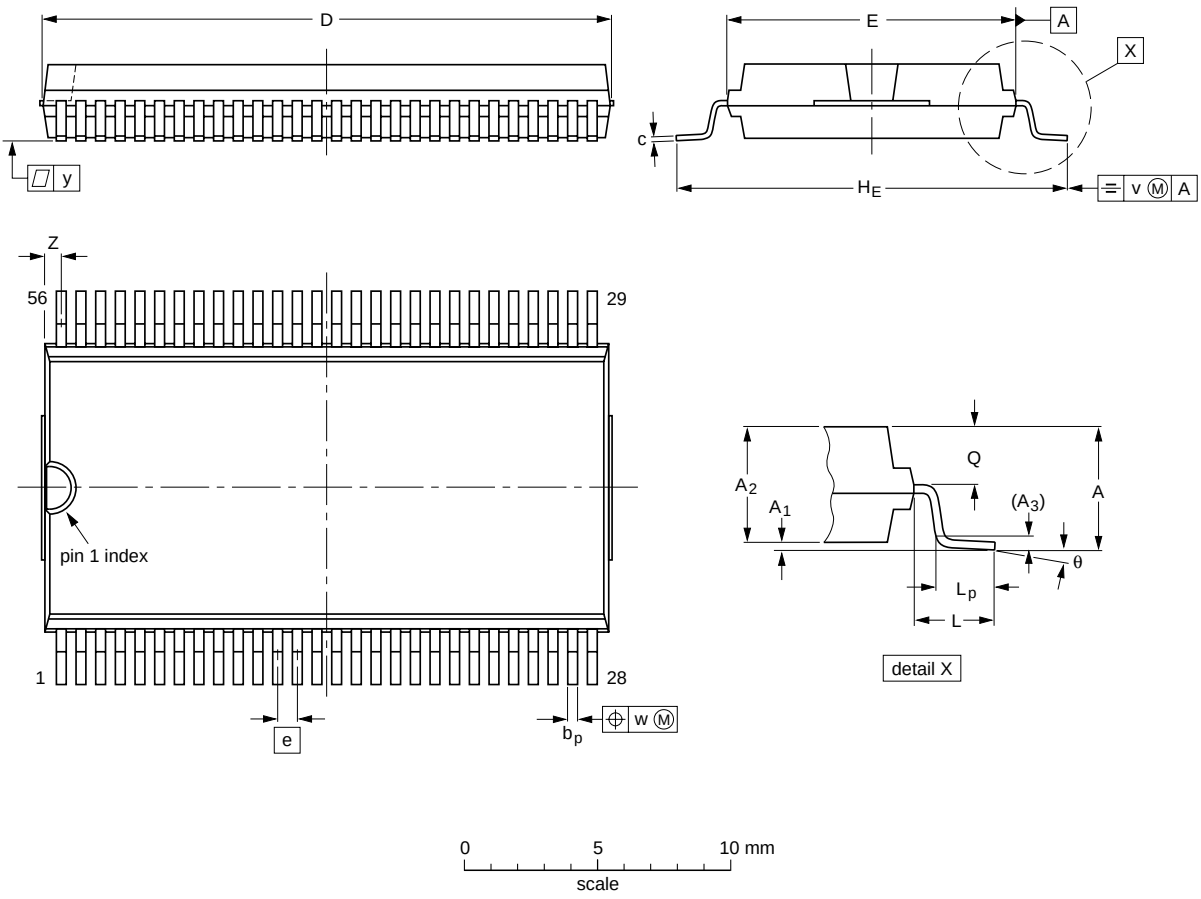
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 32. Package outline SOT314-2 (LQFP64) of PCF8576CH

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7^o 0^o
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

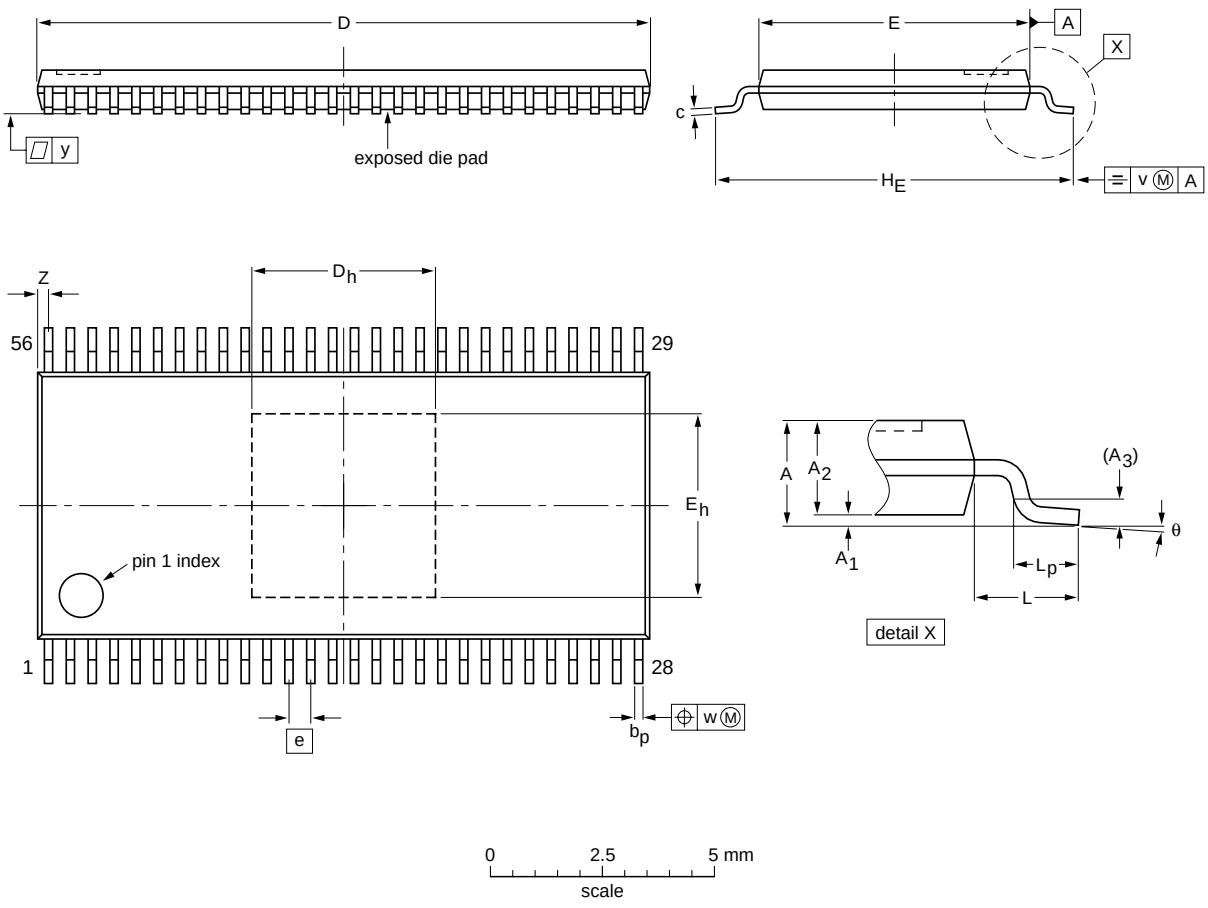
Notes

1. Plastic or metal protrusions of 0.3 mm (0.012 inch) maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT190-1						~~97-08-11~~ 03-02-19

Fig 33. Package outline SOT190-1 (VSO56) of PCF8576CT

HTSSOP56: plastic thermal enhanced thin shrink small outline package; 56 leads; body width 6.1 mm; exposed die pad **SOT793-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.80	0.25	0.27 0.17	0.20 0.09	14.1 13.9	4.3 4.1	6.2 6.0	4.3 4.1	0.5	8.3 7.9	1	0.8 0.4	0.2	0.08	0.1	0.4 0.1	8^o 0^o

Notes

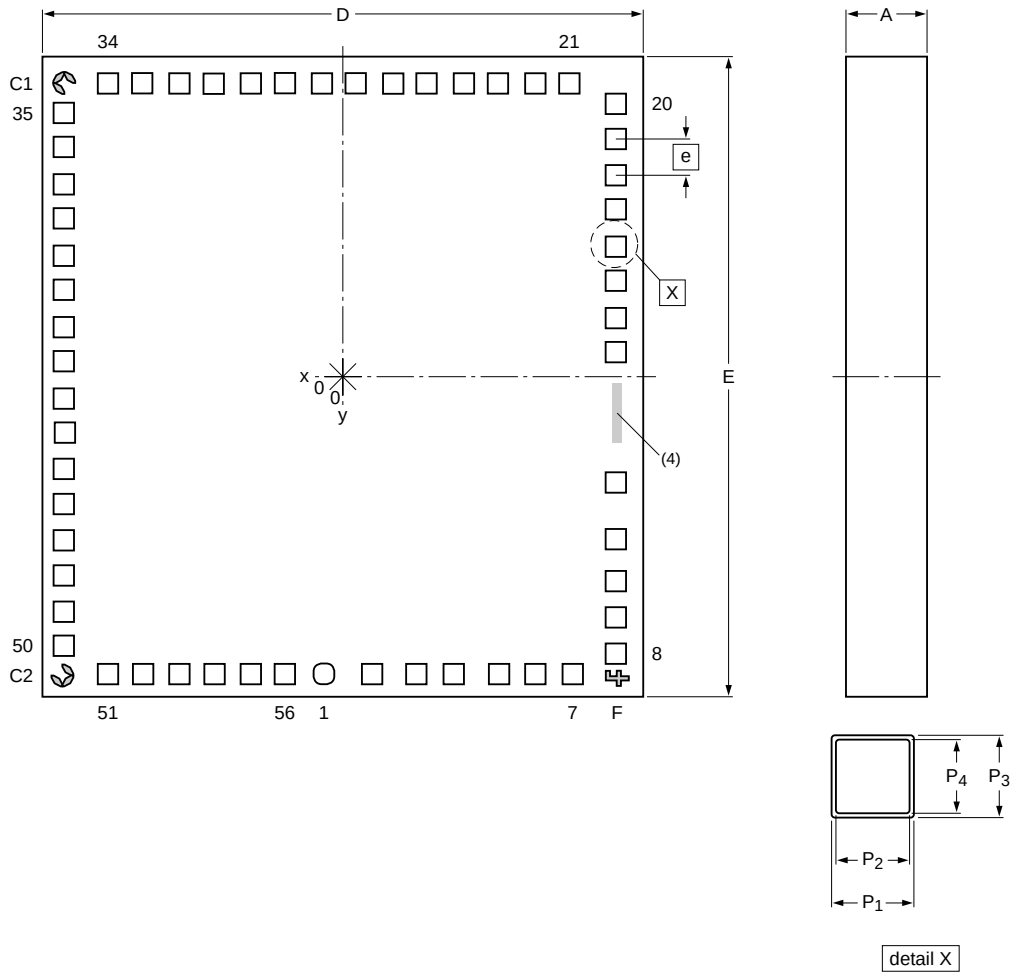
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT793-1	143E36T	MO-153				03-03-04

Fig 34. Package outline SOT793-1 (HTSSOP56) of PCF8576CTT

15. Bare die outline

Wire bond die; 56 bonding pads; 3.0 x 2.82 x 0.38 mm **PCF8576CU/10**



Dimensions

Unit		A	D	E	e(3)	P1(1)	P2(2)	P3(1)	P4(2)
mm	max	0.38	2.82	3.00	0.610	0.110	0.097	0.110	0.097
	nom								
	min				0.096				

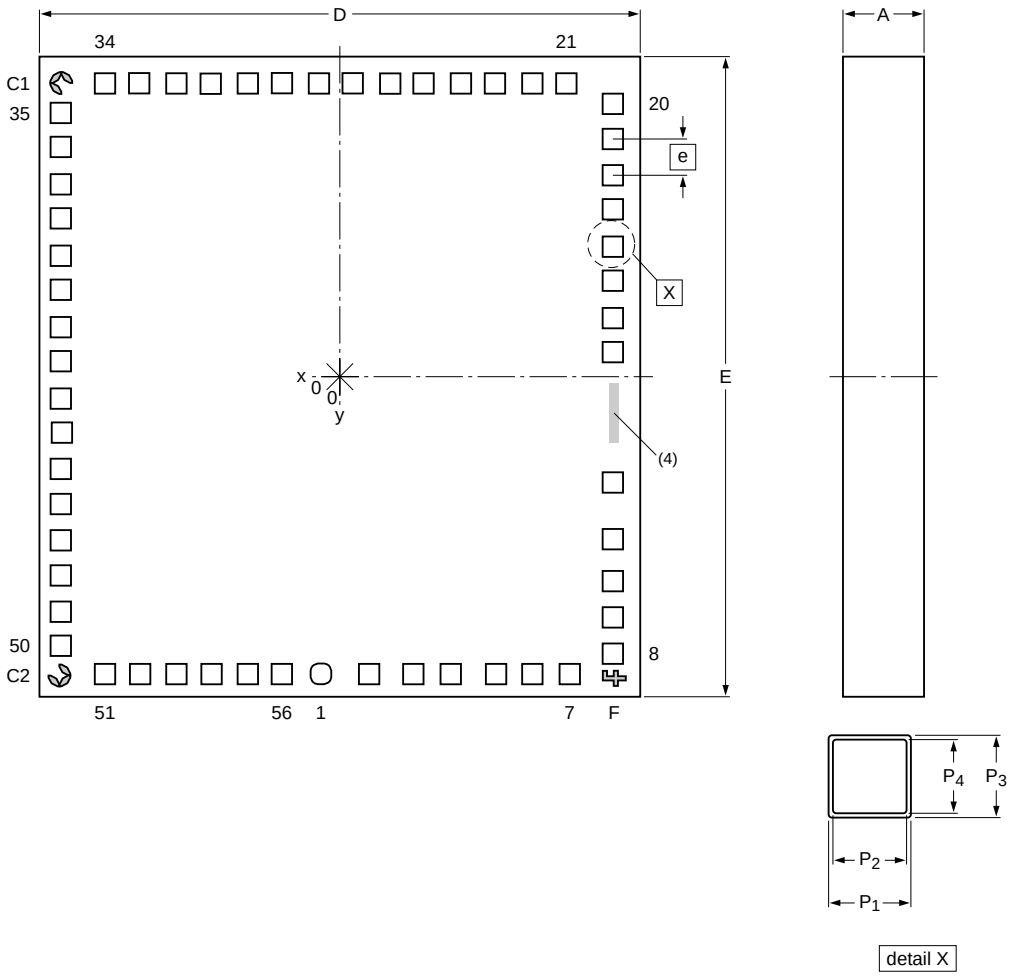
Note
1. Pad size
2. Passivation opening
3. Dimension not drawn to scale
4. Marking code: PC8576C-1

pcf8576cu_10_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576CU/10						09-06-02

Fig 35. Bare die outline of PCF8576CU/10

Wire bond die; 56 bonding pads; 3.0 x 2.82 x 0.38 mm **PCF8576CU**



Dimensions

Unit		A	D	E	e(3)	P1(1)	P2(2)	P3(1)	P4(2)
mm	max	0.38	2.82	3.00	0.610	0.110	0.097	0.110	0.097
	nom								
	min				0.096				

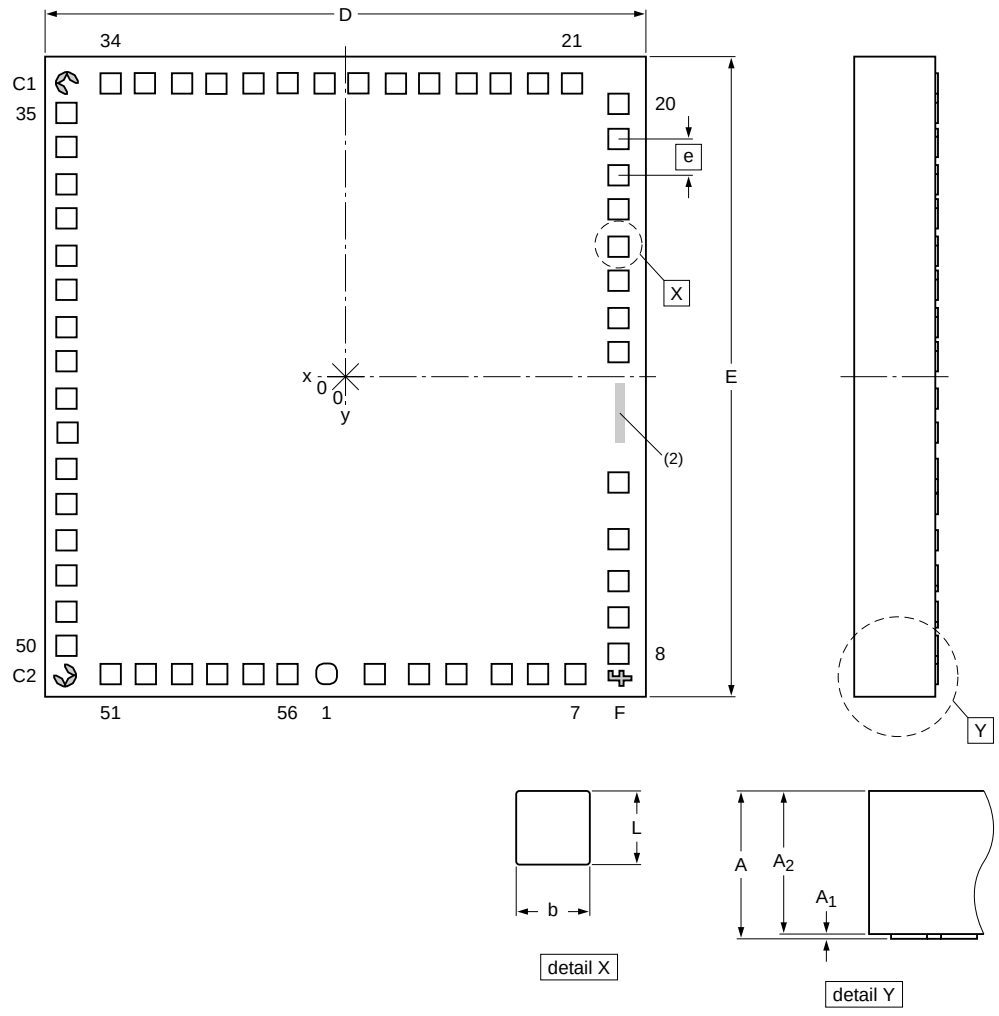
Note
1. Pad size
2. Passivation opening
3. Dimension not drawn to scale
4. Marking code: PC8576C-1

pcf8576cu_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576CU						29-06-02

Fig 36. Bare die outline of PCF8576CU

Bare die; 56 bumps; 3.0 x 2.82 x 0.40 mm **PCF8576CU/2**



Dimensions

Unit		A	A_1	A_2	b	D	E	$e^{(1)}$	L
mm	max							0.610	
	nom	0.398	0.0175	0.380	0.094	2.82	3.00		0.094
	min							0.096	

Note
1. Dimension not drawn to scale
2. Marking code: PC8576C-2

pcf8576cu_2_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8576CU/2						09-06-02

Fig 37. Bare die outline of PCF8576CU/2

Table 22. Pad and bump description for PCF8576CU

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip.

Symbol	Pad	X (μm)	Y (μm)	Description
SDA	1	−74	−1380	I^2C-bus serial data input/output
SCL	2	148	−1380	I^2C-bus serial clock input
$\overline{SYNC}$	3	355	−1380	cascade synchronization input/output
CLK	4	534	−1380	external clock input/output
V_{DD}	5	742	−1380	supply voltage
OSC	6	913	−1380	internal oscillator enable input
A0	7	1087	−1380	subaddress input
A1	8	1290	−1284	subaddress input
A2	9	1290	−1116	subaddress input
SA0	10	1290	−945	subaddress input
V_{SS}	11	1290	−751	logic ground
V_{LCD}	12	1290	−485	LCD supply voltage
BP0	13	1290	125	LCD backplane output
BP2	14	1290	285	LCD backplane output
BP1	15	1290	458	LCD backplane output
BP3	16	1290	618	LCD backplane output
S0	17	1290	791	LCD segment output
S1	18	1290	951	LCD segment output
S2	19	1290	1124	LCD segment output
S3	20	1290	1284	LCD segment output
S4	21	1074	1380	LCD segment output
S5	22	914	1380	LCD segment output
S6	23	741	1380	LCD segment output
S7	24	581	1380	LCD segment output
S8	25	408	1380	LCD segment output
S9	26	248	1380	LCD segment output
S10	27	75	1380	LCD segment output
S11	28	−85	1380	LCD segment output
S12	29	−258	1380	LCD segment output
S13	30	−418	1380	LCD segment output
S14	31	−591	1380	LCD segment output
S15	32	−751	1380	LCD segment output
S16	33	−924	1380	LCD segment output
S17	34	−1084	1380	LCD segment output
S18	35	−1290	1243	LCD segment output
S19	36	−1290	1083	LCD segment output
S20	37	−1290	910	LCD segment output
S21	38	−1290	750	LCD segment output
S22	39	−1290	577	LCD segment output

Table 22. Pad and bump description for PCF8576CU

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip.

Symbol	Pad	X (μm)	Y (μm)	Description
S23	40	–1290	417	LCD segment output
S24	41	–1290	244	LCD segment output
S25	42	–1290	84	LCD segment output
S26	43	–1290	–89	LCD segment output
S27	44	–1290	–249	LCD segment output
S28	45	–1290	–422	LCD segment output
S29	46	–1290	–582	LCD segment output
S30	47	–1290	–755	LCD segment output
S31	48	–1290	–915	LCD segment output
S32	49	–1290	–1088	LCD segment output
S33	50	–1290	–1248	LCD segment output
S34	51	–1083	–1380	LCD segment output
S35	52	–923	–1380	LCD segment output
S36	53	–750	–1380	LCD segment output
S37	54	–590	–1380	LCD segment output
S38	55	–417	–1380	LCD segment output
S39	56	–257	–1380	LCD segment output

Table 23. Alignment marks

Symbol	X (μm)	Y (μm)
C1	–1290	1385
C2	–1295	–1385
F	1305	–1405

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information

17.1 Tray information

Tray information for the PCF8576CU and PCF8576CU/2 is shown in Figure 38, Figure 39 and Table 24.

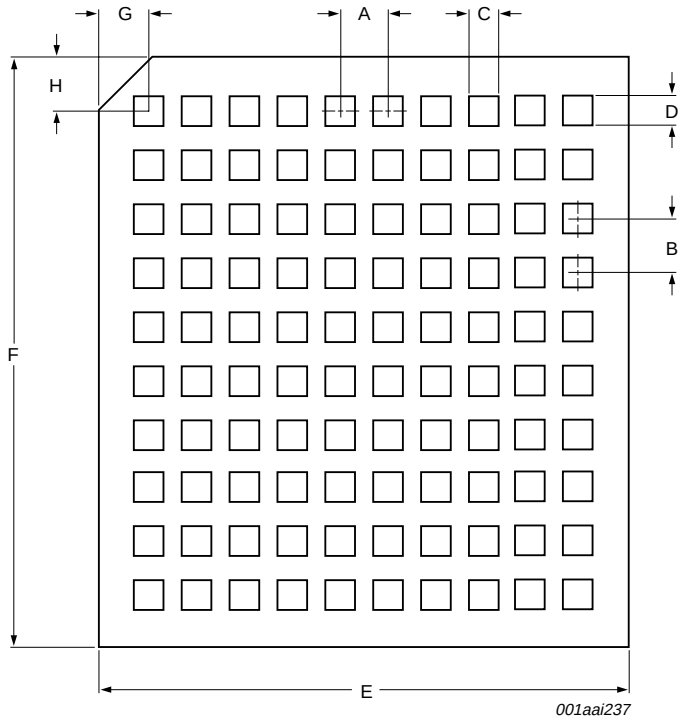


Fig 38. Tray details

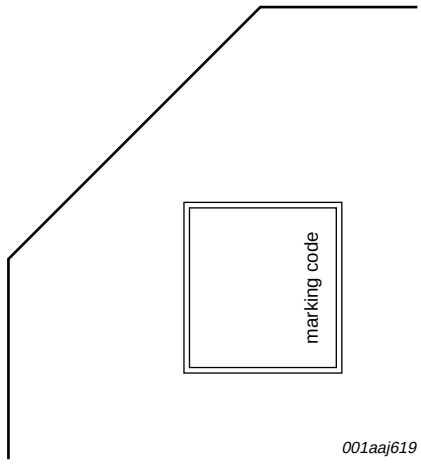


Fig 39. Tray alignment

Table 24. Tray dimensions

Symbol	Description	Value
A	pocket pitch; x direction	5.59 mm
B	pocket pitch; y direction	6.35 mm
C	pocket width; x direction	3.22 mm
D	pocket width; y direction	3.50 mm

Table 24. Tray dimensions

Symbol	Description	Value
E	tray width; x direction	50.67 mm
F	tray width; y direction	50.67 mm
G	cut corner to pocket 1,1 center	5.78 mm
H	cut corner to pocket 1,1 center	6.29 mm
J	tray thickness	3.94 mm
K	tray cross section	1.76 mm
L	tray cross section	2.46 mm
M	pocket depth	0.89 mm
x	number of pockets; x direction	8
y	number of pockets; y direction	7

17.2 Film frame carrier information

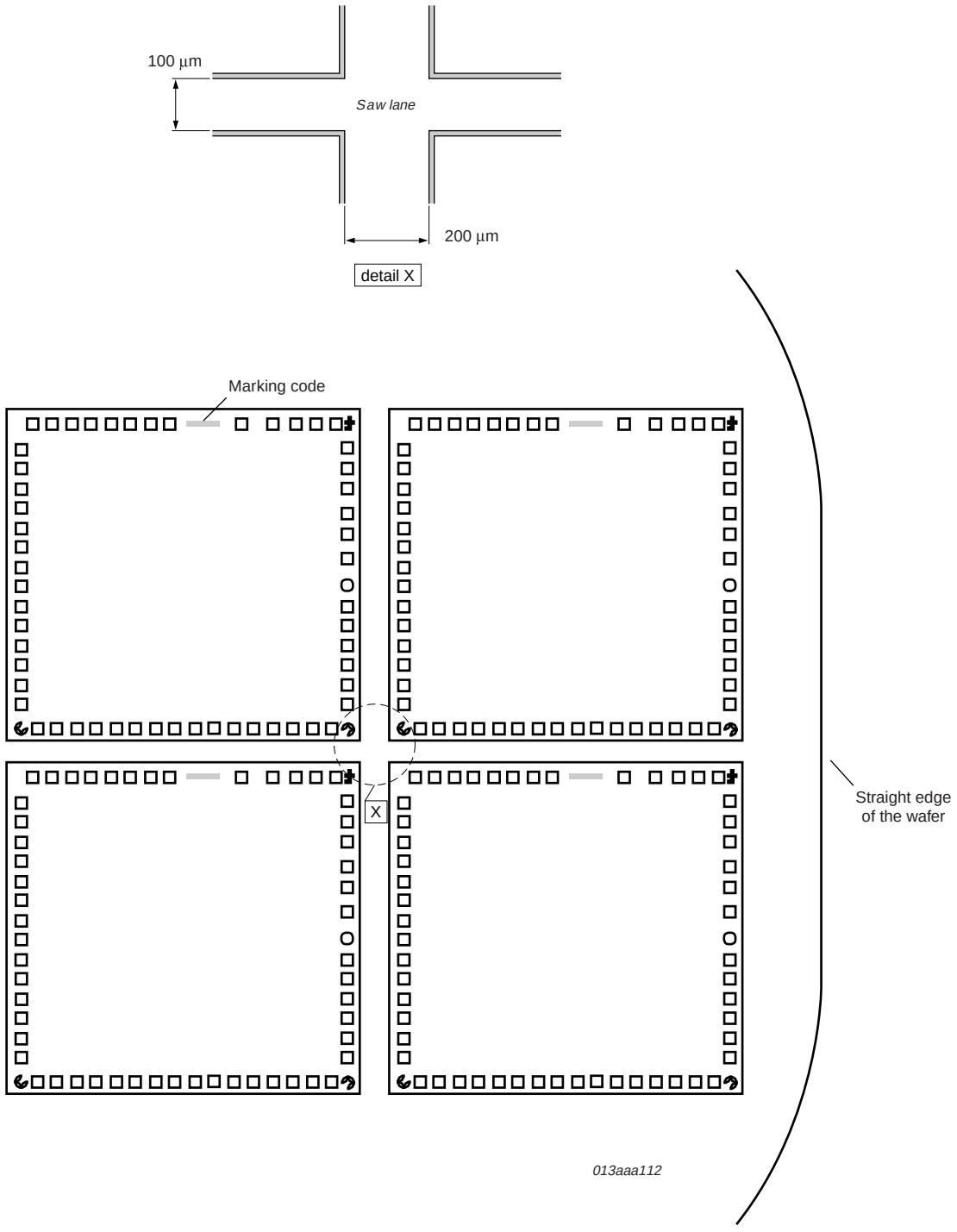


Fig 40. Layout of wafer on film frame carrier of PCF8576CU/10

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 41) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 25 and 26

Table 25. SnPb eutectic process (from J-STD-020C)

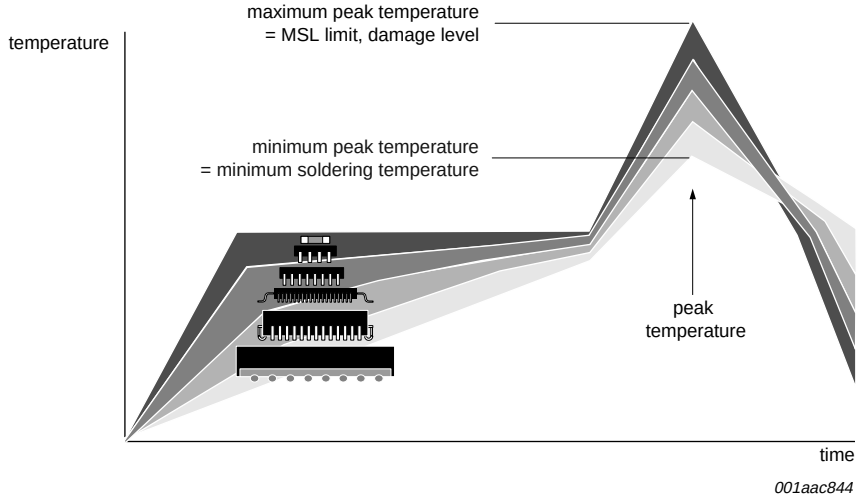
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 26. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 41.



MSL: Moisture Sensitivity Level

Fig 41. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 27. Abbreviations

Acronym	Description
DC	Direct Current
FFC	Film Frame Carrier
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial Clock Line
SDA	Serial Data Line
SMD	Surface Mount Device

20. Revision history

Table 28. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8576C_9	20090709	Product data sheet	-	PCF8576C_8
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Symbols updated and checked with NXP Symbols Library • Changed values in limiting values table (see Table 18) from relative to absolute values • Added TT type • Added bare die outline drawings • Added FFC information • Rewritten chapter 7.3 (see Section 7.3)			
PCF8576C_8	20041122	Product specification	-	PCF8576C_7
PCF8576C_7	20011002	Product specification	-	PCF8576C_6
PCF8576C_6	19980730	Product specification	-	PCF8576C_5
PCF8576C_5	19971114	Product specification	-	PCF8576C_4
PCF8576C_4	19970402	Product specification	-	PCF8576C_3
PCF8576C_3	19970203	Product specification	-	PCF8576C_2
PCF8576C_2	19961209	Product specification	-	PCF8576C_1
PCF8576C_1	19950630	Product specification	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

23. Contents

For more information, please visit: http://www.nxp.com
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