

AN11502

BFU590Q ISM 866 MHz PA design

Rev. 1 — 16 June 2014

Application note

Document information

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| Abstract | This document describes an ISM Frequency PA design on BFU590Q Starter kit |
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1. Abstract

In this application note an ISM band (industrial, scientific and medical) PA design using a BFU590Q transistor from NXP latest wideband transistor range is described. It shows the design, simulation and implementation phases. Together with measurement results, parameters measured over temperature are shown.

The application note (AN) can be a starting point for new design(s), and/or derivative designs.

2. Introduction

The BFU500 transistor family is designed to meet the latest requirements on high frequency applications (up to approximately 2 GHz) such as communication, automotive and industrial equipment.

As soon as fast, low noise analogue up to medium power signal processing is required, combined with medium to high voltage swings the BFU500 transistors are the perfect choice. Due to the high gain at low supply current those types can also be applied very well in battery powered equipment.

Compared to previous Philips / NXP transistor generations and competitor products' improvements on gain, noise and thermal properties are realized. BFU500 transistors are available in various packages.

The transistors are promoted with a full promotion package, called "starter kits" (one kit type per package-type). Those kits include two PCB's (one with grounded emitter, one with emitter degeneration provision), RF connectors, transistors and simulation model parameters required to perform simulations. See the overview of available starter kits in the table below.

Table 1. Customer evaluation kits

| | Basic type | Customer evaluation kits |
|---|------------------------------|---|
| 1 | BFU520W, BFU530W, BFU550W | OM7960, starter kit for transistors in SOT323 package |
| 2 | BFU520A, BFU530A, BFU550A | OM7961, starter kit for transistors in SOT23 package |
| 3 | BFU520, BFU530, BFU550 | OM7962, starter kit for transistors in SOT143 package |
| 4 | BFU520X, BFU530X, BFU550X | OM7963, starter kit for transistors in SOT143X package |
| 5 | BFU520XR, BFU530XR, BFU550XR | OM7964, starter kit for transistors in SOT143XR package |
| 6 | BFU580Q, BFU590Q | OM7965, starter kit for transistors in SOT89 package |
| 7 | BFU580G, BFU590G | OM7966, starter kit for transistors in SOT223 package |

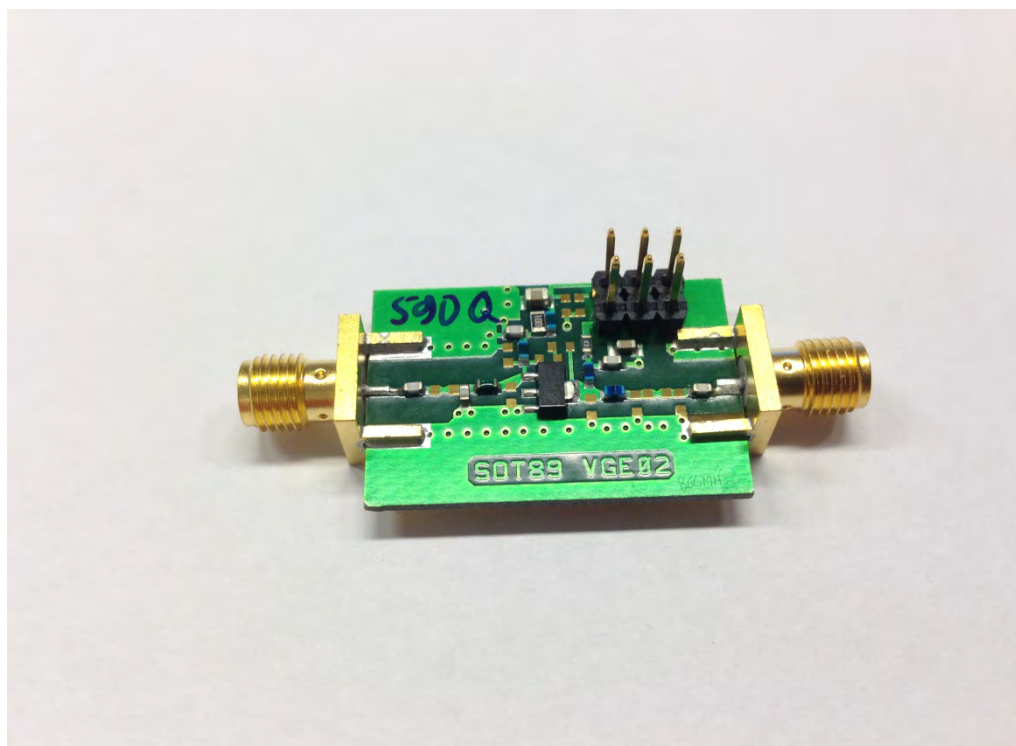


Fig 1. BFU590Q evaluation boards

3. Requirements

The demonstrator circuit is designed to show the BFU590Q capabilities for a 866 MHz ISM PA with strong focus on best possible efficiency.

The goal of the demonstrator circuit was to design a PA optimized for the ISM band meeting following requirements:

| | |
|--------------------|---------------------------------|
| Supply Voltage: | 8 Volts nominal |
| Quiescent current: | 0 - 10mA at ambient temperature |
| Gain: | approx. 10dB |
| P1dB: | >26dBm |
| Input Return-Loss: | >10dB |
| Efficiency: | >55% |

The design is aimed at low BOM cost and small PCB area, inductors are SMD types (preferable low cost multilayer types) to enable simple tuning to other frequency bands.

4. Design considerations

Power amplifiers are critical components in wireless systems. They consume a substantial percentage of the total power.

Design goals for a power amplifier can be the following:

- High output power for given dissipation budget
- High gain. (having less stages, less material and lower cost)

- High efficiency (saving energy)
- Low distortion (having a linear system and reducing unwanted spurious emissions)
- Good stability (under given circumstances)

In order to achieve maximum power, high efficiency and Gain (close to the maximum available gain), the output impedance has to be close to the optimum loadline.

Designing for maximum output power and efficiency, will compromise for example the gain and input return loss, but this is assumed to be acceptable.

At any time the circuit should be stable, hence during the design phase the K-factor needs to be observed carefully.

5. Design approach

The design starts in the simulation phase, applying the Mextram Model (available at <http://www.nxp.com>). Agilent "Advanced Design System" (ADS) was used for this but other simulation software packages should give equal results. Spice / Gummel Poon models are also available but may give less reliable results in nonlinear performance (P1dB, IP3 etc).

Once simulation results meet the requirements, the circuit is built on a universal Printed Circuit Board (PCB) and evaluated. If measurement results show significant offset from simulated results, fine tuning is required until required performance is met. To achieve better matching between simulations and measurements, the PCB parasitic properties have to be added in the simulation template. Basic knowledge of PA design is assumed, see literature.

Following blocks of passive components can be identified:

- 1) passives for DC biasing
- 2) passives set up collector load
- 3) passives for input matching
- 4) passives required to ensure stable operation

5.1 Simulation steps

Following simulation / design approach can be useful:

- 1) Configure the DC bias set-up, ensuring the I_{cc} is set around desired value.
- 2) Configure the collector load circuit and output matching circuitry, optimizing the output Return Loss (RL).
- 3) Check stability on the bench afterwards.
- 4) Configure the input matching for maximum gain and acceptable input return loss.
- 5) Check stability on the bench afterwards.

Assumptions:

- Realistic passives are used by applying Murata design kit (0603/0805)
- PCB tracks represented by strip-lines

5.2 Implementation / evaluation steps

Following implementation / evaluation steps have been executed:

- 1) Implement simulated design on universal PCB.
- 2) Evaluate PA on output power / efficiency / Gain / matching / Stability at ambient temperature.
- 3) Fine tune passives if required.
- 4) In case significant differences between simulations and measured results are observed, add or modify parasitic properties in the simulation template.
- 5) Measure PA design on RF parameters over temperature.

5.3 Setting up the DC bias circuit

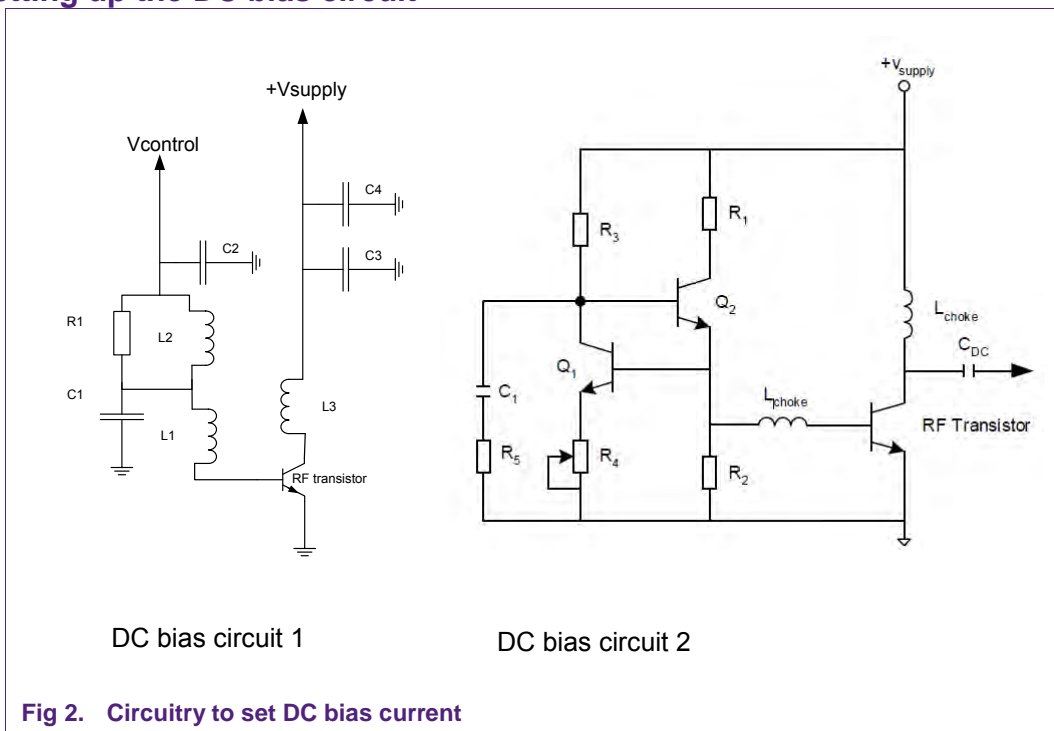


Fig 2. Circuitry to set DC bias current

In a class A amplifier, it is custom to stabilize the operating point by means of an emitter and base resistor. In a RF power amplifier, however, it is preferable to ground the emitter to obtain maximum power gain.

Circuit 1 shows the basic circuit of the bias circuit of an RF power amplifier. Biasing de-coupling networks are designed to present high impedance in the RF band and to have a low impedance in the low frequency band.

Due to proper choice of RF chokes (L1,L2) and bypass capacitors (C1,C2,C3,C4), parasitic oscillations can occur far below the working frequency. The RF chokes combined with the parasitic feedback capacitor (Ccb) can result in a Hartley type of oscillator as shown below. In order to avoid oscillation the inductance values of the chokes should fulfill the condition given in figure 3.

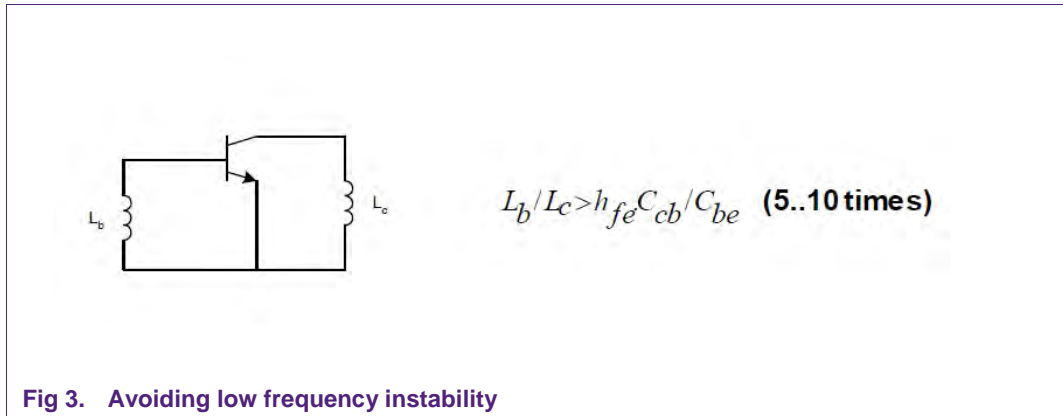


Fig 3. Avoiding low frequency instability

The formula in figure 3 gives the ratio between the collector coil and base coil to avoid low frequency instability.

It is good practice to de-couple the supply points with large capacitors (uF range) to eliminate transients and interactions between other system components on the same supply rail.

To avoid LF instability this should not be inserted at the RF de-coupling points. Instead a LF choke (L_2) is added to isolate the RF and supply de-coupling points shunted by a resistor (R_1).

Circuit 2 shows an example of the class-AB bias circuit. It is required to have a constant V_{BE} , a low output resistance, temperature compensation and low power consumption (efficiency)

The bias circuit shown here has large negative feedback. If the base current of the RF power transistor increases the output voltage of the bias circuit will decrease slightly causing the collector current of Q1 to decrease and its collector voltage to increase, counteracting the drop in output voltage.

Q1 should have a V_{BE} level which is lower than that of the RF power transistor. R_4 compensates for the difference between these two values and used to set the bias level.

R_1 is incorporated to protect Q2 in case of short circuit in the power transistor.

R_2 is a preloading resistor used to reduce the base current variation.

This circuit can develop parasitic oscillation near 1MHz with highly capacitive loads (such as the base supply bypass capacitors). The series combination C1-R5 can prevent this.

In this AN the circuit on the left has been implemented by using an additional power supply to set the bias current. The circuit on the right is an example of how a bias circuit can be build up.

5.4 Setting up the Simulation circuit in ADS

The configuration below is used for the simulation by ADS. It's a basic circuit amplifier available in the ADS design guide: Amplifier / 1-Tone Nonlinear Simulations / Spectrum, gain, Harmonic Distortion.

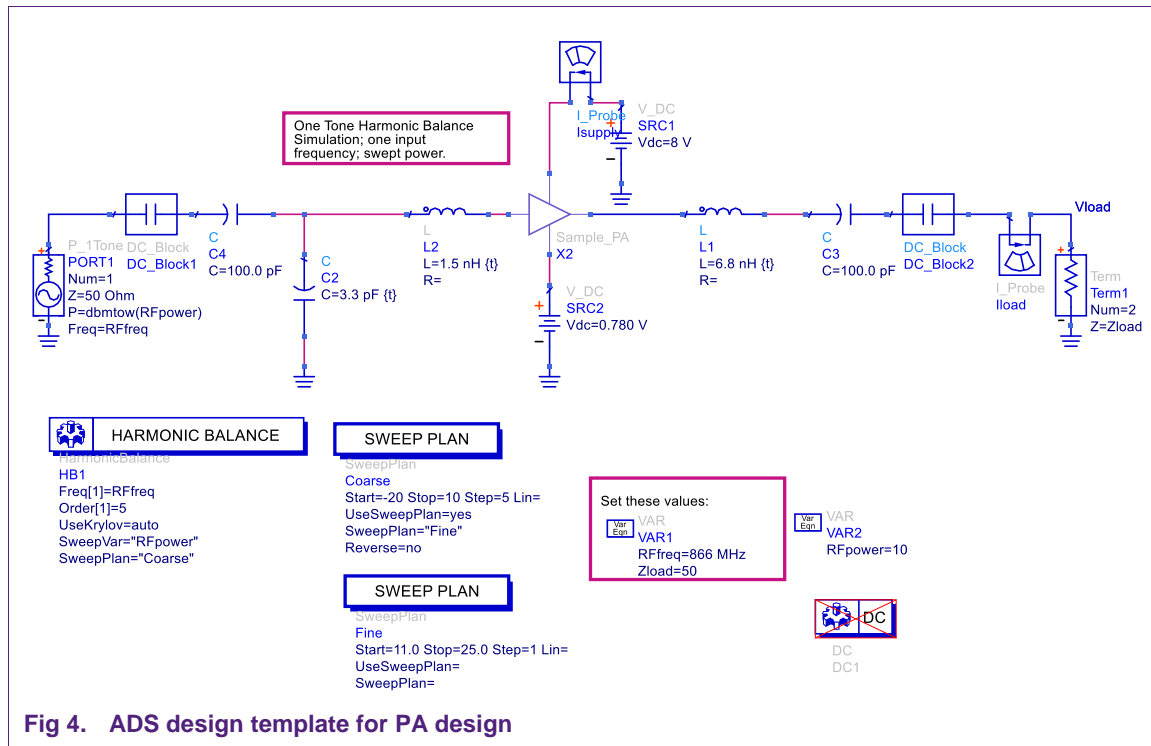


Fig 4. ADS design template for PA design

The circuit shows the possibility to choose any frequency, impedance, power range.

5.5 Setting up the collector load

The design has been concentrated to have maximum 1dB compression at 8V power supply having high efficiency and gain.

The load impedance is:
$$R_L = \frac{(V_{supply} - V_{saturation})^2}{2P_{out}}$$

For 0.5W output power the load impedance should be close to 50 Ohm.

Two ways to calculate efficiency:

Efficiency:
$$\eta_c = \frac{P_{output}}{P_{dc}}$$

Power added Efficiency:
$$\eta_a = \frac{(P_{output} - P_{input})}{P_{dc}} = \eta_c \frac{1}{(1 - \frac{1}{G_p})}$$

In this AN the η_c will be used.

The components C2, L2, C1 and L1 (see figure 4) have been used to tune the maximum 1dB compression power, efficiency input return loss and gain in the required frequency band of 433MHz. The bias coil to the base of the transistor was set to 470nH and for the collector was set to 18nH. This ratio meets the low frequency stability rule see figure 3.

There are tradeoffs to make to meet the 1dB compression target:

- Output collector coil (to supply): 18nH. Higher value will reduce the efficiency, a lower value will reduce the gain.
- Output series inductor: 6.8nH. Higher value will decrease the 1dB compression but will improve the efficiency

- The input inductor (L2) and capacitor (C2) can be set to match the input for gain and input return loss.

When going one level deeper in the PA design, the transistor template with it's bias and collector coil is shown, see figure 5.

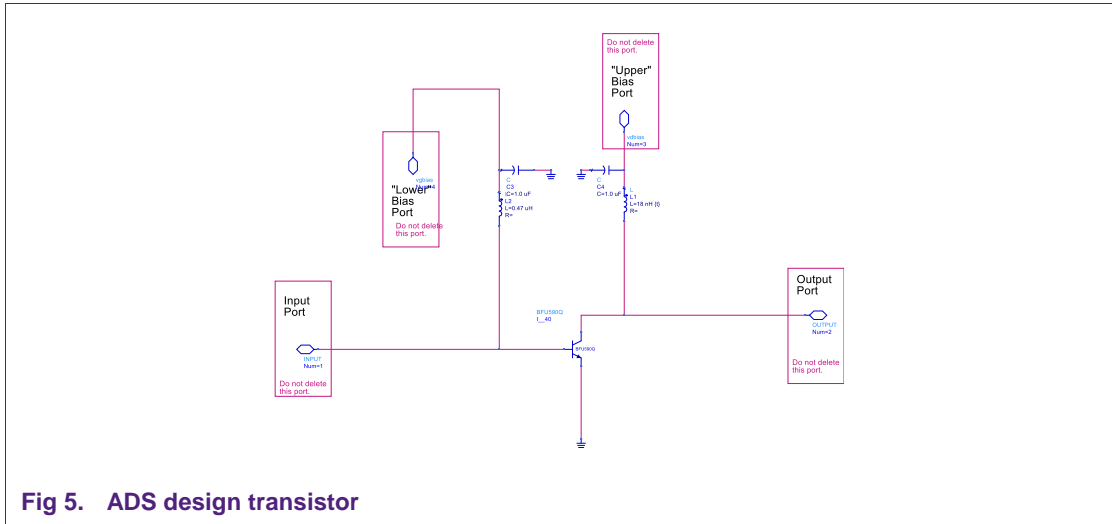


Fig 5. ADS design transistor

The circuit below shows the Idc settings of the circuit:

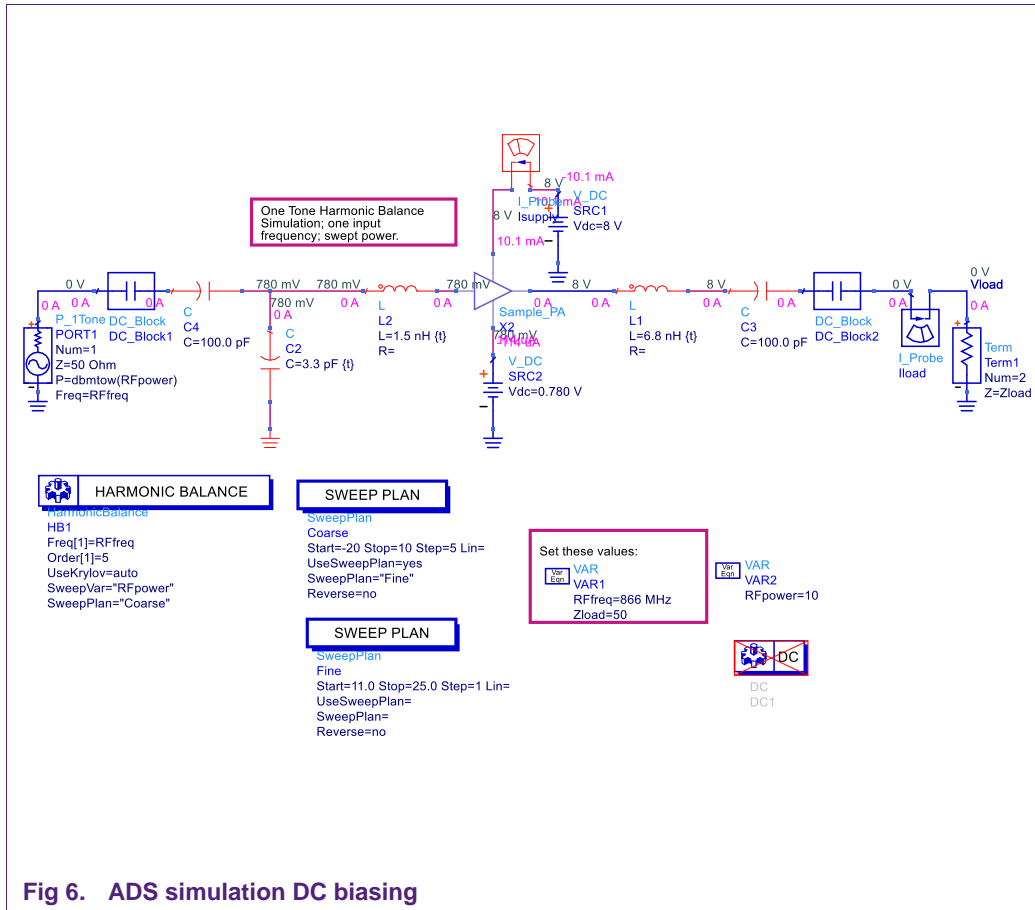


Fig 6. ADS simulation DC biasing

By applying ~0.78V bias at the base of the transistor, the collector current is ~10mA.

Harmonic balance simulation template is used, results to the 5th order are shown below:

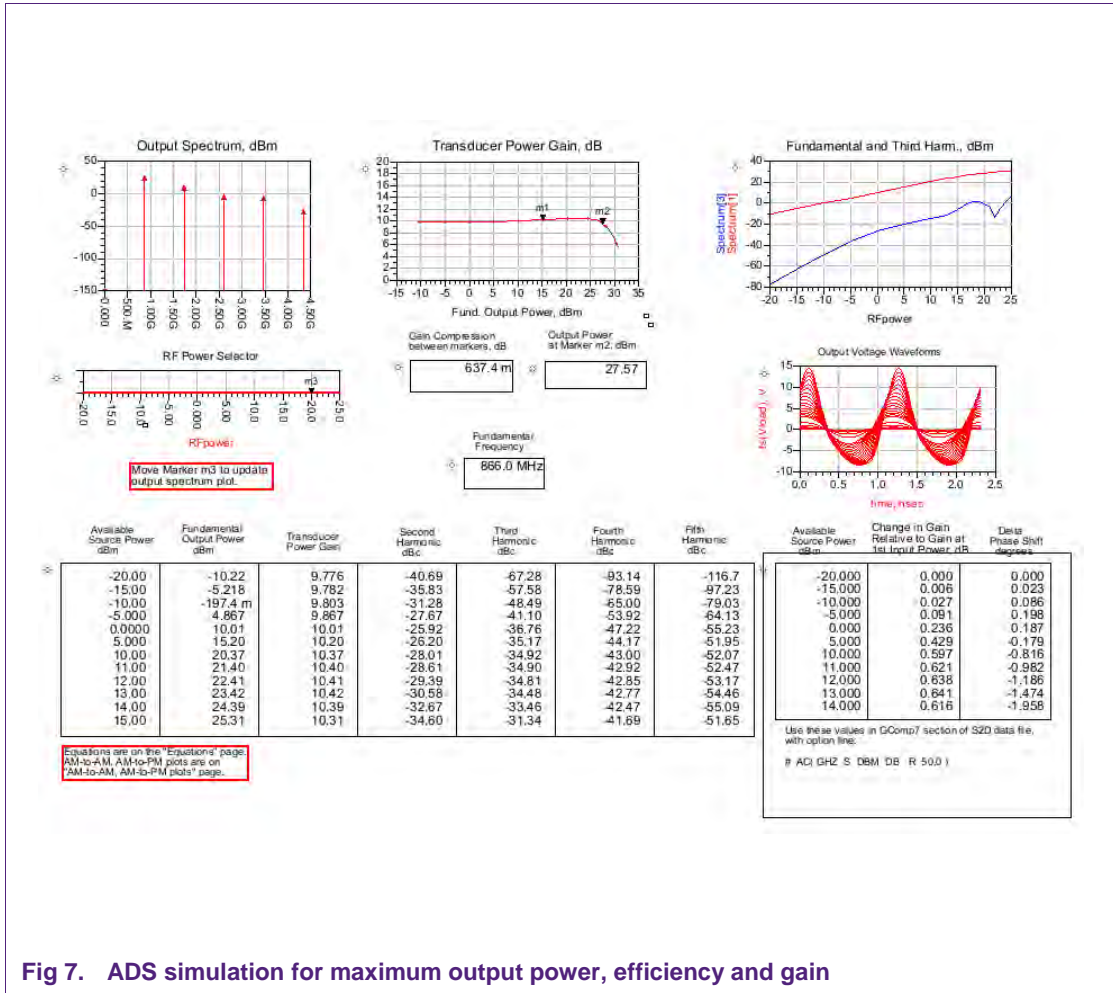


Fig 7. ADS simulation for maximum output power, efficiency and gain

The simulation gives a 1dB compression of 28dBm. The gain is 10dB for low output power. The gain increases slightly to 10.5dB just before reaching the 1dB compression. The harmonic content of the output signal is also given in the table.

In the graph below the Idc over output power is shown.

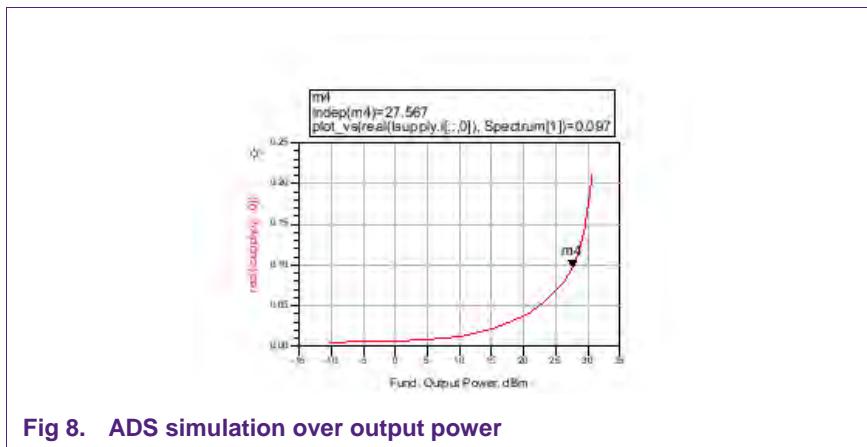


Fig 8. ADS simulation over output power

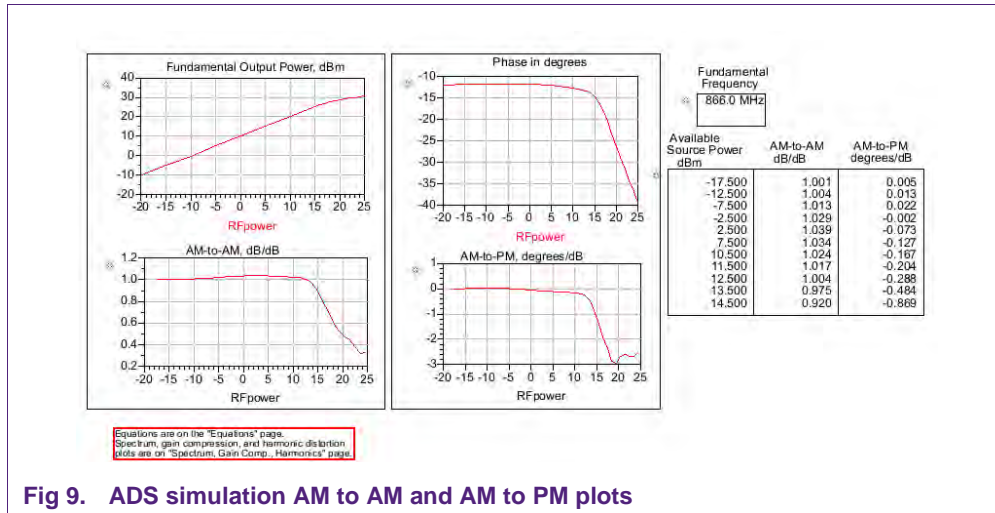


Fig 9. ADS simulation AM to AM and AM to PM plots

Natural behavior of a class AB circuit is the I_{dc} increase over output power. At 1dB compression (28dBm) the $I_{dc} = 133\text{mA}$. Dissipated power in that situation is $8 \times 0.133 = 1.06\text{W}$ which gives an efficiency of 59%.

5.6 Definition of input / source matching circuit

By tuning C2 and L2 the input RF match and gain can be set, results of the simulation see figure 10.

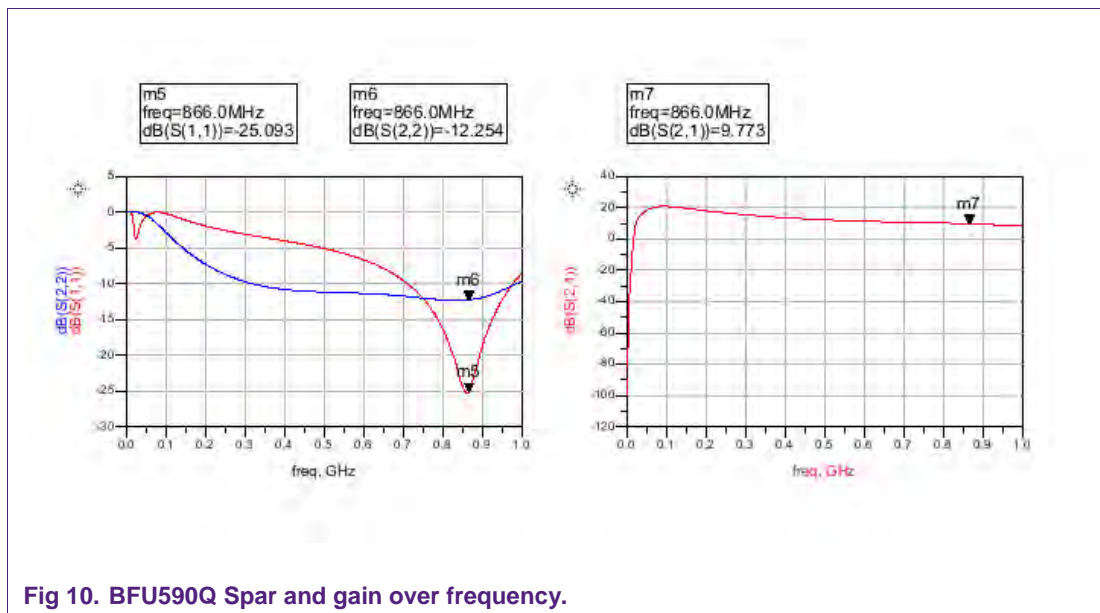


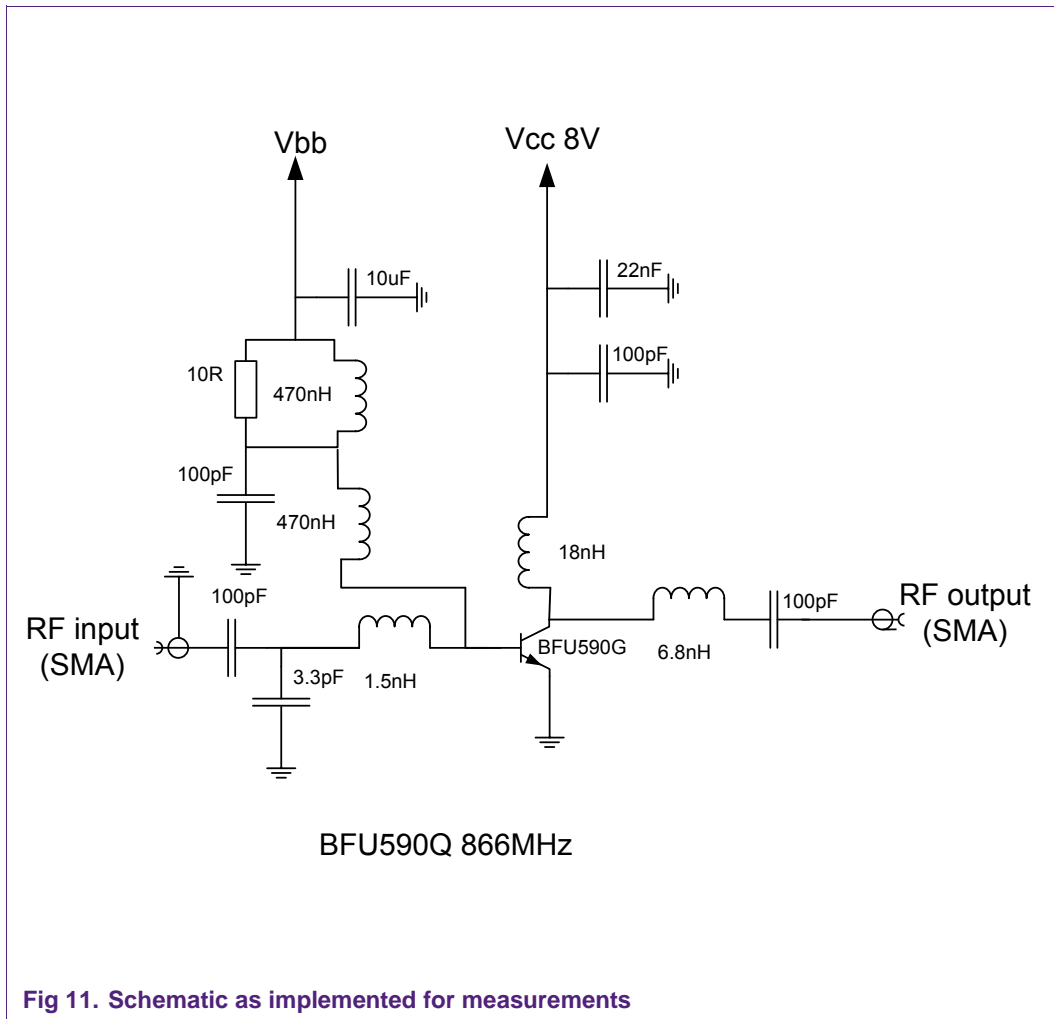
Fig 10. BFU590Q Spar and gain over frequency.

S-parameters and gain over frequency.

6. Application circuit

The circuit diagram of the evaluation board is shown in Fig 11 PCB schematic.

6.1 BFU590Q 866 MHz ISM PA schematic



6.2 BFU590Q 866 MHz ISM PA PCB drawing

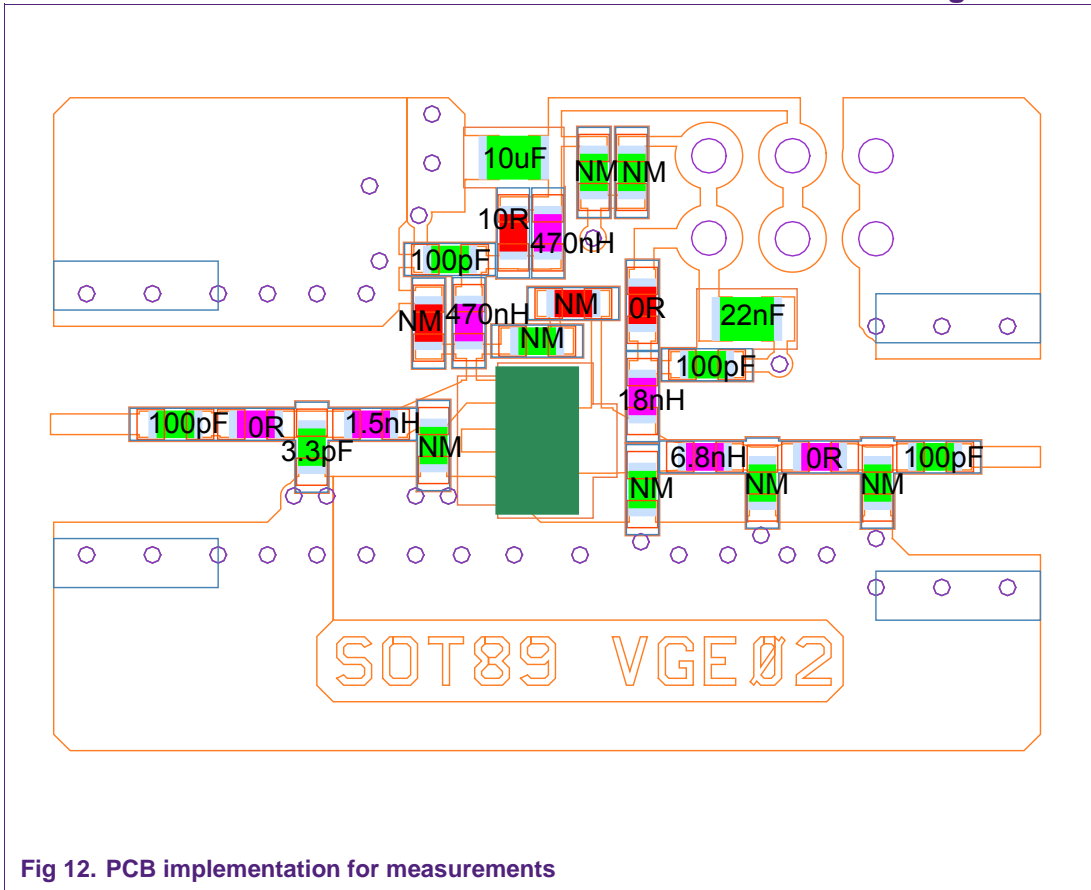


Fig 12. PCB implementation for measurements

Remarks:

0R = SMD jumper

NM = component not mounted.

This layout, as delivered with the Starter kit, accommodates the possibility to implement the biasing as shown in the ADS schematics.

6.3 PCB properties, layer stack

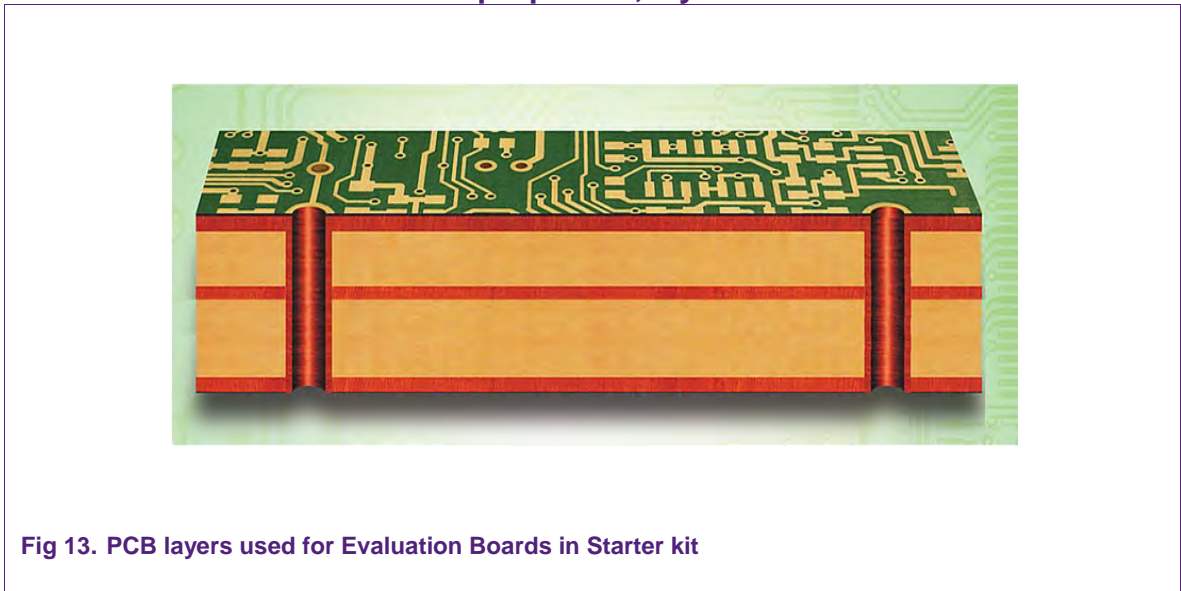


Fig 13. PCB layers used for Evaluation Boards in Starter kit

6.4 Typical PA evaluation board results

Table 2. Typical results measured on the evaluation boards

Operating Frequency is $f = 866$ MHz unless otherwise specified; Temp = 25 °C

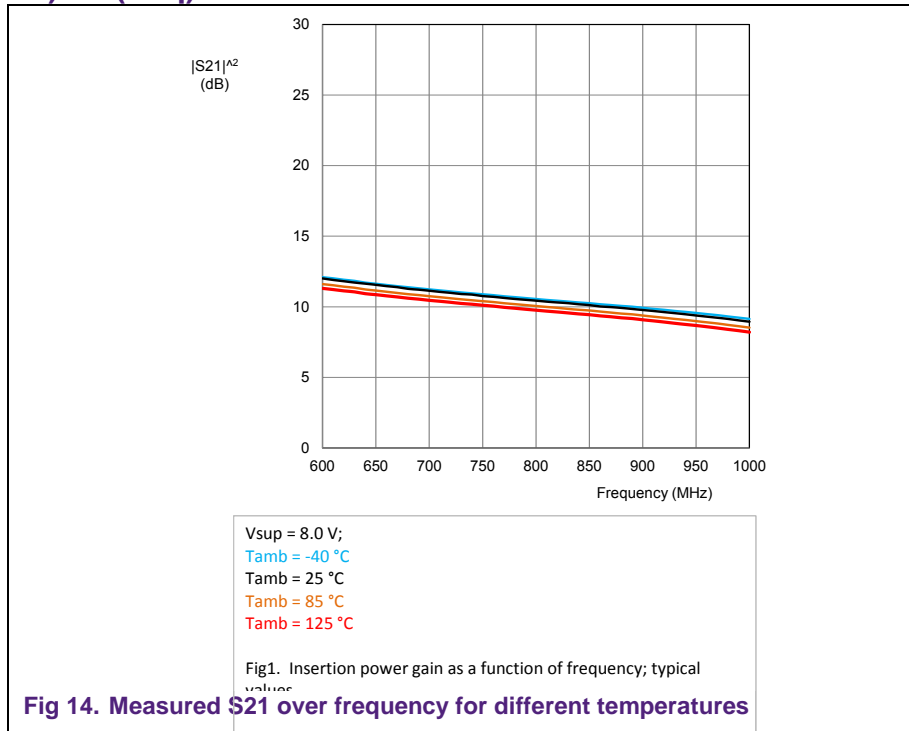
| Parameter | Symbol | EVB | Unit | Remarks |
|---------------------|-----------|-----|------|---------|
| Supply Voltage | V_{CC} | 8 | V | |
| Supply Current | I_{CC} | 100 | mA | |
| Power Gain | G_p | 10 | dB | |
| Input Return Loss | RL_{in} | -12 | dB | |
| Output Power (P1dB) | P1dB | 27 | dBm | |
| Efficiency | η_c | 55 | % | |

Table 3. Bill Of Materials

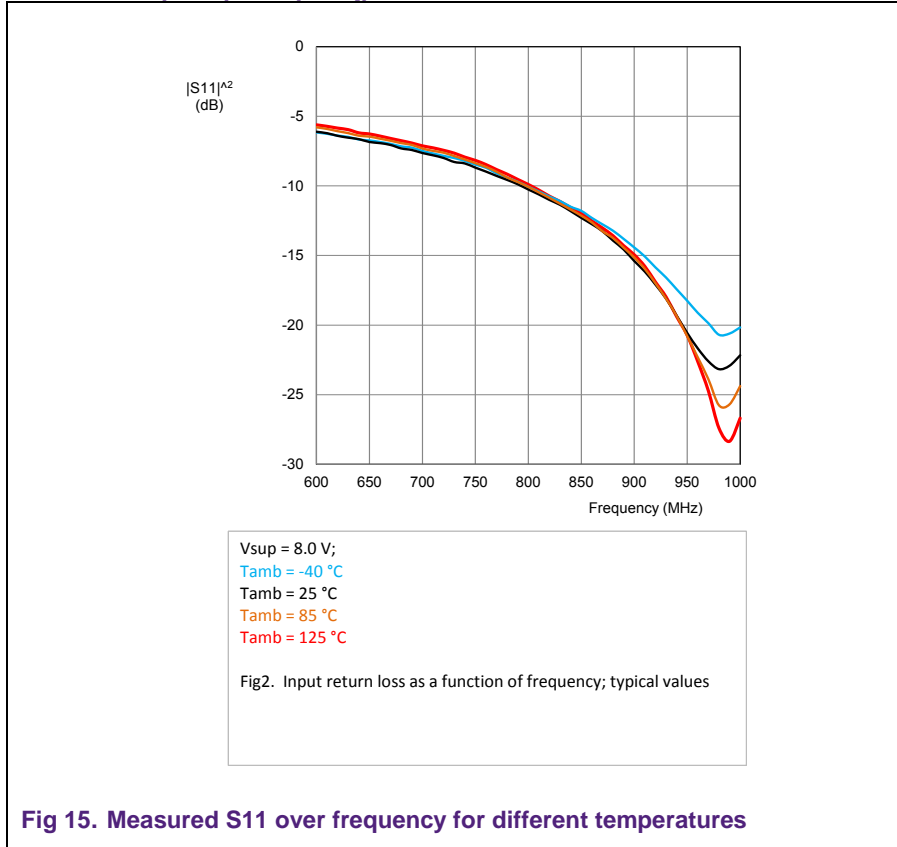
| Value | Description | Footprint | Manufacturer |
|-------------|-------------|-----------|--------------------|
| BFU590Q | Transistor | SOT89 | NXP Semiconductors |
| 100 pF | Capacitor | 0603 | Various |
| 3.3 pF | Capacitor | 0603 | Various |
| 100 pF | Capacitor | 0603 | Various |
| 10 uF | Capacitor | 0805 | Various |
| 22 nF | Capacitor | 0805 | Various |
| 100 pF | Capacitor | 0603 | Various |
| 1.5 nH | Inductor | 0603 | Various |
| 470 nH | Resistor | 0603 | Various |
| 470 nH | Inductor | 0603 | Various |
| 18 nH | Inductor | 0603 | Various |
| 6.8 nH | Inductor | 0603 | Various |
| 10 Ω | Resistor | 0603 | Various |

7. Characterization of PA over temperature and supply voltage

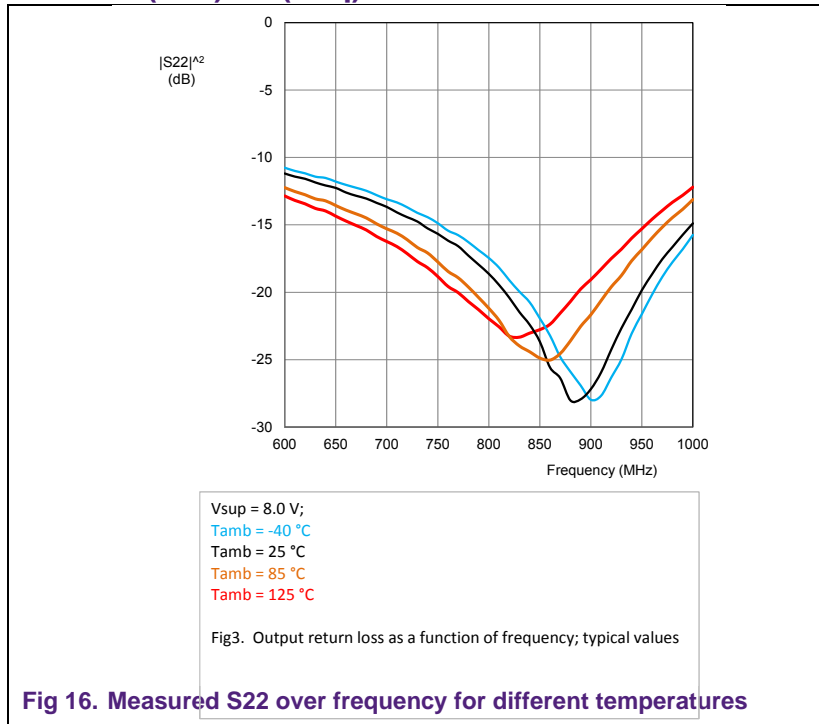
7.1 Gain (S_{21}) = f (freq)



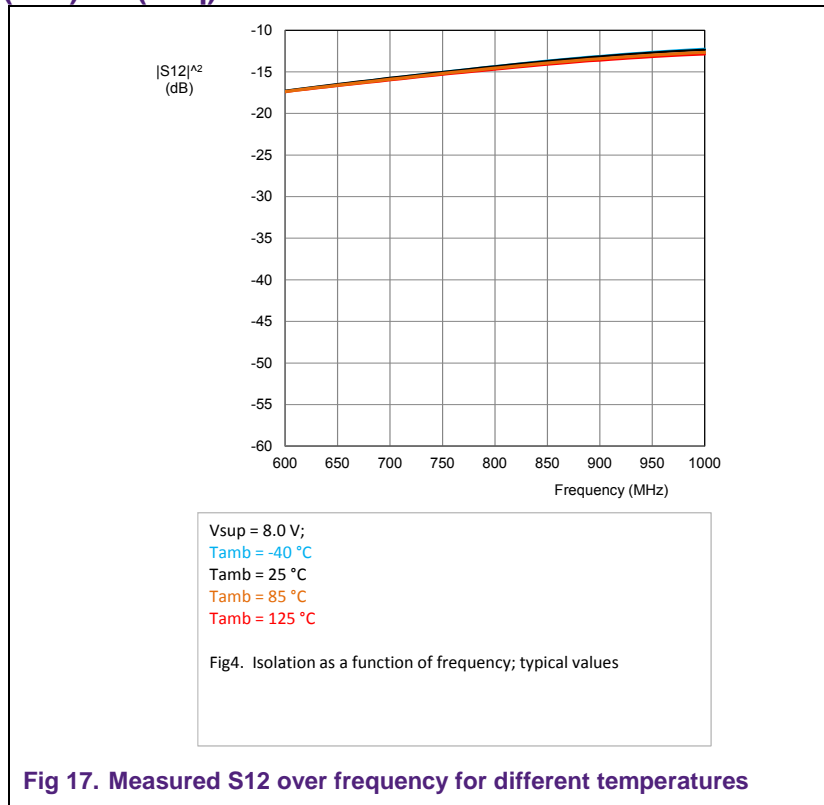
7.2 Input return-loss (S_{11}) = f (freq)



7.3 Output return-loss (S22) = f (freq)

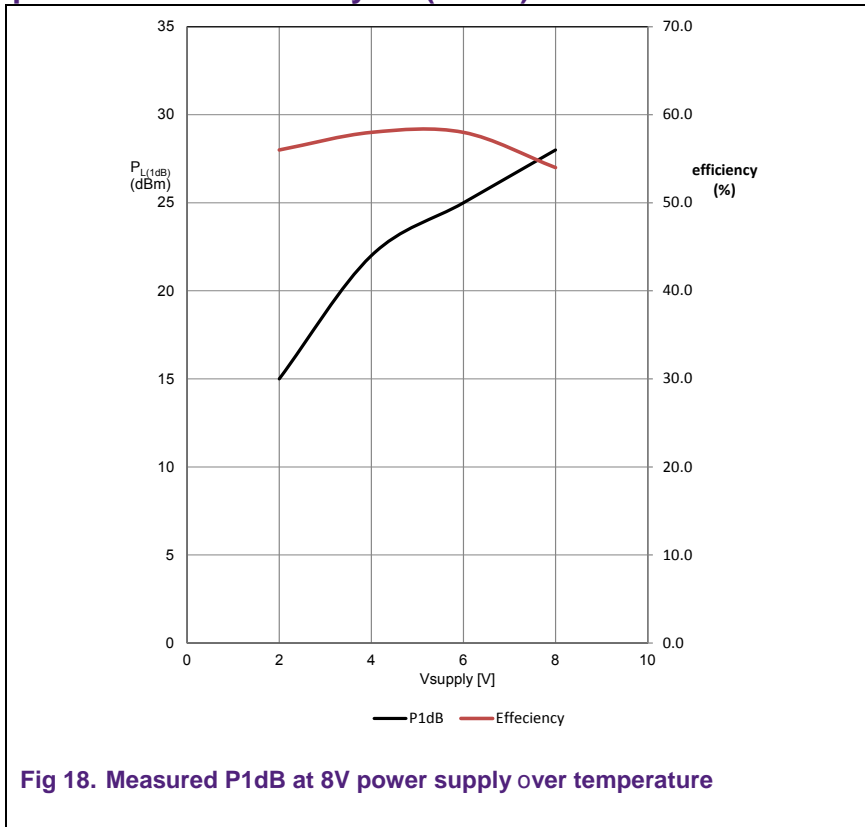


7.4 Isolation (S12) = f (freq)

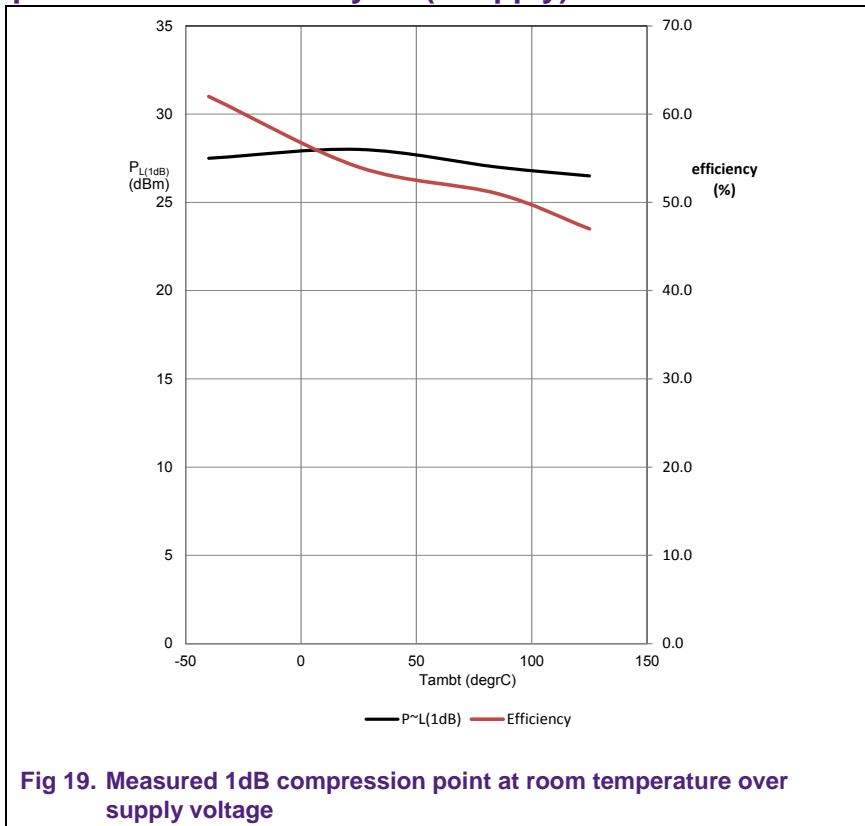


All Sparameters measured at low input power (-40dBm)

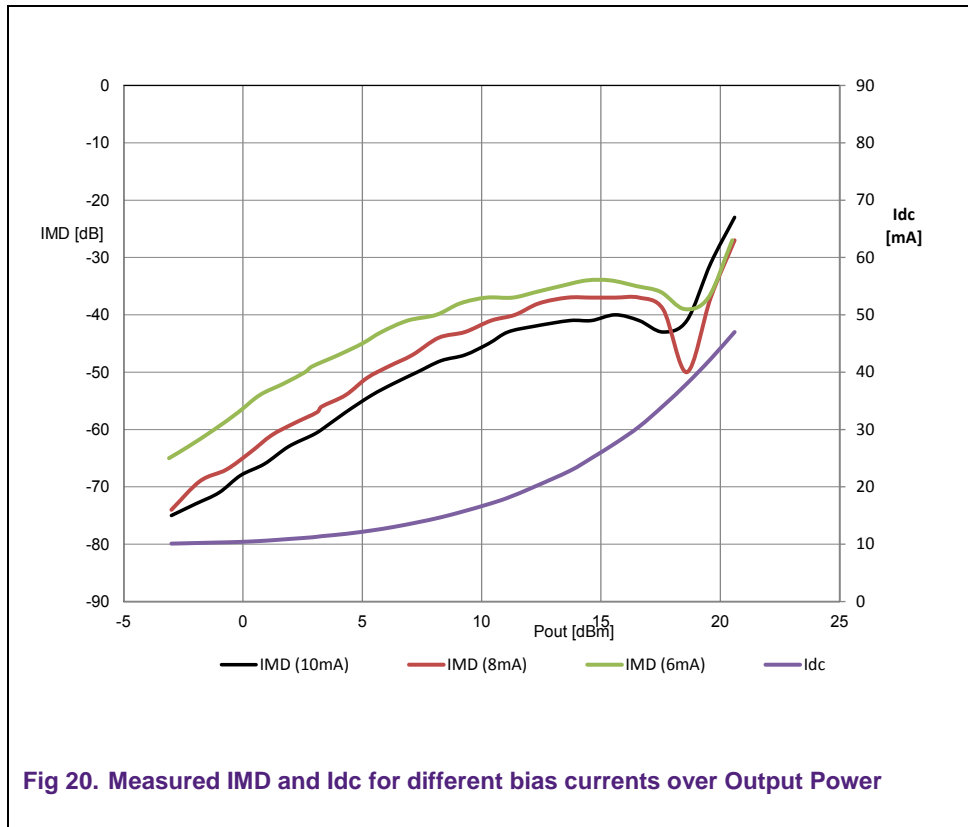
7.5 1dB compression and efficiency = f (Tamb)



7.6 1dB compression and efficiency = f (Vsupply)



7.7 2 tone IMD and $I_{dc} = f(P_{out})$ for 3 bias currents



8. Conclusions / recommendations

With the BFU590Q transistor a 866 MHz PA design can be implemented with a P1dB of about 27dBm and having a good efficiency of about 55%. Gain is 10dB. The circuit can be used as a base for derivative designs, matching to other frequencies can be done by tuning relevant capacitors and inductors.

For improvements on linearity over output level it could be recommended to set the correct DC biasing current.

This PA can be tuned to other frequencies as well. The presented configuration has been designed for a small bandwidth application.

For wideband power amplifiers a feedback is recommended which can be implemented on the existing board.

9. References

BFU590Q datasheet

BFU590Q starter-kit (OM7965) User Manual, UM10772

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