Freescale Semiconductor
Technical Data

Document Number: A2I35H060N
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RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A2I35H060NR1
A2I35H060GNR1

3400–3800 MHz, 10 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

The A2I35H060N wideband integrated circuit is an asymmetrical Doherty designed with on-chip matching that makes it usable from 3400 to 3800 MHz. This multi-stage structure is rated for 26 to 32 V operation and covers all typical cellular base station modulation formats.

3500 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 56 mA, I_{DQ2A} = 141 mA, V_{GS1B} = 1.6 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 10 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
3400 MHz	24.0	32.5	–33.4
3500 MHz	24.0	32.4	–37.0
3600 MHz	23.7	31.3	–39.0

Features

- Advanced High Performance In-Package Doherty
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems

TO-270WB-17
PLASTIC
A2I35H060NR1

TO-270WBG-17
PLASTIC
A2I35H060GNR1

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

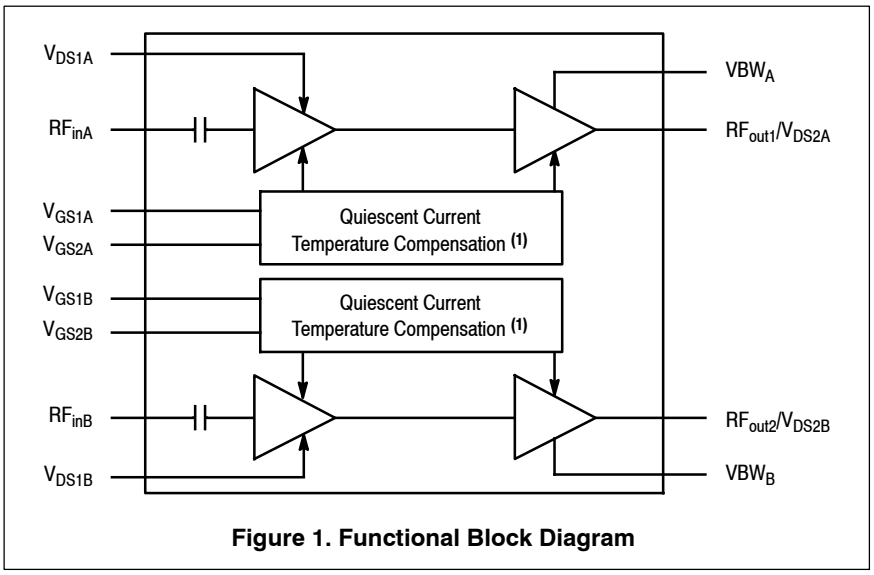
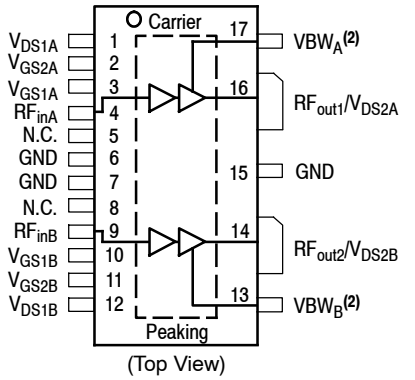


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
2. Device can operate with V_{DD} current supplied through pin 13 and pin 17.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (3,4)	T_J	–40 to +225	°C
Input Power	P_{in}	26	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (4,5)	Unit
Thermal Resistance, Junction to Case Case Temperature 75°C, 10 W Avg., W-CDMA, 3500 MHz Stage 1, 28 Vdc, I_{DQ1A} = 56 mA, V_{GS1B} = 1.6 Vdc, Stage 2, 28 Vdc, I_{DQ2A} = 141 mA, V_{GS2B} = 1.3 Vdc	$R_{\theta JC}$	 7.0 1.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

3. Continuous use at maximum temperature will affect MTTF.
4. MTTF calculator available at http://www.nxp.com/RF/calculators.
5. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 1 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 5 μAdc)	$V_{GS(th)}$	0.6	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 56 mAdc)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = 56 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	7.0	8.9	9.5	Vdc
Carrier Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 2 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 28 μAdc)	$V_{GS(th)}$	0.6	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 141 mAdc)	$V_{GS(Q)}$	—	1.9	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 141 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.0	4.9	5.5	Vdc
Drain–Source On–Voltage (1) (V_{GS} = 10 Vdc, I_D = 360 mAdc)	$V_{DS(on)}$	0.1	0.22	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Peaking Stage 1 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 1 – On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 8 μAdc)	$V_{GS(th)}$	0.6	1.2	1.6	Vdc
Peaking Stage 2 – Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 2 – On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 44 μAdc)	$V_{GS(th)}$	0.6	1.3	1.6	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 360 mAdc)	$V_{DS(on)}$	0.05	0.22	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2,3] (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 56 mA, I_{DQ2A} = 141 mA, V_{GS1B} = 1.6 Vdc. V_{GS2B} = 1.3 Vdc, P_{out} = 10 W Avg., f = 3500 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	23.0	24.6	26.5	dB
Power Added Efficiency	PAE	25.2	29.9	—	%
Adjacent Channel Power Ratio	ACPR	—	–35.9	–30.4	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	46.3	50.6	—	W
Load Mismatch [2] (In Freescale Doherty Characterization Test Fixture, 50 ohm system) I_{DQ1A} = 56 mA, I_{DQ2A} = 141 mA, V_{GS1B} = 1.6 Vdc. V_{GS2B} = 1.3 Vdc, f = 3500 MHz					
VSWR 10:1 at 32 Vdc, 56 W CW Output Power (3 dB Input Overdrive from 47 W CW Rated Power)	No Device Degradation				
Typical Performance [2] (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 56 mA, I_{DQ2A} = 141 mA, V_{GS1B} = 1.6 Vdc, V_{GS2B} = 1.3 Vdc, 3400–3600 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	48	—	W
P_{out} @ 3 dB Compression Point [4]	P3dB	—	65	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 3400–3600 MHz frequency range.)	Φ	—	–23	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point, measured Class AB: I_{DQ1A} = 56 mA, I_{DQ2A} = 141 mA, I_{DQ1B} = 80 mA, I_{DQ2B} = 220 mA)	VBW_{res}	—	140	—	MHz
Quiescent Current Accuracy over Temperature [5] with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1 with 4.7 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2	ΔI_{QT}	 — —	 3.45 1.21	 — —	%
Gain Flatness in 200 MHz Bandwidth @ P_{out} = 10 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.032	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I35H060NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-17
A2I35H060GNR1		TO-270WBG-17

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

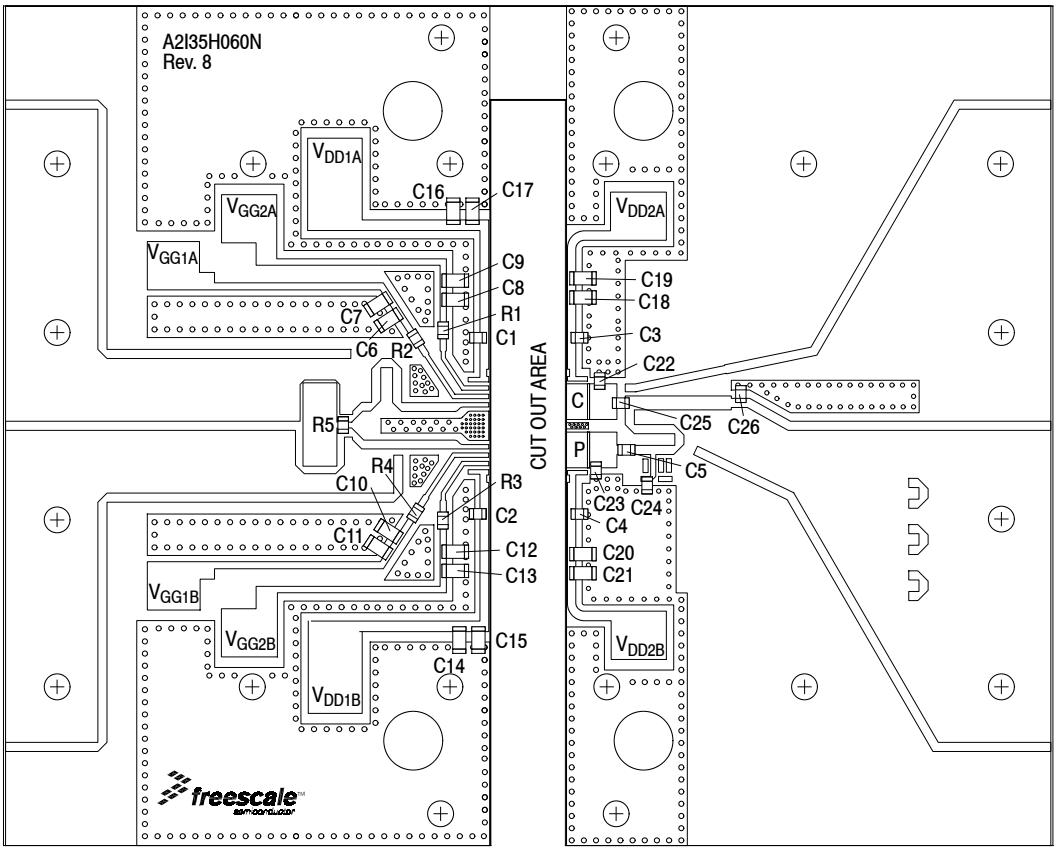
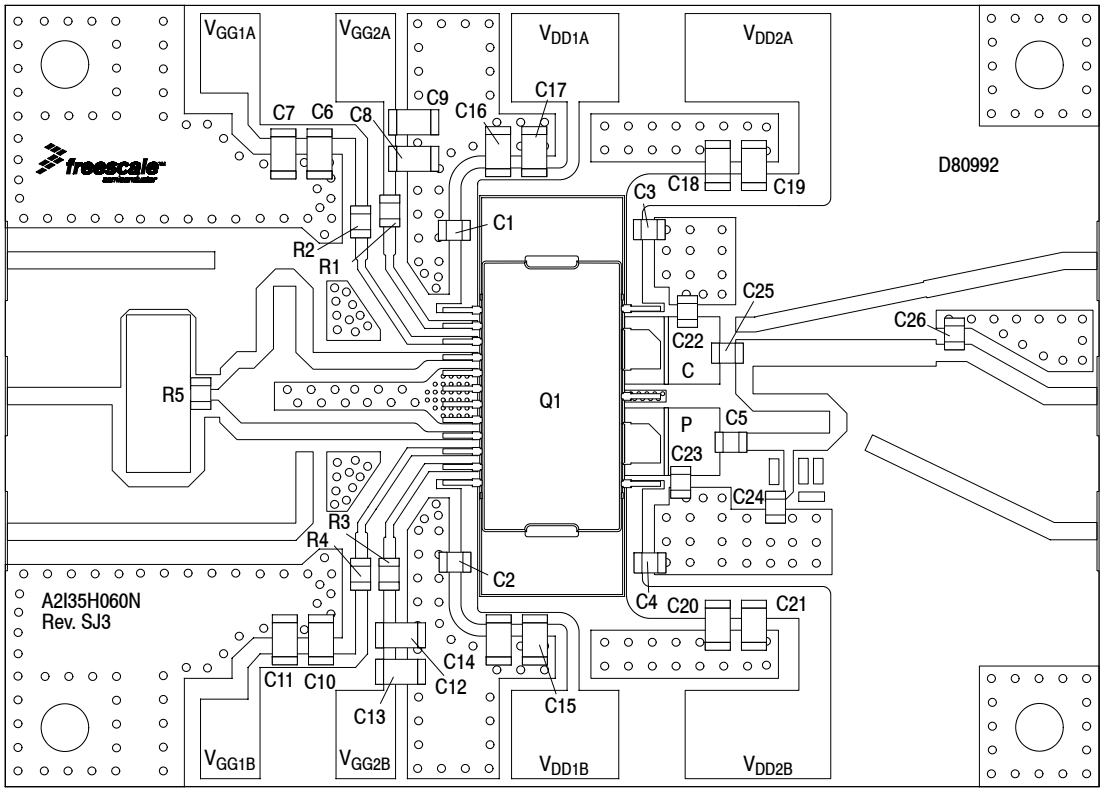


Figure 3. A2I35H060NR1 Production Test Circuit Component Layout — 4.0″ × 5.0″ (10.2 cm × 12.7 cm)

Table 7. A2I35H060NR1 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C6, C8, C10, C12, C14, C16, C18, C20	1 μF Chip Capacitors	GRM31MR71H105KA88K	Murata
C7, C9, C11, C13, C15, C17, C19, C21	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C22	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C23	0.6 pF Chip Capacitor	ATC600F0R6AT250XT	ATC
C24	8.2 pF Chip Capacitor	ATC600F8R2JT250XT	ATC
C25	2.7 pF Chip Capacitor	ATC600F2R7BT250XT	ATC
C26	0.2 pF Chip Capacitor	ATC600F0R2AW250XT	ATC
R1, R2, R3, R4	4.7 kΩ, 1/10 W Chip Resistors	RR1220P−472-D	Susumu
R5	100 Ω, 1/10 W Chip Resistor	RR1220P100-A	Susumu
PCB	Taconic RF35A2, 0.020″, ε_r = 3.66	—	MTL



Note: All data measured in fixture with device soldered to heatsink.

Figure 4. A2I35H060NR1 Characterization Test Circuit Component Layout — 2.0″ × 2.8″ (5.0 cm × 7.0 cm)

Table 8. A2I35H060NR1 Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C6, C8, C10, C12, C14, C16, C18, C20	1 μF Chip Capacitors	GRM31MR71H105KA88K	Murata
C7, C9, C11, C13, C15, C17, C19, C21	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C22	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C23	0.6 pF Chip Capacitor	ATC600F0R6AT250XT	ATC
C24	8.2 pF Chip Capacitor	ATC600F8R2JT250XT	ATC
C25	2.7 pF Chip Capacitor	ATC600F2R7BT250XT	ATC
C26	0.1 pF Chip Capacitor	ATC600F0R1AW250XT	ATC
Q1	RF LDMOS Power Amplifier	A2I35H060NR1	NXP
R1, R2, R3, R4	4.7 kΩ, 1/10 W Chip Resistors	RR1220P-472-D	Susumu
R5	100 Ω, 1/10 W Chip Resistor	RR1220P100-A	Susumu
PCB	Taconic RF35A2, 0.020″, ε_r = 3.66	D80992	MTL

TYPICAL CHARACTERISTICS — 3400–3600 MHz

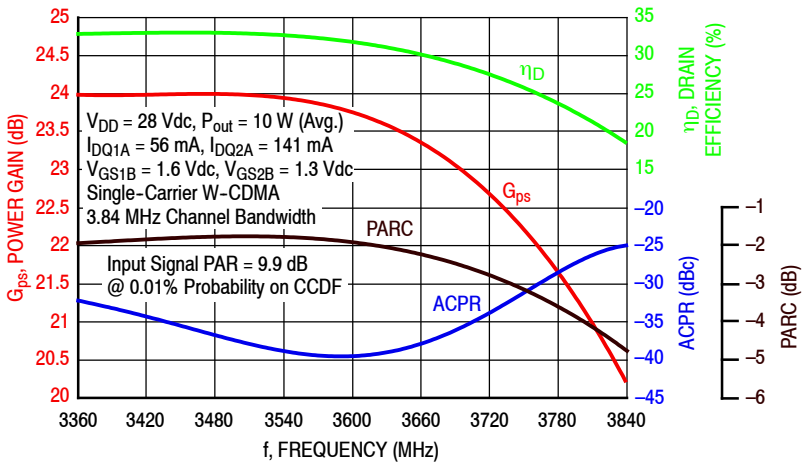


Figure 5. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 10 Watts Avg.

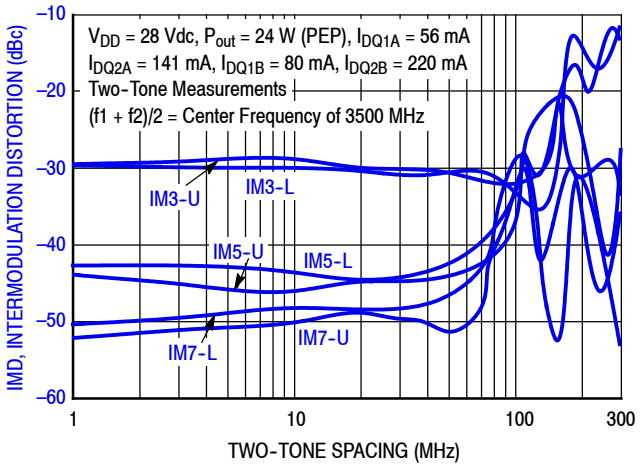


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

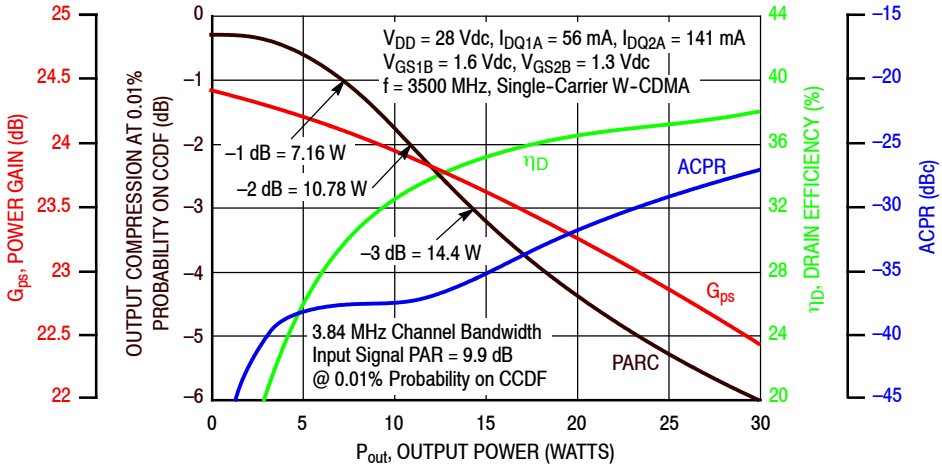


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 3400–3600 MHz

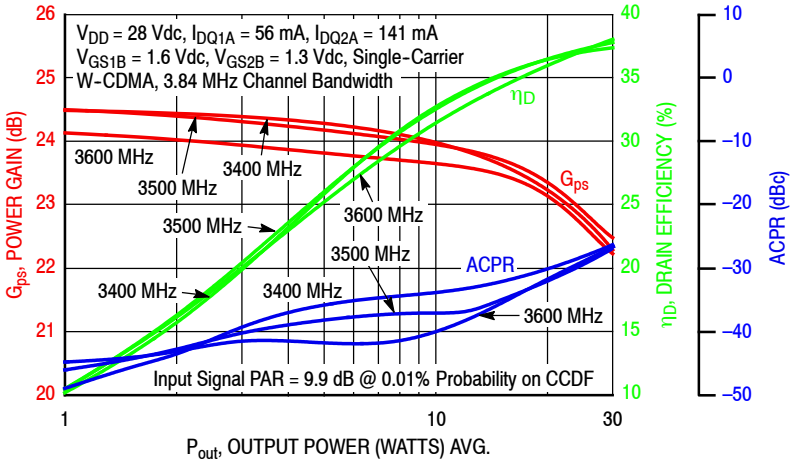


Figure 8. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

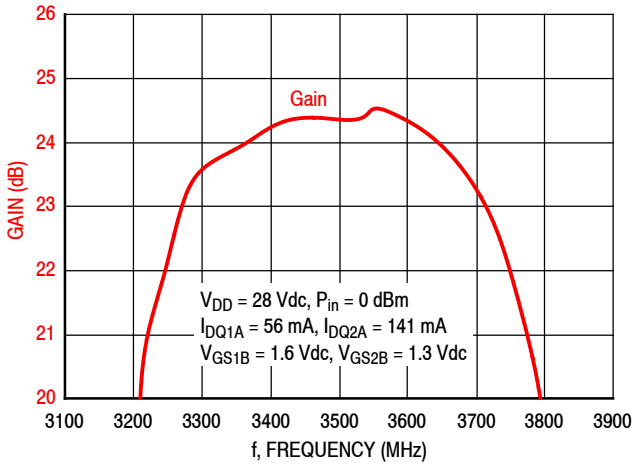
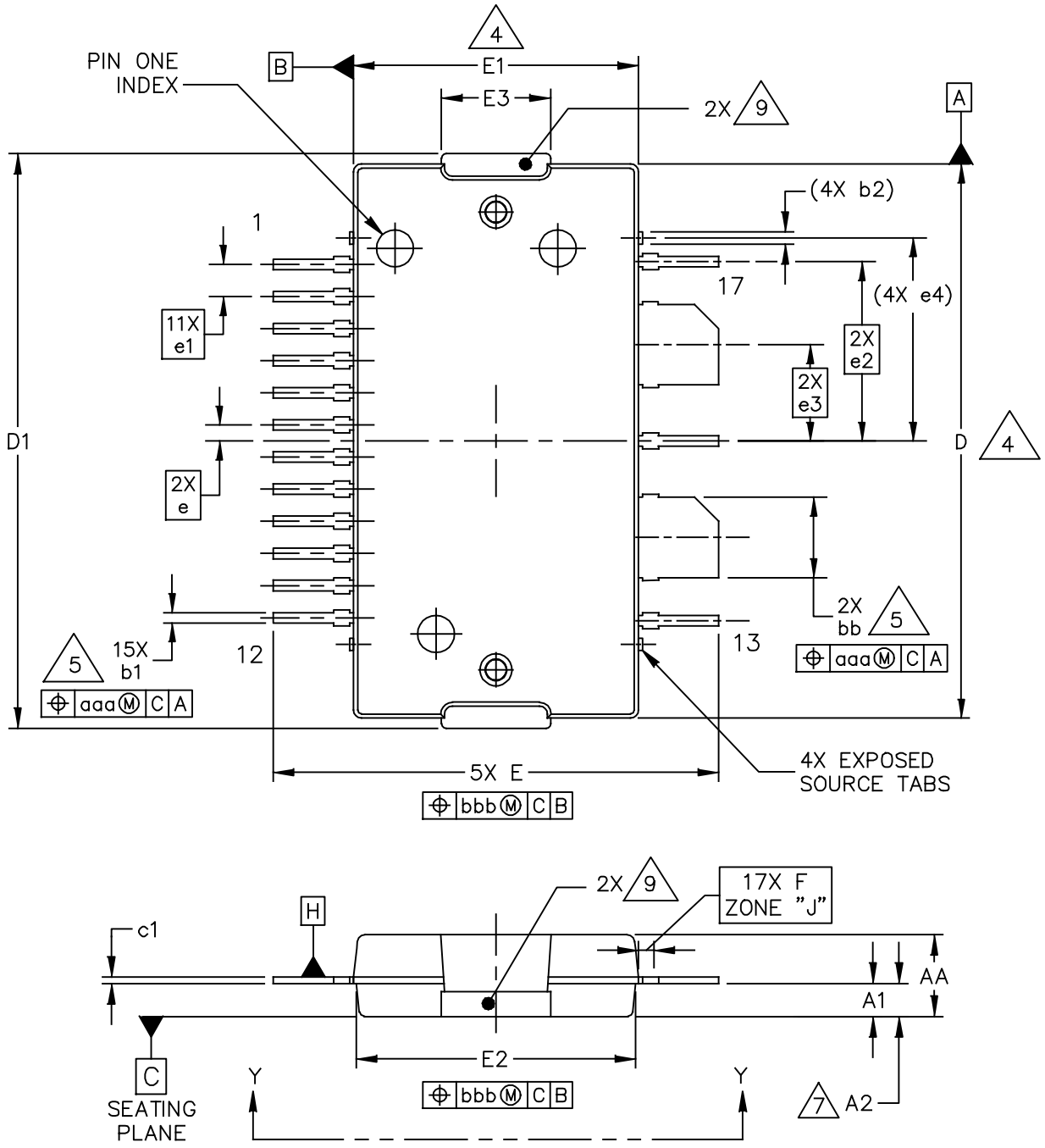


Figure 9. Broadband Frequency Response

PACKAGE DIMENSIONS



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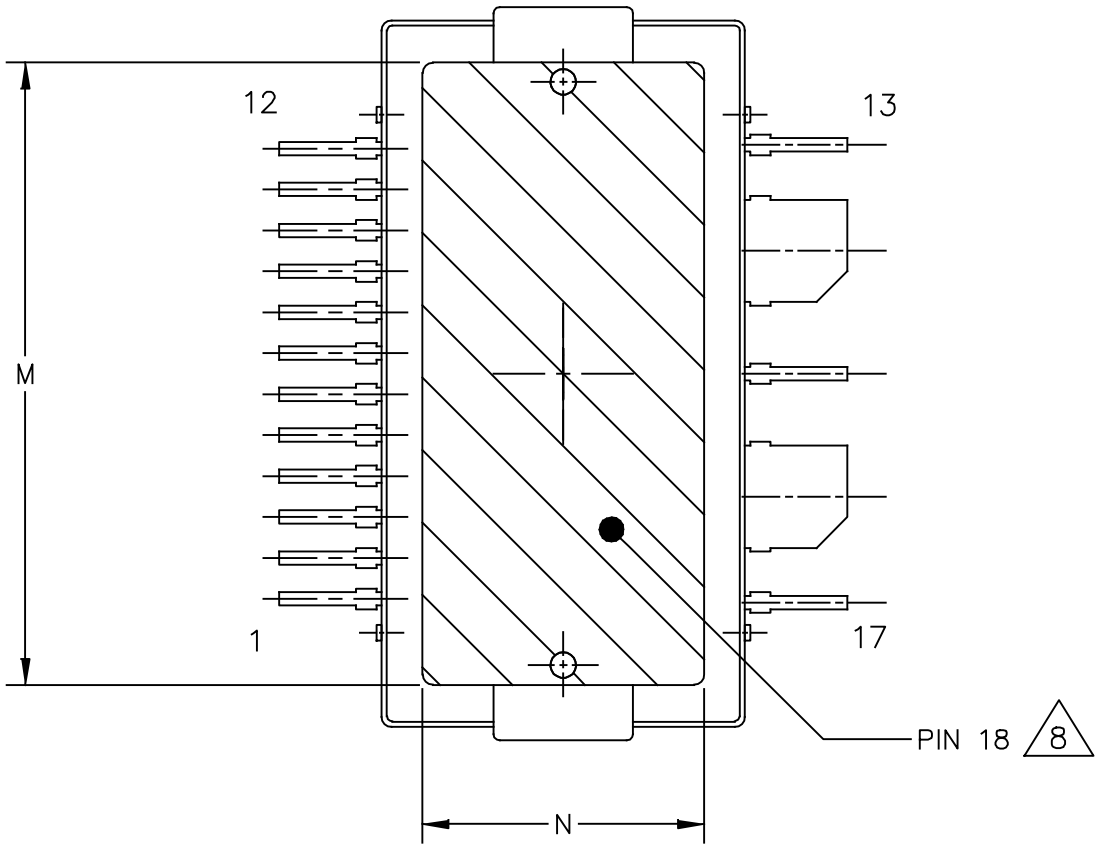

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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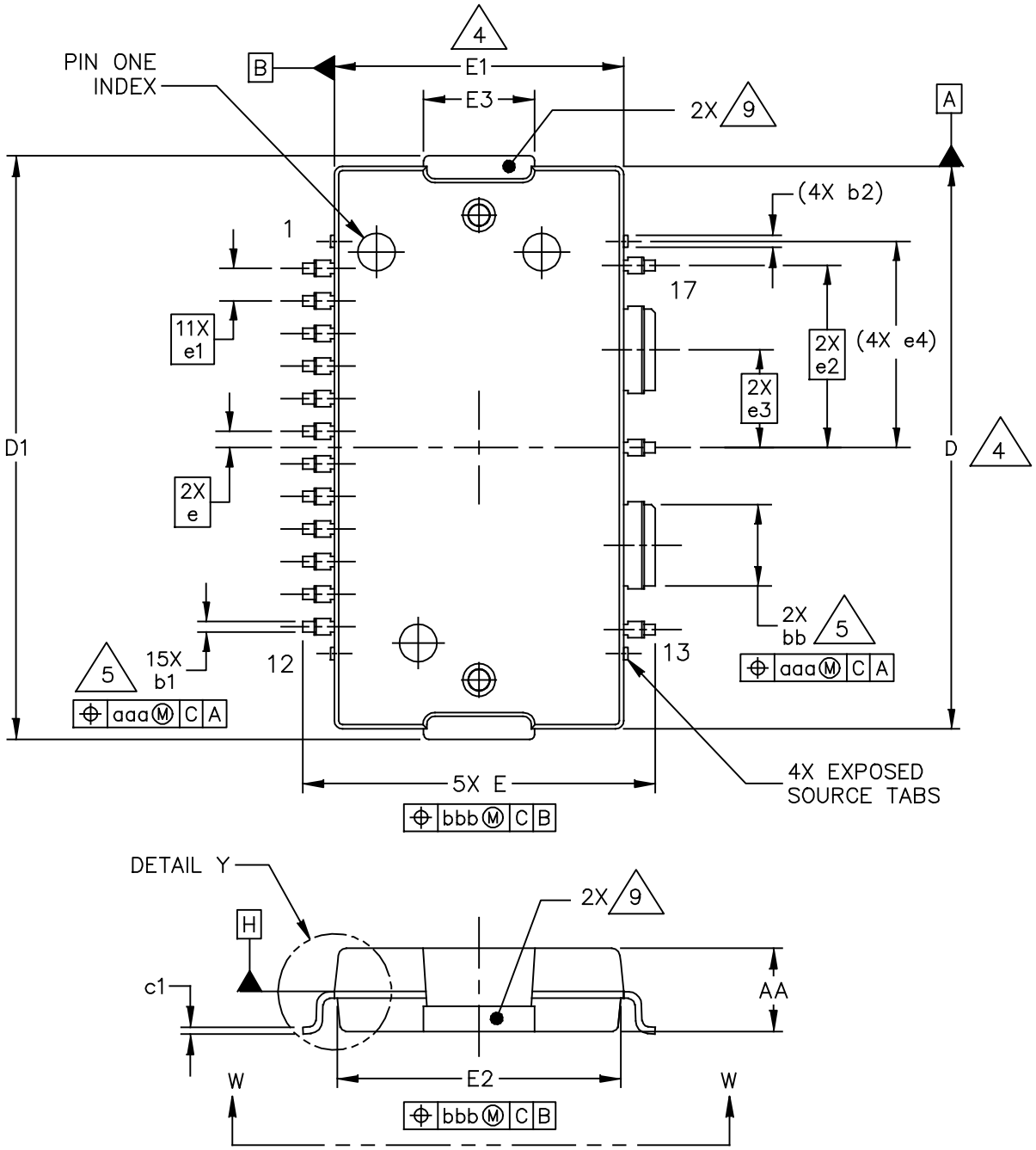

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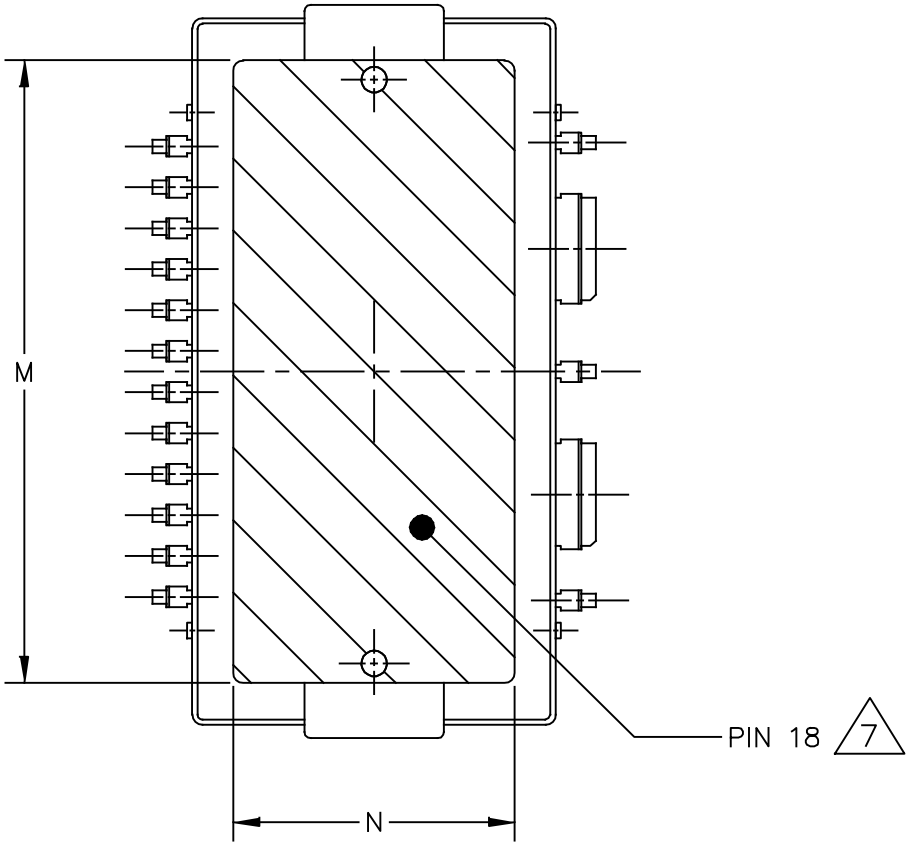

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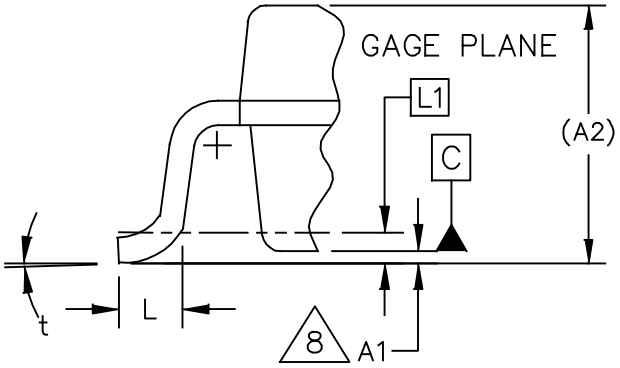

DETAIL "Y"

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	STANDARD: NON–JEDEC	
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7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2016	• Initial Release of Data Sheet

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