

# RF LDMOS Wideband Integrated Power Amplifiers

The MD71C1812N wideband integrated circuit is designed with on-chip matching that makes it usable from 1805 to 2170 MHz. This multi-stage structure is rated for 24 to 32 V operation and covers all typical cellular base station modulation formats.

## Driver Application — 1800 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ1A} = I_{DQ1B} = 20$  mA,  $I_{DQ2A} = I_{DQ2B} = 70$  mA,  $P_{out} = 1.3$  W Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)
1805 MHz	31.9	13.0	-50.3
1840 MHz	31.6	13.4	-50.2
1880 MHz	31.5	14.0	-49.8

- Capable of Handling 5:1 VSWR, @ 32 Vdc, 1840 MHz, 19 W CW Output Power (3 dB Input Overdrive from Rated  $P_{out}$ )

## Driver Application — 1900 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ1A} = I_{DQ1B} = 20$  mA,  $I_{DQ2A} = I_{DQ2B} = 70$  mA,  $P_{out} = 1.3$  W Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)
1930 MHz	32.2	15.2	-51.6
1960 MHz	32.1	15.1	-52.3
1995 MHz	32.0	15.1	-52.6

## Driver Application — 2100 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ1A} = I_{DQ1B} = 20$  mA,  $I_{DQ2A} = I_{DQ2B} = 70$  mA,  $P_{out} = 1.3$  W Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)
2110 MHz	32.2	14.8	-52.8
2140 MHz	32.3	14.6	-52.6
2170 MHz	32.5	14.4	-49.4

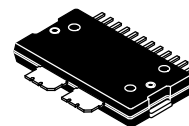
## Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function <sup>(1)</sup>
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

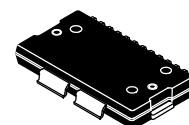
1. Refer to [AN1977](#), Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family, and to [AN1987](#), Quiescent Current Control for the RF Integrated Circuit Device Family. Go to <http://www.freescale.com/rf> and search for AN1977 or AN1987.

**MD71C1812NR1**  
**MD71C1812GNR1**

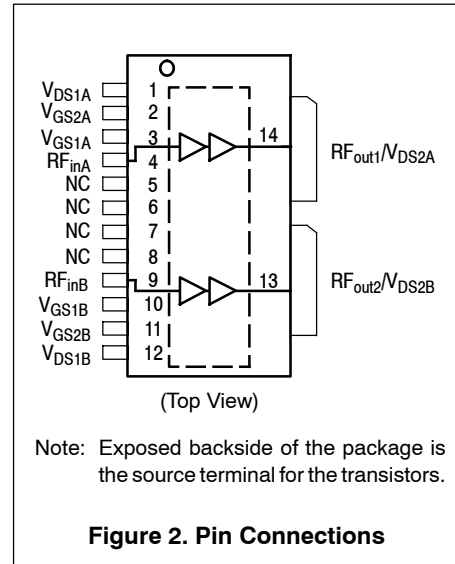
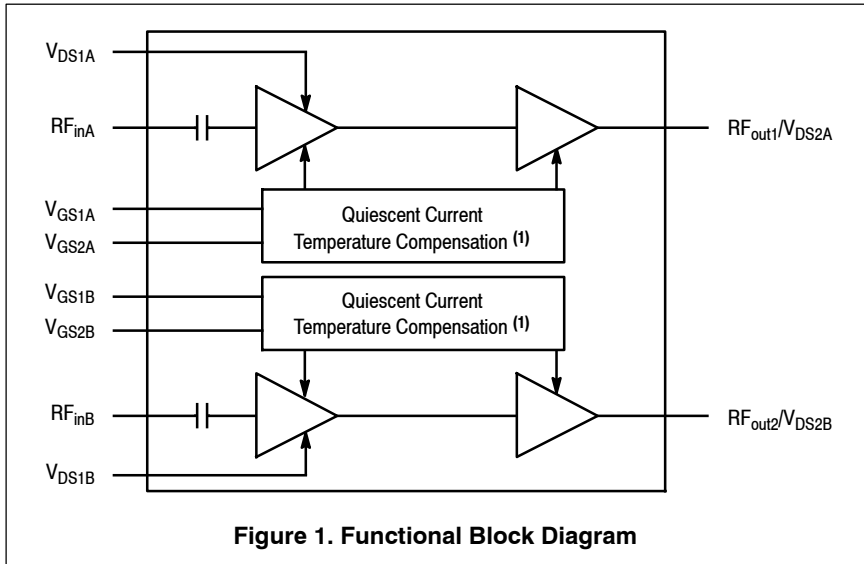
**1805–2170 MHz, 1.3 W AVG., 28 V**  
**SINGLE W-CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**



**TO-270WB-14**  
**PLASTIC**  
**MD71C1812NR1**



**TO-270WBG-14**  
**PLASTIC**  
**MD71C1812GNR1**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (2,3)	$T_J$	225	°C
Input Power	$P_{in}$	20	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 1.3 W CW Stage 1, 28 Vdc, $I_{DQ1A} = I_{DQ1B} = 40$ mA, 1840 MHz Stage 2, 28 Vdc, $I_{DQ2A} = I_{DQ2B} = 180$ mA, 1840 MHz	$R_{\theta JC}$	6.5 2.9	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JEESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Refer to [AN1977](#), *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to [AN1987](#), *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf> and search for AN1977 or AN1987.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
4. Refer to [AN1955](#), *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 1 - Off Characteristics</b> <sup>(1)</sup>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$

**Stage 1 - On Characteristics** <sup>(1)</sup>

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 5\text{ }\mu\text{A}$ )	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ1A} = I_{DQ1B} = 20\text{ mA}$ )	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1A} = I_{DQ1B} = 20\text{ mA}$ , Measured in Functional Test)	$V_{GG(Q)}$	4.2	5.0	5.7	Vdc

**Stage 2 - Off Characteristics** <sup>(1)</sup>

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$

**Stage 2 - On Characteristics** <sup>(1)</sup>

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 24\text{ }\mu\text{A}$ )	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2A} = I_{DQ2B} = 70\text{ mA}$ )	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2A} = I_{DQ2B} = 70\text{ mA}$ , Measured in Functional Test)	$V_{GG(Q)}$	3.2	4.0	4.7	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 240\text{ mA}$ )	$V_{DS(on)}$	0.1	0.24	1.5	Vdc

**Functional Tests** <sup>(2,3)</sup> (In Freescale Wideband 1805–1880 Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1A} = I_{DQ1B} = 20\text{ mA}$ ,  $I_{DQ2A} = I_{DQ2B} = 70\text{ mA}$ ,  $P_{out} = 1.3\text{ W Avg.}$ ,  $f = 1880\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	31.0	31.5	35.0	dB
Power Added Efficiency	PAE	13.0	14.0	—	%
Adjacent Channel Power Ratio	ACPR	—	-49.8	-47.5	dBc

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurement made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

(continued)

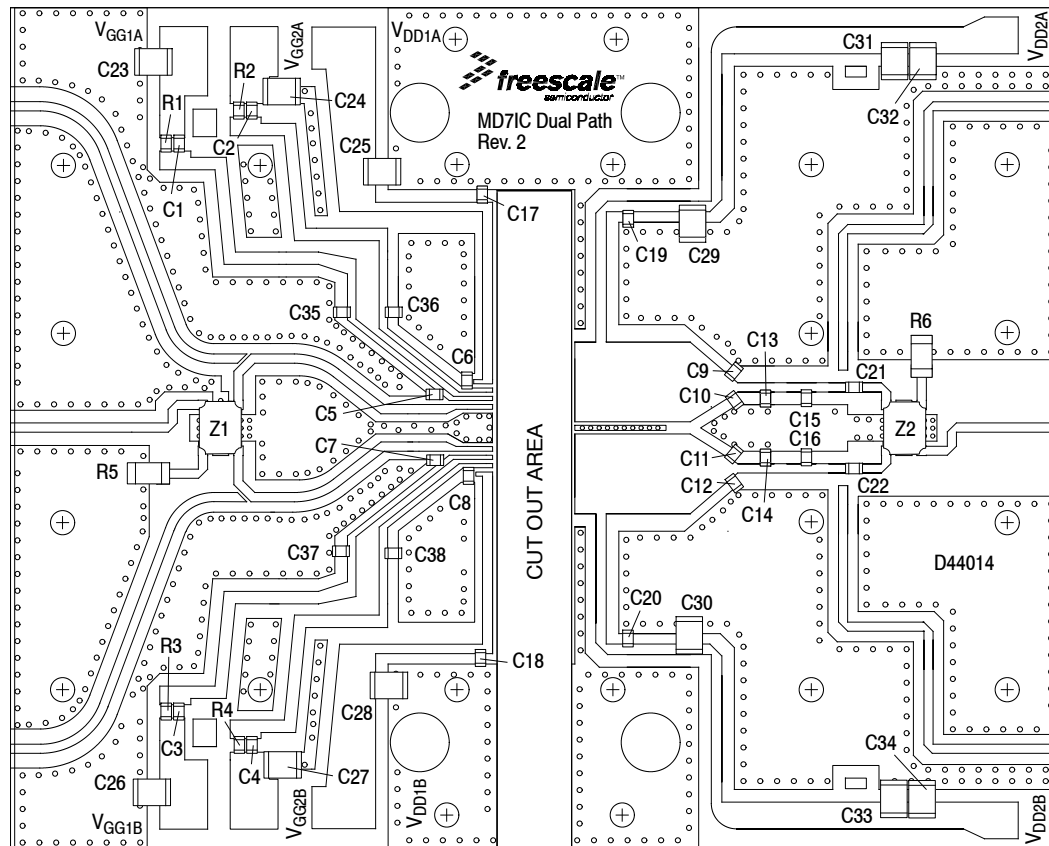
**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performance</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1A} = I_{DQ1B} = 20\text{ mA}$ , $I_{DQ2A} = I_{DQ2B} = 70\text{ mA}$ , 1805–1880 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	12	—	W
$P_{out}$ @ 3 dB Compression Point, CW	P3dB	—	13	—	W
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	140	—	MHz
Quiescent Current Accuracy over Temperature <sup>(1)</sup> with 2 k $\Omega$ Gate Feed Resistors (–30 to 85°C)      Stage 1 with 2 k $\Omega$ Gate Feed Resistors (–30 to 85°C)      Stage 2	$\Delta I_{QT}$	—	2.5 1.7	—	%
Gain Flatness in 75 MHz Bandwidth @ $P_{out} = 1.3\text{ W Avg.}$	$G_F$	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	$\Delta G$	—	0.03	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	$\Delta P_{1dB}$	—	0.014	—	dB/°C

**Table 6. Ordering Information**

Device	Tape and Reel Information	Package
MD7IC1812NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-14
MD7IC1812GNR1		TO-270WBG-14

1. Refer to [AN1977](#), *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to [AN1987](#), *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf> and search for AN1977 or AN1987.

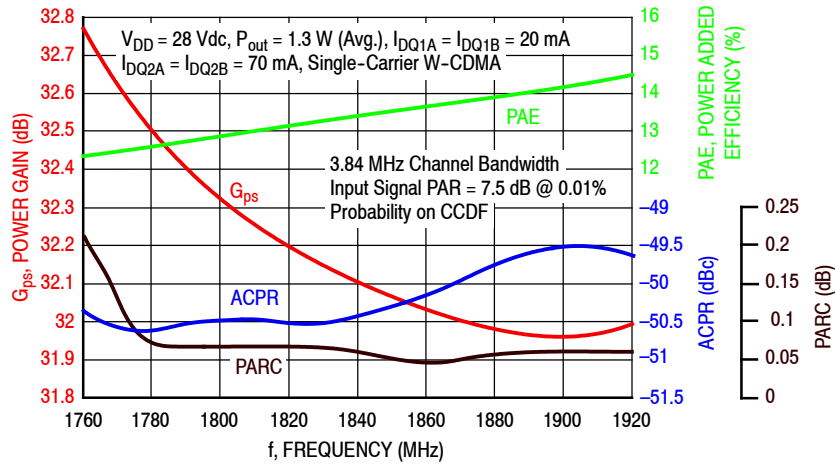


**Figure 3. MD7IC1812NR1 Test Circuit Component Layout**

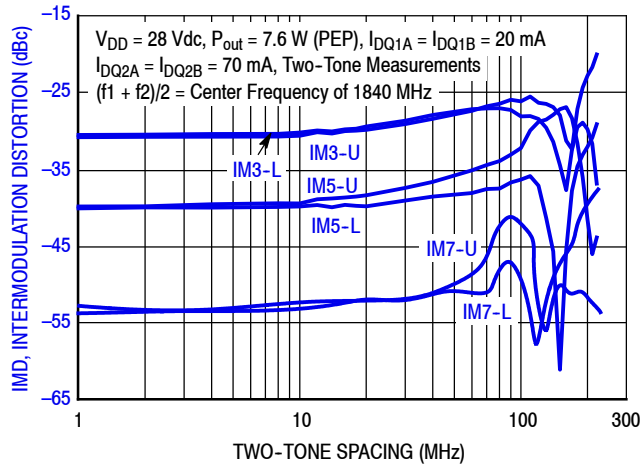
**Table 7. MD7IC1812NR1 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	3.9 pF Chip Capacitors	ATC600F3R9BT250XT	ATC
C5, C6, C7, C8	1.0 pF Chip Capacitors	ATC600F1R0BT250XT	ATC
C9, C10, C11, C12	0.6 pF Chip Capacitors	ATC600F0R6BT250XT	ATC
C13, C14	0.8 pF Chip Capacitors	ATC600F0R8BT250XT	ATC
C15, C16	1.2 pF Chip Capacitors	ATC600F1R2BT250XT	ATC
C17, C18, C19, C20	10 pF Chip Capacitors	ATC600F10RBT250XT	ATC
C21, C22	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34	10 $\mu$ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C35, C36, C37, C38	22 nF Chip Capacitors	GRM31MR72A223KA01L	Murata
R1, R2, R3, R4	2 K $\Omega$ , 1/4 W Chip Resistors	CRCW12062K00FKEA	Vishay
R5, R6	50 $\Omega$ , 20 W Termination	375375-6X50-2	Anaren
Z1, Z2	1800–2300 MHz Band, 90°, 3 dB Hybrid Couplers	X3C21P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D44014	MTL

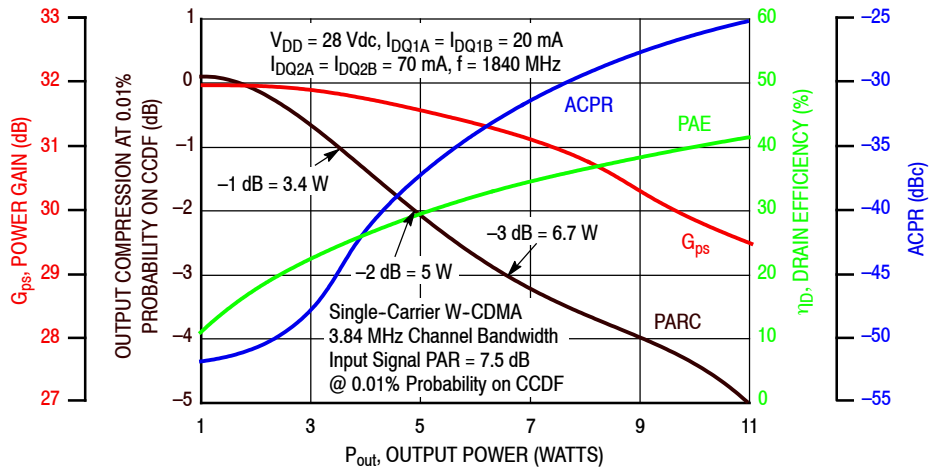
### TYPICAL CHARACTERISTICS — 1805–1880 MHz



**Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.3$  Watts Avg.**

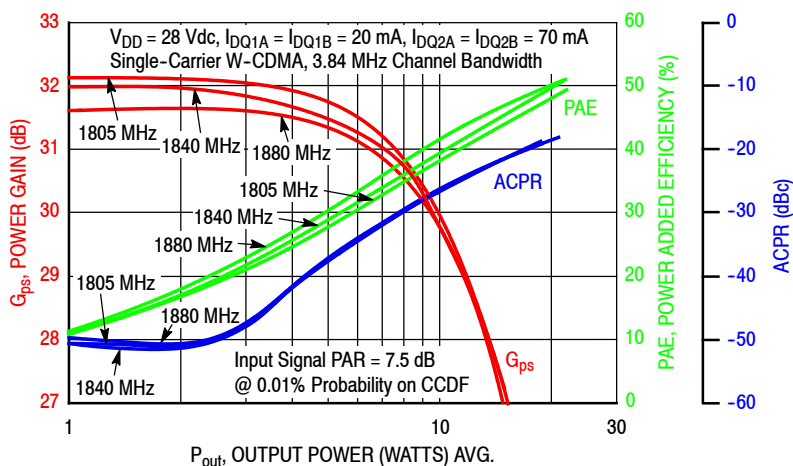


**Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing**

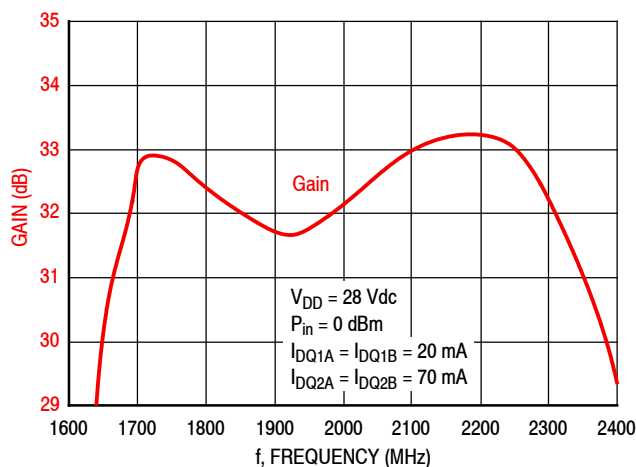


**Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS — 1805–1880 MHz



**Figure 7. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**



**Figure 8. Broadband Frequency Response**

**Table 8. Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQ1A} = I_{DQ1B} = 12$  mA,  $I_{DQ2A} = I_{DQ2B} = 80$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1800	18.6 + j0.84	21.6 – j14.9	9.75 – j4.18	26.4	40.8	12	59.9	–5
1840	18.9 – j2.06	22.0 – j13.4	9.94 – j4.69	25.5	40.8	12	59.8	–4
1880	19.9 – j5.86	22.3 – j11.4	9.53 – j5.22	24.7	40.8	12	59.6	–3
1930	21.2 – j6.08	21.2 – j8.50	9.13 – j5.50	24.3	40.9	12	59.5	–3
1960	21.3 – j7.19	20.7 – j7.35	9.42 – j5.43	23.9	40.8	12	58.5	–3
1995	23.3 – j9.53	19.9 – j6.74	9.23 – j5.43	23.8	40.8	12	58.1	–3
2110	16.2 + j0.01	16.6 + j0.14	9.12 – j5.48	24.5	40.8	12	57.6	–4
2140	16.2 – j1.24	16.9 + j2.33	9.27 – j5.44	24.6	40.8	12	57.5	–4
2170	16.1 – j2.79	17.2 + j4.75	9.44 – j5.76	24.9	40.8	12	56.8	–4

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
1800	18.6 + j0.84	22.8 – j15.9	10.8 – j4.58	24.1	41.5	14	60.9	–6
1840	18.9 – j2.06	22.7 – j14.6	10.9 – j5.19	23.2	41.6	14	60.6	–5
1880	19.9 – j5.86	22.6 – j12.7	10.4 – j5.78	22.4	41.6	14	60.2	–5
1930	21.2 – j6.08	21.2 – j8.50	9.13 – j5.50	24.3	40.9	12	59.5	–3
1960	21.3 – j7.19	20.7 – j7.35	9.42 – j5.43	23.9	40.8	12	58.5	–3
1995	23.3 – j9.53	19.9 – j6.74	9.23 – j5.43	23.8	40.8	12	58.1	–3
2110	16.2 + j0.01	16.6 + j0.14	9.12 – j5.48	24.5	40.8	12	57.6	–4
2140	16.2 – j1.24	16.9 + j2.33	9.27 – j5.44	24.6	40.8	12	57.5	–4
2170	16.1 – j2.79	17.2 + j4.75	9.44 – j5.76	24.9	40.8	12	56.8	–4

(1) Load impedance for optimum P1dB power.

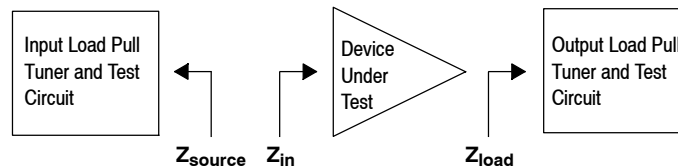
(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Note: Measurement made on a per side basis.**





**Table 9. Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1A} = I_{DQ1B} = 12 \text{ mA}$ ,  $I_{DQ2A} = I_{DQ2B} = 80 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
1800	18.6 + j0.84	21.8 - j10.1	5.59 - j0.05	27.8	39.2	8	68.3	-9
1840	18.9 - j2.06	22.5 - j9.13	5.29 - j1.05	26.9	39.2	8	67.6	-9
1880	19.9 - j5.86	23.1 - j7.30	5.08 - j1.75	26.1	39.3	8	67.4	-9
1930	21.2 - j6.08	22.4 - j5.16	4.95 - j2.29	25.7	39.4	9	67.0	-9
1960	21.3 - j7.19	22.0 - j4.53	5.22 - j2.57	25.3	39.6	9	66.5	-8
1995	23.3 - j9.53	21.7 - j3.81	5.26 - j2.76	25.1	39.6	9	65.4	-8
2110	16.2 + j0.01	18.8 + j2.28	4.73 - j3.36	25.8	39.5	9	64.3	-9
2140	16.2 - j1.24	18.1 + j3.56	4.67 - j3.68	26.1	39.5	9	64.2	-10
2170	16.1 - j2.79	18.9 + j6.77	5.18 - j3.92	26.4	39.7	9	63.3	-10

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
1800	18.6 + j0.84	22.7 - j12.6	6.21 - j0.66	25.6	40.2	11	69.5	-10
1840	18.9 - j2.06	23.1 - j11.5	5.87 - j1.57	24.8	40.2	11	68.7	-10
1880	19.9 - j5.86	23.6 - j9.16	5.27 - j1.95	24.1	40.0	10	68.0	-11
1930	21.2 - j6.08	22.4 - j5.16	4.95 - j2.29	25.7	39.4	9	67.0	-9
1960	21.3 - j7.19	22.0 - j4.53	5.22 - j2.57	25.3	39.6	9	66.5	-8
1995	23.3 - j9.53	21.7 - j3.81	5.26 - j2.76	25.1	39.6	9	65.4	-8
2110	16.2 + j0.01	18.8 + j2.28	4.73 - j3.36	25.8	39.5	9	64.3	-9
2140	16.2 - j1.24	18.1 + j3.56	4.67 - j3.68	26.1	39.5	9	64.2	-10
2170	16.1 - j2.79	18.9 + j6.77	5.18 - j3.92	26.4	39.7	9	63.3	-10

(1) Load impedance for optimum P1dB efficiency.

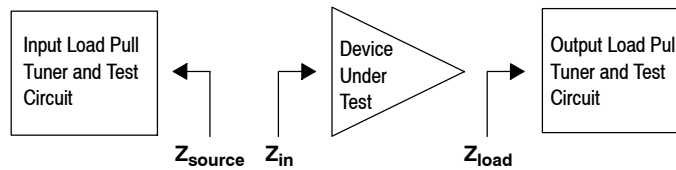
(2) Load impedance for optimum P3dB efficiency.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Note: Measurement made on a per side basis.**



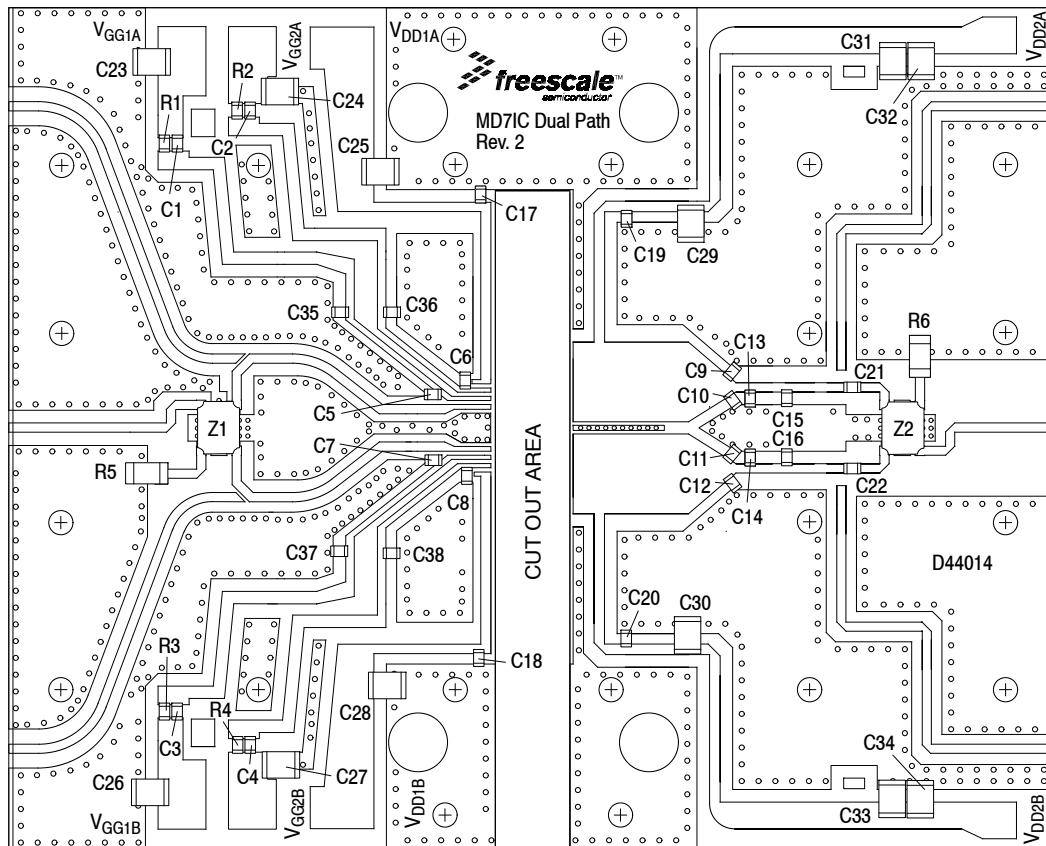
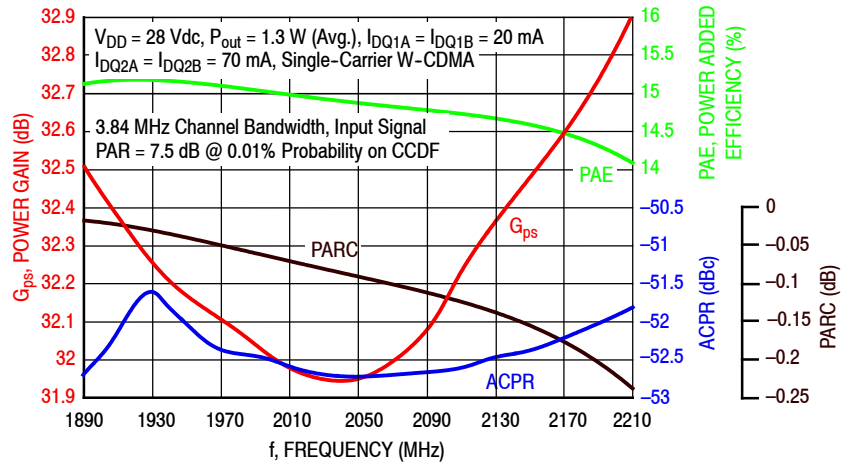


Figure 9. MD7IC1812NR1 Test Circuit Component Layout — 1930–2170 MHz

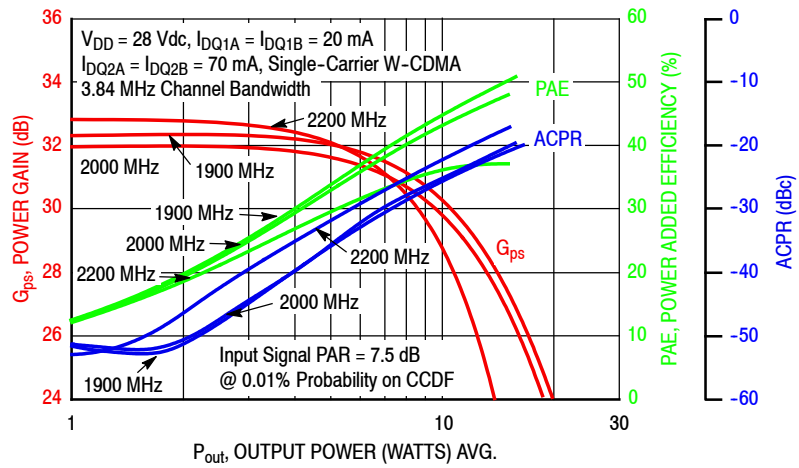
Table 10. MD7IC1812NR1 Test Circuit Component Designations and Values — 1930–2170 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	3.3 pF Chip Capacitors	ATC600F3R3BT250XT	ATC
C5, C7	2.0 pF Chip Capacitors	ATC600F2R0BT250XT	ATC
C6, C8	1.5 pF Chip Capacitors	ATC600F1R5BT250XT	ATC
C9, C10, C11, C12	0.6 pF Chip Capacitors	ATC600F0R6BT250XT	ATC
C13, C14	0.8 pF Chip Capacitors	ATC600F0R8BT250XT	ATC
C15, C16	1.2 pF Chip Capacitors	ATC600F1R2BT250XT	ATC
C17, C18, C19, C20	10 pF Chip Capacitors	ATC600F10RBT250XT	ATC
C21, C22	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34	10 $\mu$ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C35, C36, C37, C38	22 nF Chip Capacitors	GRM31BR72E223KW01L	Murata
R1, R2, R3, R4	2 K $\Omega$ , 1/4 W Chip Resistors	CRCW12062K00FKEA	Vishay
R5, R6	50 $\Omega$ , 20 W Termination	375375-6X50-2	Anaren
Z1, Z2	1800–2300 MHz Band, 90°, 3 dB Hybrid Couplers	X3C21P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D44014	MTL

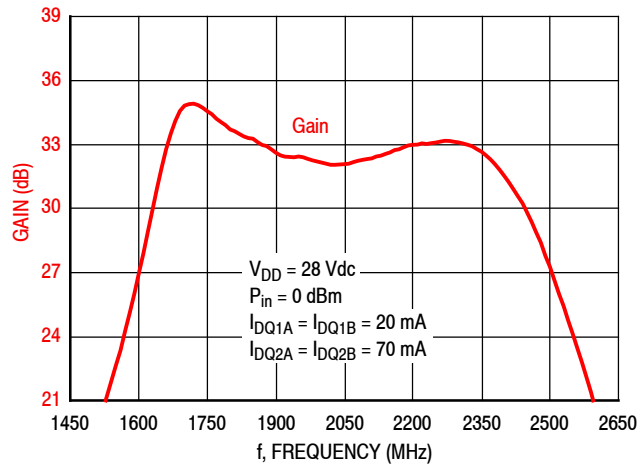
### TYPICAL CHARACTERISTICS — 1930–2170 MHz



**Figure 10. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 1.3$  Watts Avg.**

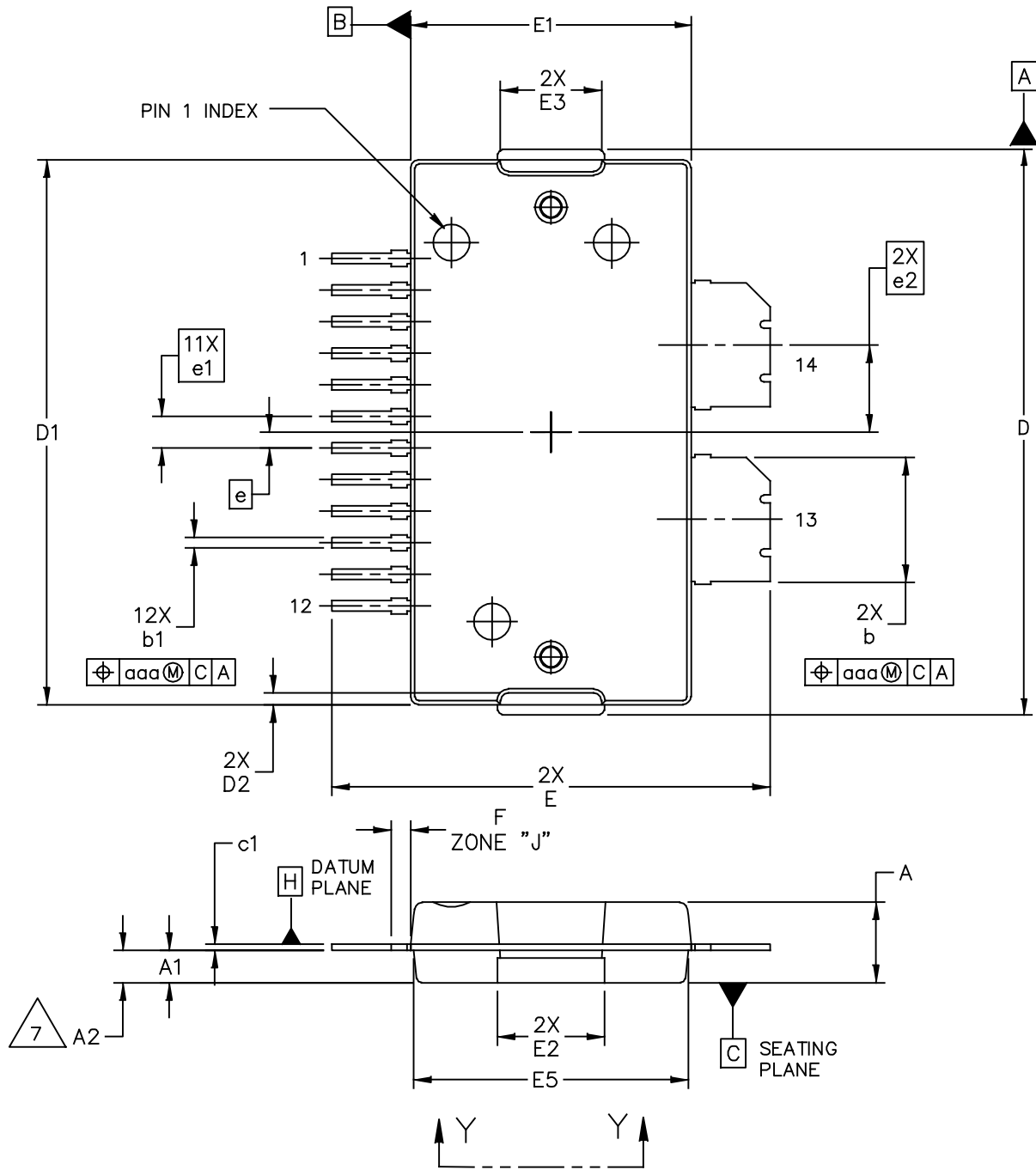


**Figure 11. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**



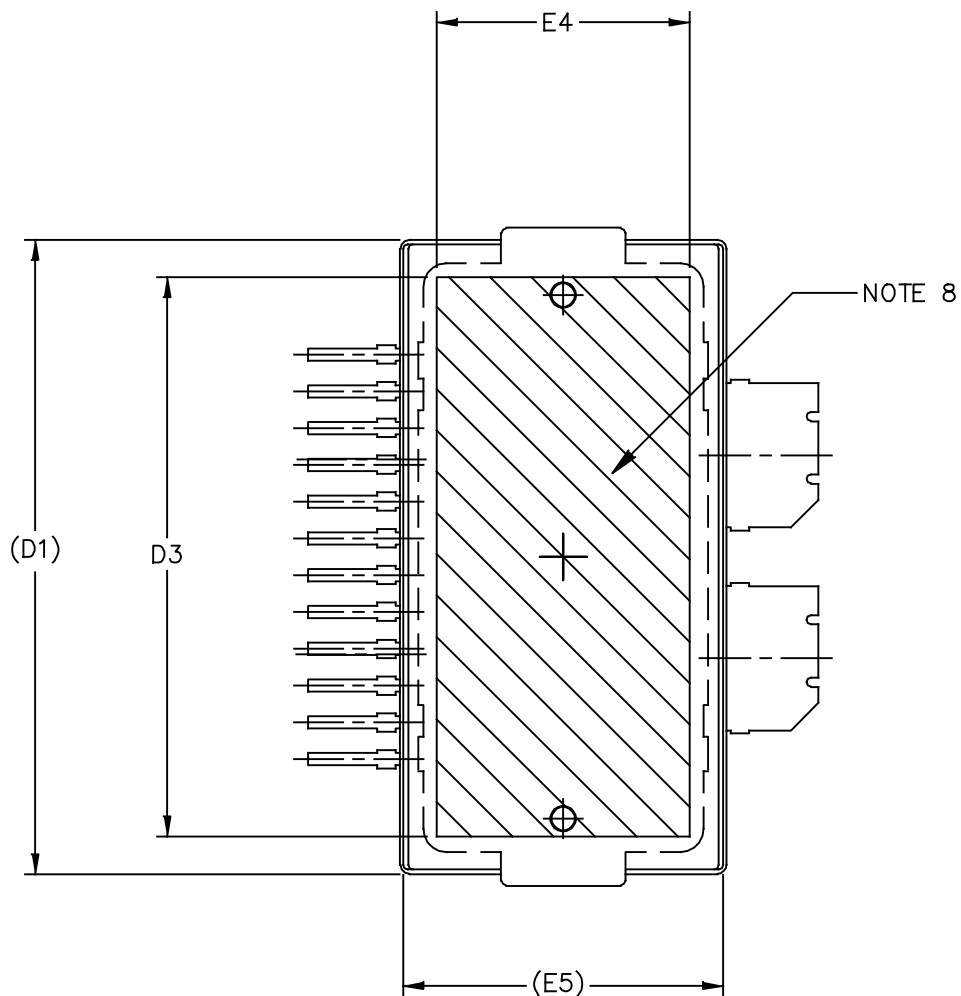
**Figure 12. Broadband Frequency Response**

**PACKAGE DIMENSIONS**



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**MD7IC1812NR1 MD7IC1812GNR1**



VIEW Y-Y

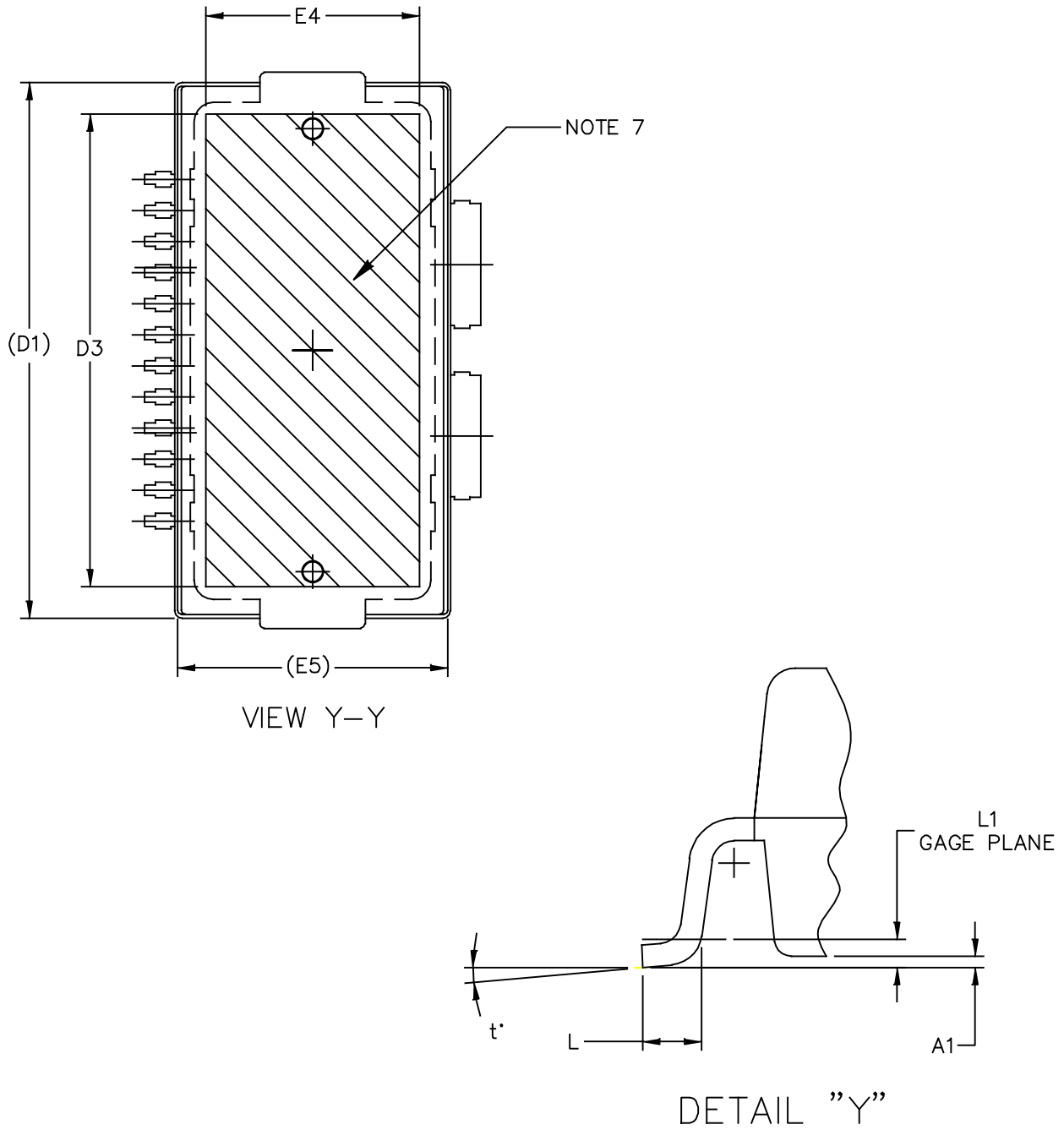
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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2'	8'	2'	8'
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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					CASE NUMBER: 1621-02			19 JUN 2007	
					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

### Development Tools

- Printed Circuit Boards

### To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2015	• Initial Release of Data Sheet

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