74LVC646A

Octal bus transceiver/register; 3-state

Rev. 5 — 28 March 2013 Product data sheet

1. General description

The 74LVC646A consists of non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the A or B bus is clocked in the internal registers, as the appropriate clock (CPAB or CPBA) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. With the select source inputs (SAB and SBA), stored and real-time (transparent mode) data can be multiplexed. The direction (DIR) input determines which bus receives data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), A data may be stored in the B register and/or B data may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses A or B may be driven at a time.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V and 5 V applications.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Supports partial power-down applications; inputs/outputs are high-impedance when V_{CC} = 0 V
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC646AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC646ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC646APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Functional diagram

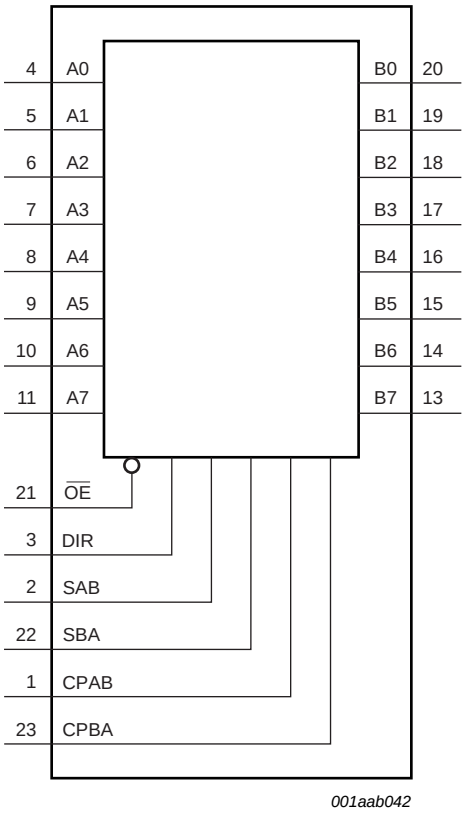

Fig 1. Functional diagram

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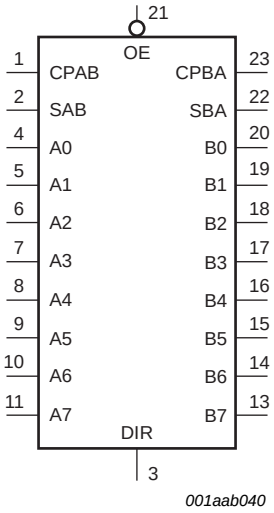

Fig 2. Logic symbol

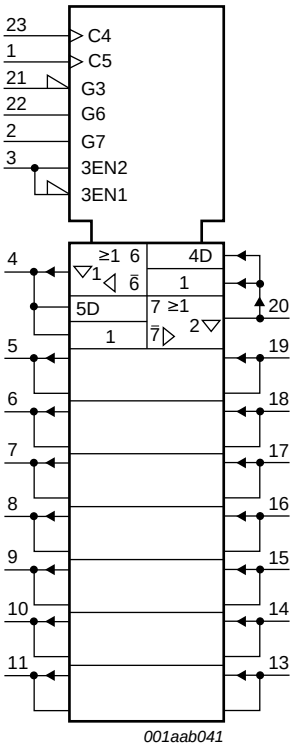

Fig 3. IEC logic symbol

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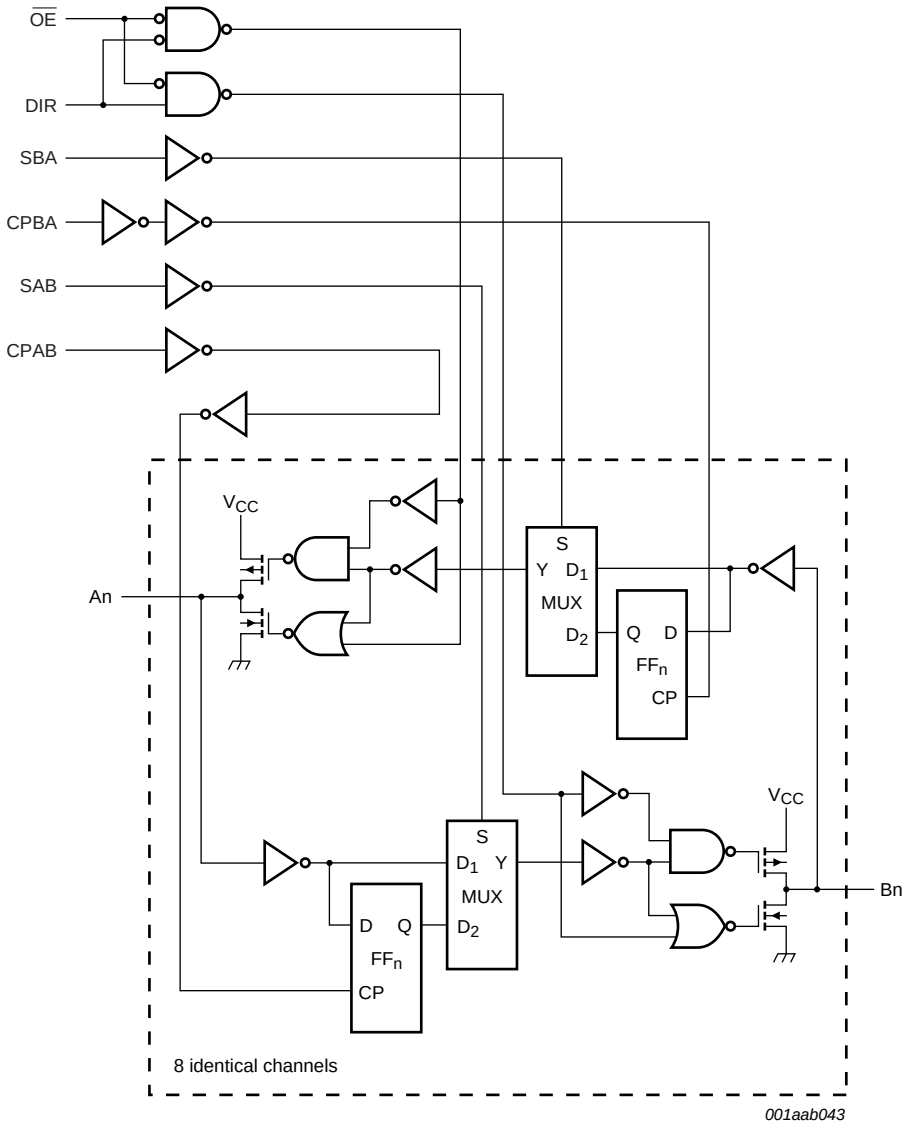

Fig 4. Logic diagram

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5. Pinning information

5.1 Pinning

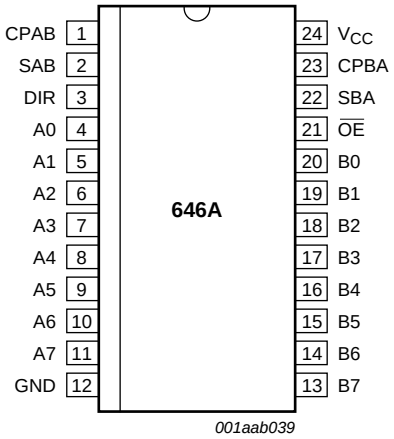

Fig 5. Pin configuration SO24 and (T)SSOP24

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CPAB	1	A to B clock input (LOW to HIGH; edge-triggered)
SAB	2	A to B select source input
SBA	22	B to A select source input
DIR	3	direction control input
A[0:7]	4, 5, 6, 7, 8, 9, 10, 11	A data input/output
B[0:7]	20, 19, 18, 17, 16, 15, 14, 13	B data input/output
$\overline{OE}$	21	output enable input (active LOW)
CPBA	23	B to A clock input (LOW to HIGH, edge-triggered)
GND	12	ground (0 V)
V_{CC}	24	supply voltage

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6. Functional description

Table 3. Function table[1]

Input						Data I/O		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A0 to A7	B0 to B7	
X	X	↑	X	X	X	input	unspecified[2]	store A and B unspecified
X	X	X	↑	X	X	unspecified[2]	input	store B and A unspecified
H	X	↑	↑	X	X	input	input	store A and B data
H	X	H or L	H or L	X	X	input	input	hold storage; isolation
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	H or L	X	H	output	input	stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus
L	H	H or L	X	H	X	input	output	stored A data to B bus

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW to HIGH level transition

[2] The data output functions are enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e. data at the bus inputs are stored on every LOW to HIGH transition on the clock inputs.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		−50	-	mA
V_I	input voltage		[1]	−0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2]	−0.5	V_{CC} + 0.5	V
		output 3-state	[2]	−0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			−100	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	HIGH or LOW state	0	-	V_{CC}	V
		3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	−40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = −100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} − 0.2	-	-	V_{CC} − 0.3	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = −18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	µA

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Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND; [2]	-	0.1	±10	-	±20	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	0.1	±10	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V; I_O = 0 A	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF
$C_{I/O}$	input/output capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	10.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] For transceivers, the parameter I_{OZ} includes the input leakage current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 11.

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	An, Bn to Bn, An; see Figure 6 [2]						
		V_{CC} = 1.2 V	-	17	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.8	6.9	15.8	1.8	18.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.7	8.2	1.5	9.4	ns
		V_{CC} = 2.7 V	1.5	3.6	7.8	1.5	10.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.1	6.8	1.0	8.0	ns
		CPAB, CPBA to Bn, An; see Figure 7 [2]						
		V_{CC} = 1.2 V	-	19	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.4	8.6	17.8	2.4	20.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	4.5	9.1	1.7	10.5	ns
		V_{CC} = 2.7 V	1.5	4.1	8.6	1.5	11.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.8	7.6	1.0	9.5	ns
		SAB, SBA to Bn, An; see Figure 8 [2]						
		V_{CC} = 1.2 V	-	19	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	7.6	19.8	1.5	22.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	4.0	10.2	1.5	11.8	ns
		V_{CC} = 2.7 V	1.5	4.0	9.5	1.5	12.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.4	8.5	1.0	11.0	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 11.

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{en}	enable time	$\overline{OE}$ to An and Bn; see Figure 9 [2]						
		V_{CC} = 1.2 V	-	20	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.4	7.2	17.8	2.4	20.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	4.1	9.8	2.0	11.3	ns
		V_{CC} = 2.7 V	1.5	4.2	8.8	1.5	11.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.3	7.8	1.0	10.0	ns
		DIR to An and Bn; see Figure 10 [2]						
		V_{CC} = 1.2 V	-	20	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.9	8.0	18.1	2.9	20.9	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	4.5	9.9	2.4	11.5	ns
		V_{CC} = 2.7 V	1.5	4.2	8.9	1.5	11.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.6	7.9	1.0	10.0	ns
t_{dis}	disable time	$\overline{OE}$ to An and Bn; see Figure 9 [2]						
		V_{CC} = 1.2 V	-	10	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	3.6	5.0	10.4	3.6	12.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	5.9	1.0	6.8	ns
		V_{CC} = 2.7 V	1.5	3.6	7.1	1.5	9.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.3	6.1	1.0	8.0	ns
		DIR to An and Bn; see Figure 10 [2]						
		V_{CC} = 1.2 V	-	10	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.9	3.9	10.1	2.9	11.7	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.1	5.7	1.0	6.6	ns
		V_{CC} = 2.7 V	1.5	3.5	7.0	1.5	9.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	6.0	1.0	7.5	ns
t_W	pulse width	clock HIGH or LOW of CPAB or CPBA; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V_{CC} = 2.7 V	3.3	-	-	3.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	1.9	-	3.3	-	ns
t_{su}	set-up time	An, Bn to CPAB, CPBA; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	3.5	-	-	3.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V_{CC} = 2.7 V	1.6	-	-	1.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	0.35	-	1.5	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 11.

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	An, Bn to CPAB, CPBA; see Figure 7							
		V_{CC} = 1.65 V to 1.95 V		3.0	-	-	3.0	-	ns
		V_{CC} = 2.3 V to 2.7 V		2.0	-	-	2.0	-	ns
		V_{CC} = 2.7 V		1.0	-	-	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	−0.3	-	1.0	-	ns
f_{max}	maximum frequency	see Figure 7							
		V_{CC} = 1.65 V to 1.95 V		100	-	-	80	-	MHz
		V_{CC} = 2.3 V to 2.7 V		125	-	-	100	-	MHz
		V_{CC} = 2.7 V		150	-	-	120	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	250	-	120	-	MHz
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	8.0	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	11.7	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	15.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

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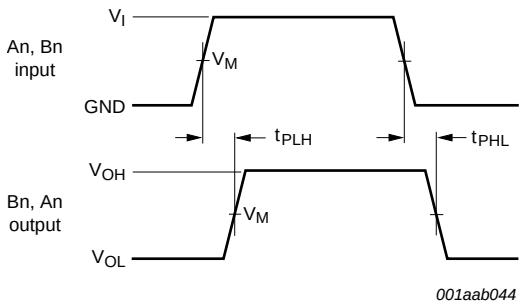
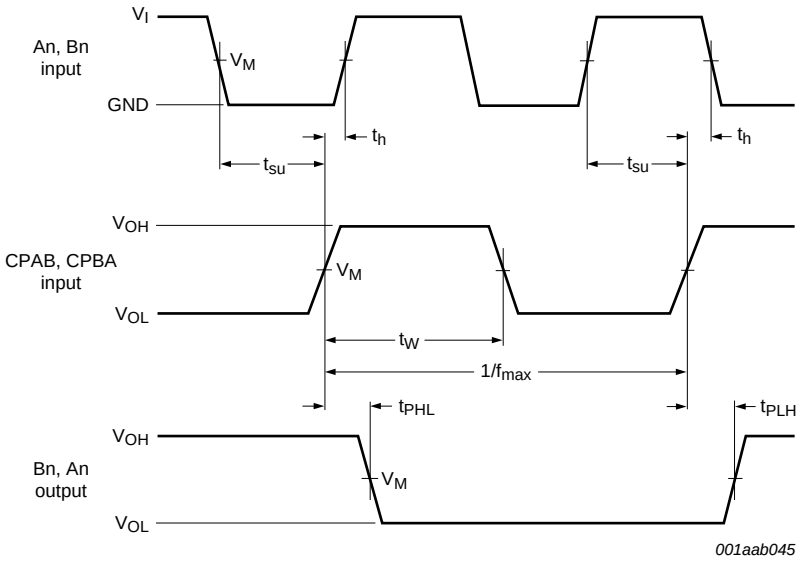
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Input (An and Bn) to output (Bn and An) propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The An, Bn to CPAB, CPBA set-up and hold times, clock CPAB and CPBA pulse width, maximum frequency, and the CPAB, CPBA to output Bn, An propagation delays

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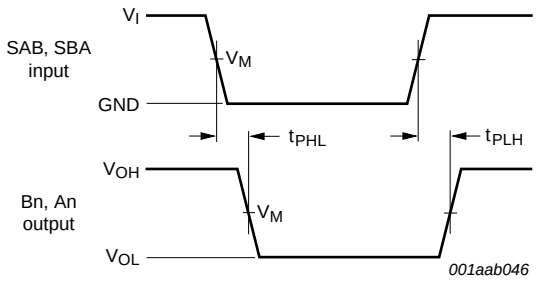
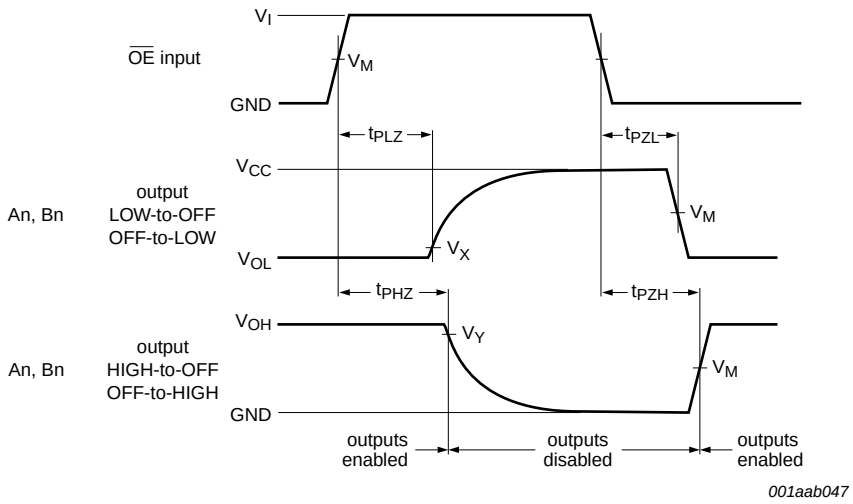


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The input SAB and SBA to output Bn and An propagation delay times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. The input $\overline{OE}$ to output An and Bn 3-state enable and disable times

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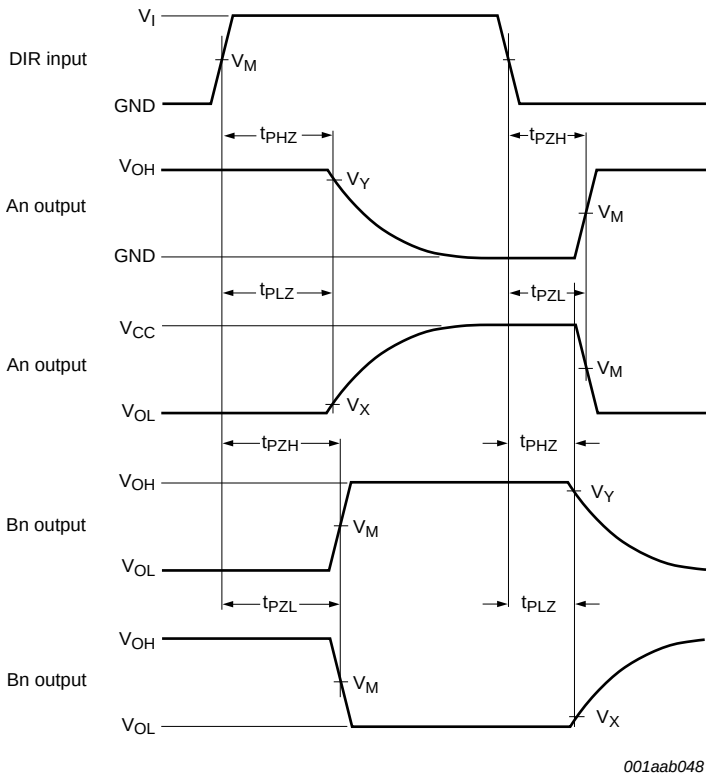

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. The input showing the input DIR to output An, Bn 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V

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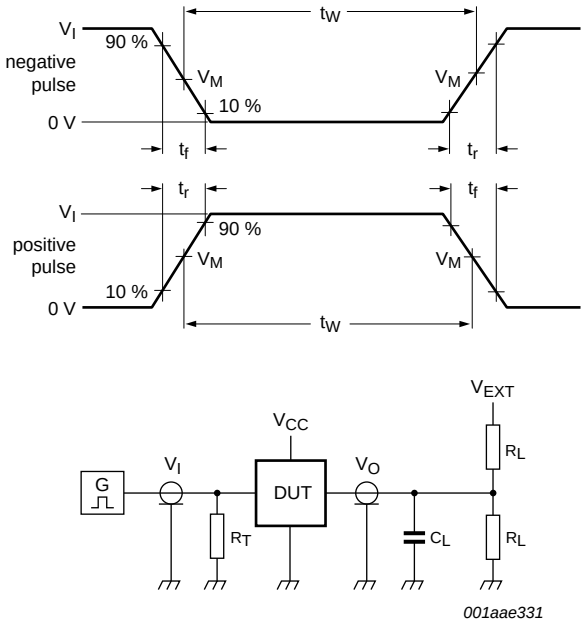

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 11. Load circuitry for switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

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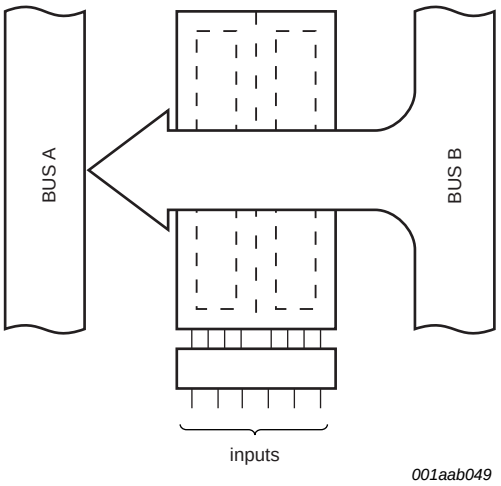
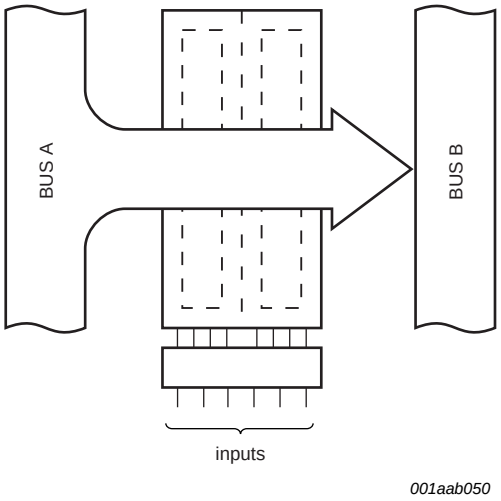
12. Application information



Values for inputs are given in Table 10.

Fig 12. Real-time transfer; bus B to bus A



Values for inputs are given in Table 10.

Fig 13. Real-time transfer; bus A to bus B

Table 10. Real-time transfer[1]

Direction	Input					
	$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
Bus B to bus A	L	L	X	X	X	L
Bus A to bus B	L	H	X	X	L	X

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care

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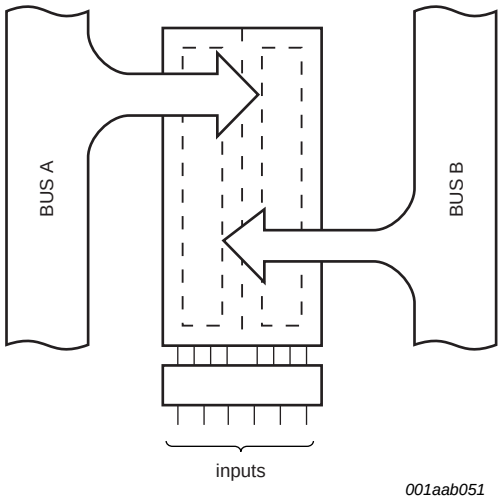
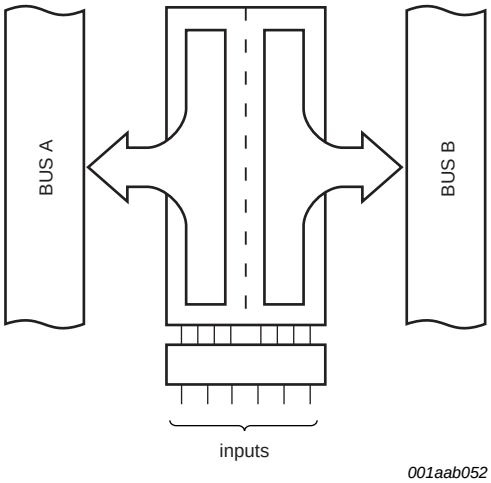


Values for inputs are given in Table 11.

Fig 14. Bus A and bus B to storage



Values for inputs are given in Table 11.

Fig 15. Storage to bus A or bus B

Table 11. Storage transfer[1]

Function	Input					
	$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
Bus A to storage	X	X	↑	X	X	X
Bus B to storage	X	X	X	↑	X	X
Bus A and B to storage	H	X	↑	↑	X	X
Storage to bus A	L	L	X	H or L	X	H
Storage to bus B	L	H	H or L	X	H	X

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW to HIGH level transition

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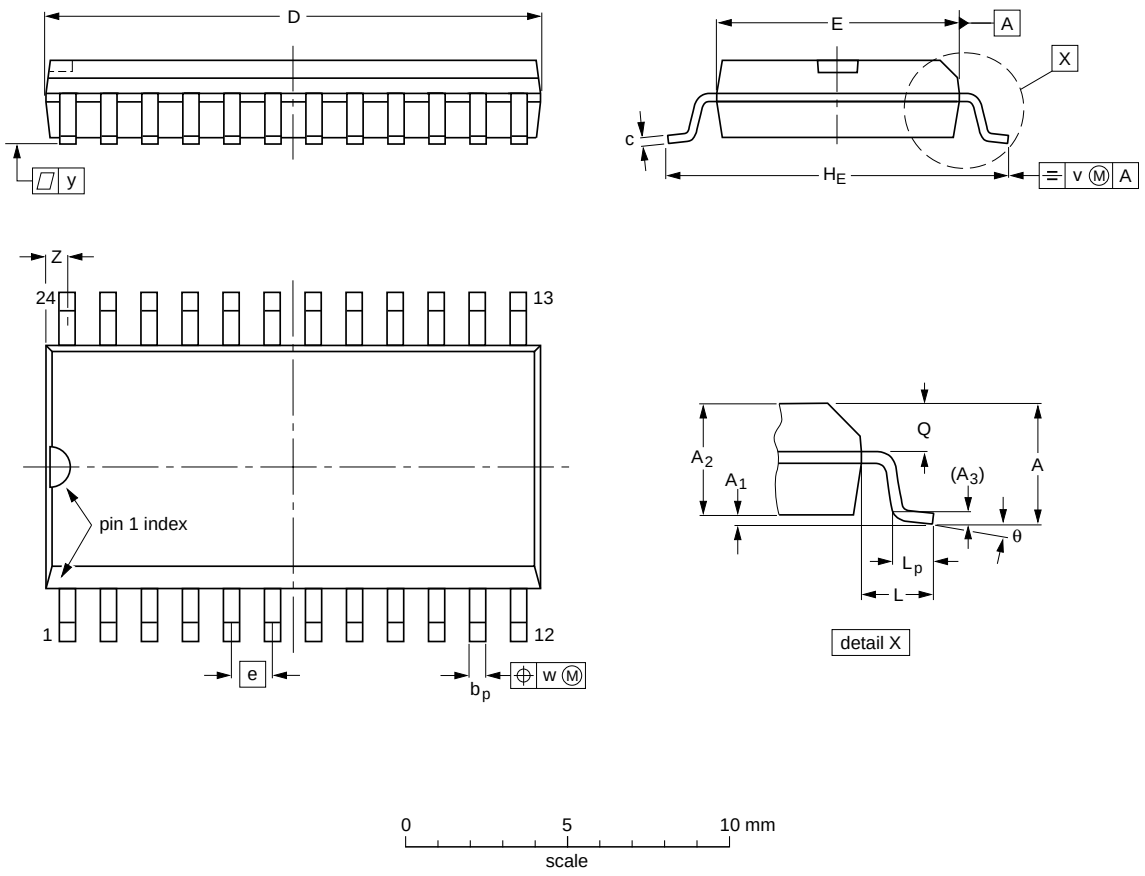
13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT137-1 (SO24)

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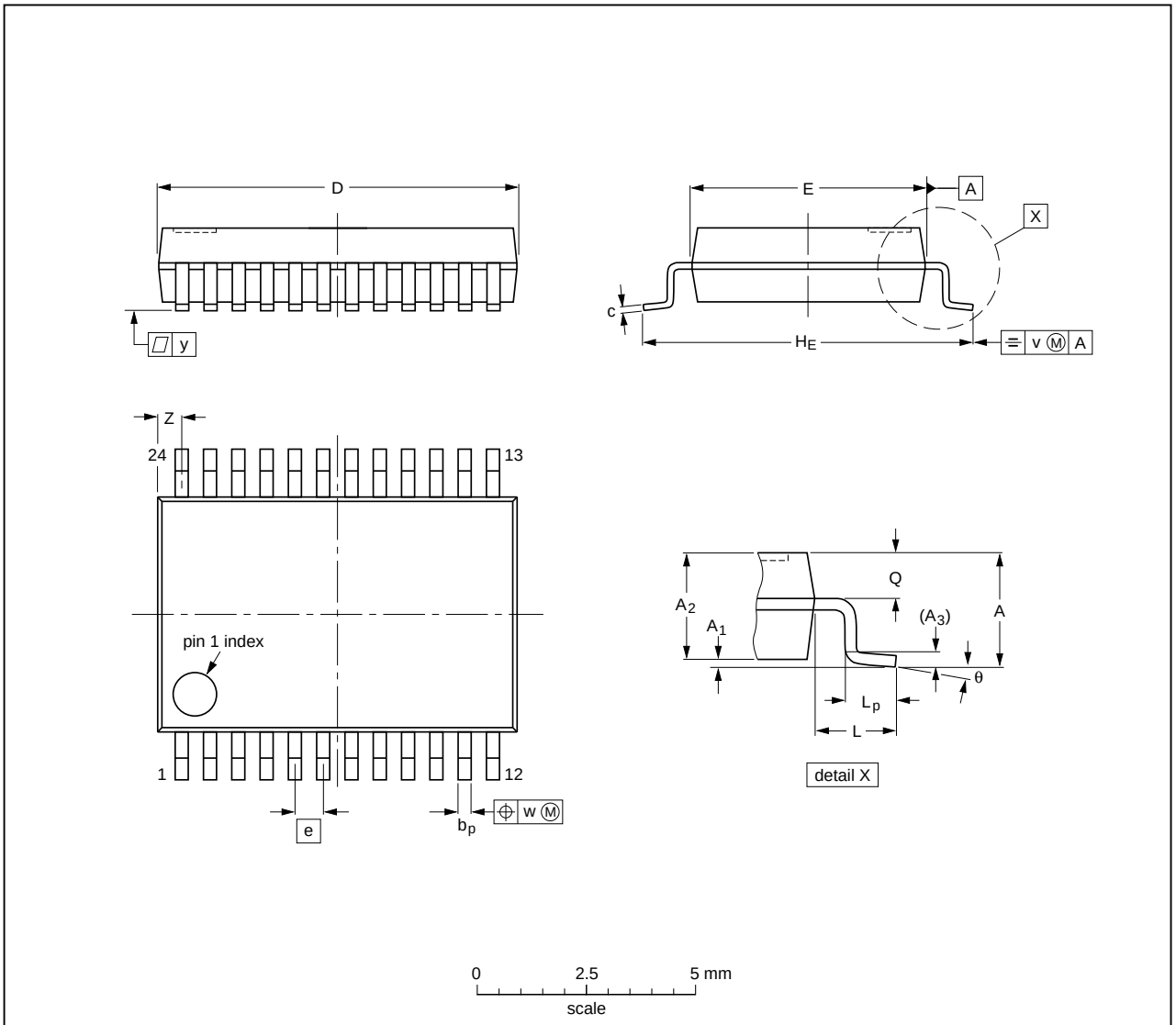
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT340-1 (SSOP24)

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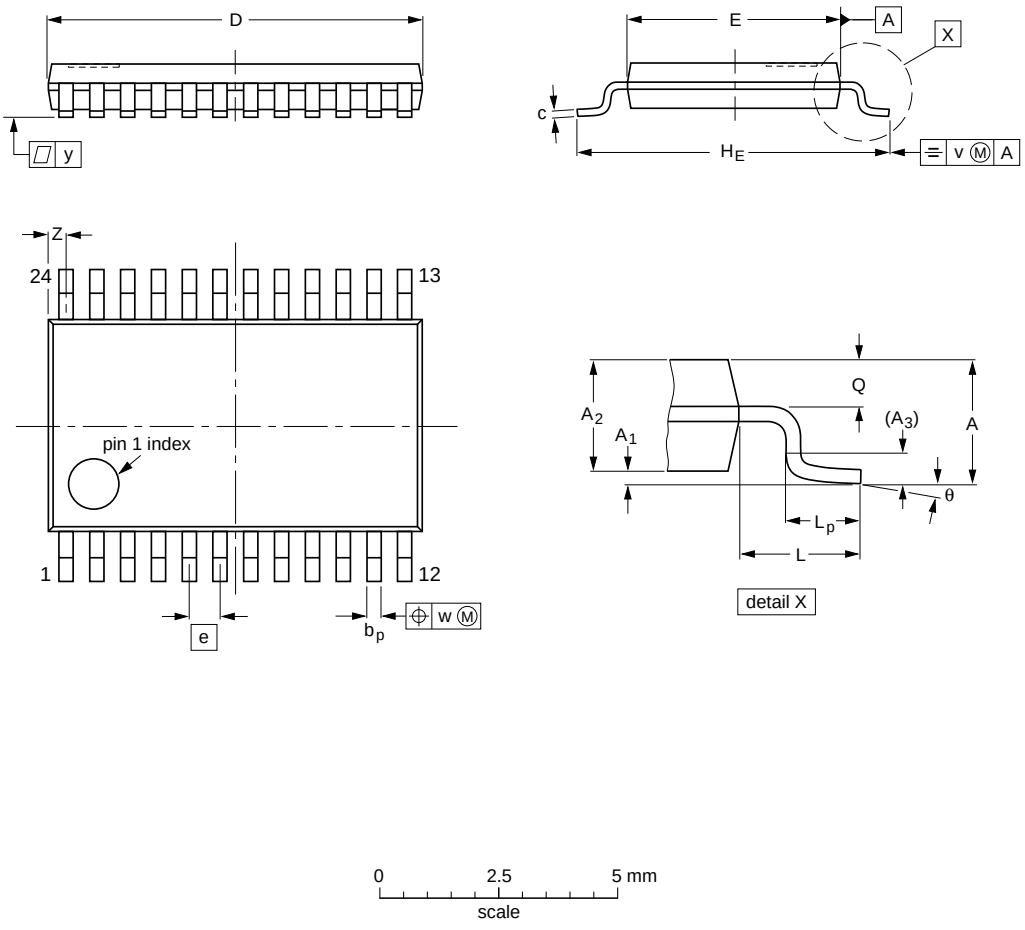
TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT355-1 (TSSOP24)

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14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC646A v.5	20130328	Product data sheet	-	74LVC646A v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges.			
74LVC646A v.4	20040629	Product specification	-	74LVC646A v.3
74LVC646A v.3	20000621	Product specification	-	74LVC646A v.2
74LVC646A v.2	19980729	Product specification	-	74LVC646A v.1
74LVC646A v.1	19980325	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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