Power Amplifier Module for LTE and 5G

The AFSC5G40E38 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS power amplifiers are designed for TDD and FDD LTE systems.

3700–4000 MHz

- Typical LTE Performance: P_{out} = 6.3 W Avg., V_{DD} = 28 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF. (1)

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3710 MHz	26.1	–27.2	38.3
3800 MHz	26.6	–26.7	39.5
3900 MHz	27.5	–25.7	39.3
3990 MHz	28.5	–23.9	37.6

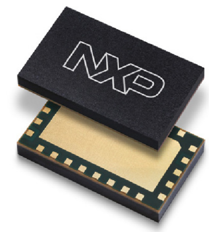
1. All data measured with device soldered in NXP reference circuit.

Features

- Frequency: 3700–4000 MHz
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity analog or digital linearization systems

AFSC5G40E38

3700–4000 MHz, 27 dB, 6.3 W Avg. AIRFAST POWER AMPLIFIER MODULE



10 mm × 6 mm Module

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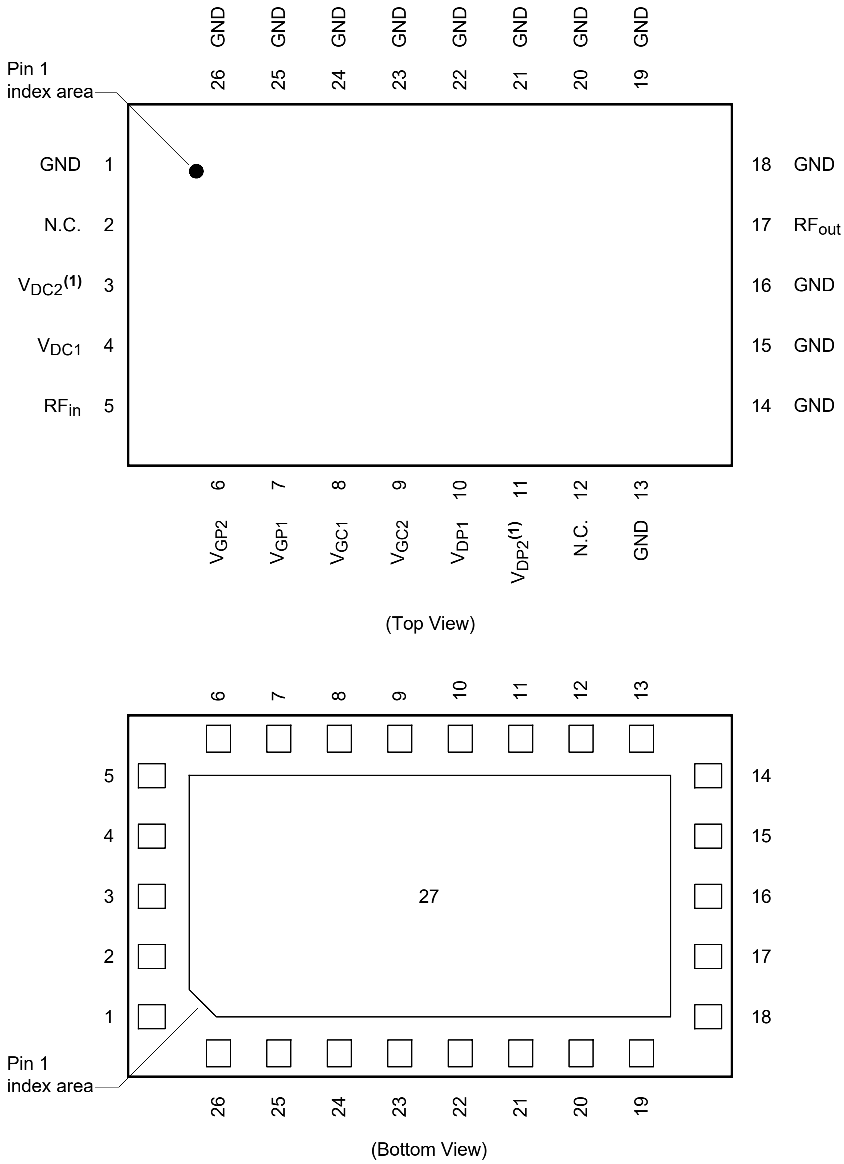

Note: Exposed backside of the package is DC and RF ground.

Figure 1. Pin Connections

1. V_{DC2} and V_{DP2} are DC coupled internal to the package and must be powered by a single DC power supply.

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Table 1. Functional Pin Description

Pin Number	Pin Function	Pin Description
1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	GND	Ground
2, 12	N.C.	No Connection
3	V_{DC2}	Carrier Drain Supply, Stage 2
4	V_{DC1}	Carrier Drain Supply, Stage 1
5	RF_{in}	RF Input
6	V_{GP2}	Peaking Gate Supply, Stage 2
7	V_{GP1}	Peaking Gate Supply, Stage 1
8	V_{GC1}	Carrier Gate Supply, Stage 1
9	V_{GC2}	Carrier Gate Supply, Stage 2
10	V_{DP1}	Peaking Drain Supply, Stage 1
11	V_{DP2}	Peaking Drain Supply, Stage 2
17	RF_{out}	RF Output

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Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Gate-Bias Voltage Range	V_G	–0.5 to +10	Vdc
Operating Voltage Range	V_{DD}	24 to 30	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	125	°C
Peak Input Power (3950 MHz, Pulsed CW, 10 μsec(on), 10% Duty Cycle)	P_{in}	25	dBm

Table 3. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure Case Temperature 125°C, 6.3 W Avg., 30 Vdc	MTTF	> 10	Years

Table 4. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1A
Charge Device Model (per JS-002-2014)	C2b

Table 5. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

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Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
Carrier Stage 1 — On Characteristics				
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 1.6 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 15 mAdc)	$V_{GS(Q)}$	1.9	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = 15 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.8	±1.4	Vdc
Carrier Stage 2 — On Characteristics				
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 14.4 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 50 mAdc)	$V_{GS(Q)}$	1.8	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 50 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	2.7	±1.2	Vdc
Peaking Stage 1 — On Characteristics [1]				
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 2.0 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 5.1 μAdc)	$V_{GS(Q)}$	1.2	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = 5.1 μAdc, Measured in Functional Test)	$V_{GG(Q)}$	1.2	±0.4	Vdc
Peaking Stage 2 — On Characteristics [1]				
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 27.2 μAdc)	$V_{GS(th)}$	1.2	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 16.7 μAdc)	$V_{GS(Q)}$	1.2	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 16.7 μAdc, Measured in Functional Test)	$V_{GG(Q)}$	1.2	±0.4	Vdc

1. Each side of device measured separately.

(continued)

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Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests — 3800 MHz [1] (In NXP Doherty Production ATE [2] Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 15 mA, I_{DQ2A} = 50 mA, V_{GS1B} = (V_t – 0.21) Vdc, V_{GS2B} = (V_t – 0.20) Vdc, P_{out} = 6.3 W Avg., 1-tone CW, f = 3800 MHz.					
Gain	G	24.8	26.7	—	dB
Drain Efficiency	η_D	34.5	43.5	—	%
P_{out} @ 3 dB Compression Point	P3dB	43.6	44.4	—	dBm
Functional Tests — 4000 MHz [1] (In NXP Doherty Production ATE [2] Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 15 mA, I_{DQ2A} = 50 mA, V_{GS1B} = (V_t – 0.21) Vdc, V_{GS2B} = (V_t – 0.20) Vdc, P_{out} = 6.3 W Avg., 1-tone CW, f = 4000 MHz.					
Gain	G	27.1	28.8	—	dB
Drain Efficiency	η_D	33.0	38.0	—	%
P_{out} @ 3 dB Compression Point	P3dB	42.9	43.7	—	dBm
Wideband Ruggedness [3] (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) I_{DQ1A} = 15 mA, I_{DQ2A} = 50 mA, V_{GSP1} = 1.3 Vdc, V_{GSP2} = 1.3 Vdc, f = 3900 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 30 Vdc, 3 dB Input Overdrive from 6.3 W Avg. Modulated Output Power	No Device Degradation				
Typical Performance [3] (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 15 mA, I_{DQ2A} = 50 mA, V_{GSP1} = 1.3 Vdc, V_{GSP2} = 1.3 Vdc, P_{out} = 6.3 W Avg., 3900 MHz					
VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	241	—	MHz
Quiescent Current Accuracy over Temperature [4] with 2.2 kΩ Gate Feed Resistors (–40 to 105°C) Stage 1 with 2.2 kΩ Gate Feed Resistors (–40 to 105°C) Stage 2	ΔI_{QT}	 — —	 1.0 6.0	 — —	%
1-carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	27.5	—	dB
Power Added Efficiency	PAE	—	39.3	—	%
Adjacent Channel Power Ratio	ACPR	—	–25.7	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–38.8	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–44.8	—	dBc
Gain Flatness [5]	G_F	—	2.4	—	dB
Fast CW, 27 ms Sweep					
P_{out} @ 3 dB Compression Point	P3dB	—	45.5	—	dBm
AM/PM @ P3dB	Φ	—	–46	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +105°C)	ΔG	—	0.025	—	dB/°C
P3dB Variation over Temperature (–40°C to +105°C)	ΔP3dB	—	0.014	—	dB/°C

Table 7. Ordering Information

Device	Tape and Reel Information	Package
AFSC5G40E38T2	T2 Suffix = 2,000 Units, 24 mm Tape Width, 13-inch Reel	10 mm × 6 mm Module

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. All data measured in fixture with device soldered in NXP reference circuit.
4. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
5. Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High}))

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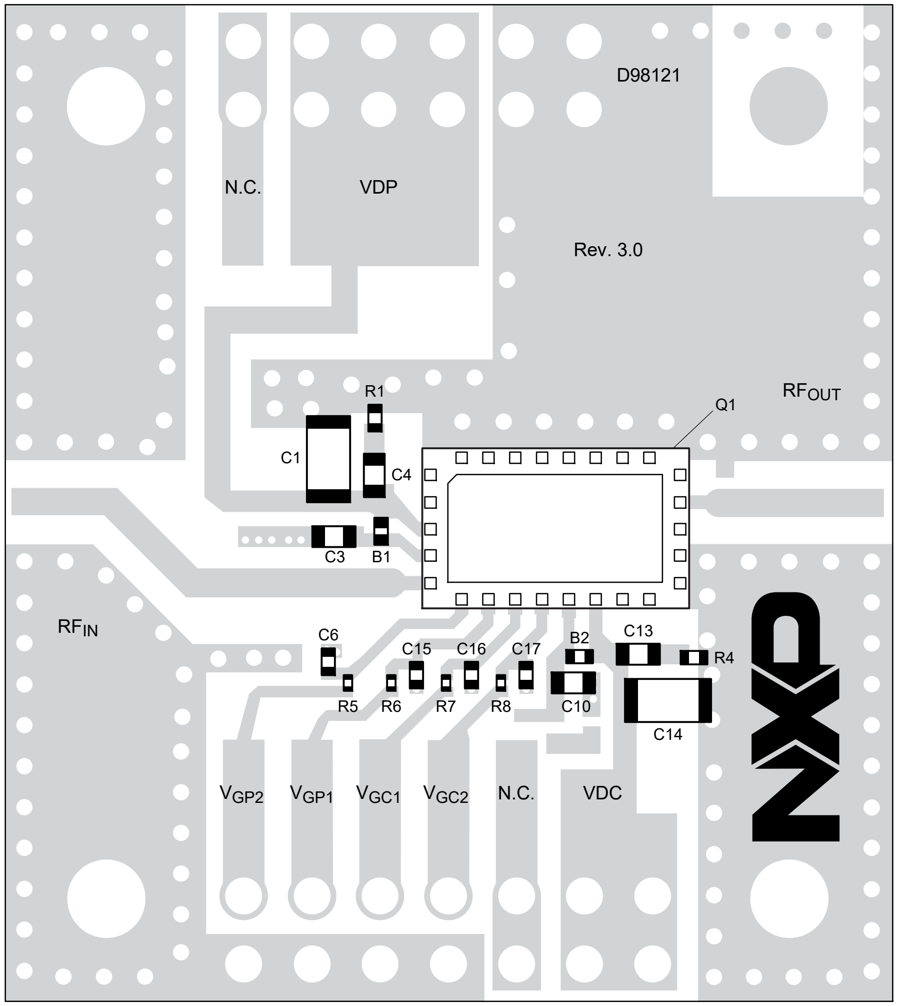

Figure 2. AFSC5G40E38 Reference Circuit Component Layout

Table 8. AFSC5G40E38 Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	30 Ω Ferrite Bead	BLM15PD300SN1	Murata
C1, C14	10 μF Chip Capacitor	CL31A106KBHNNNE	Samsung
C3, C4, C10, C13	1 μF Chip Capacitor	06035D105KAT2A	AVX
C6, C15, C16, C17	0.1 μF Chip Capacitor	GRM155R61H104KE14	Murata
Q1	Power Amplifier Module	AFSC5G40E38	NXP
R1, R4	5.1 Ω, 1/10 W Chip Resistor	ERJ-2GEJ5R1X	Panasonic
R5, R6, R7, R8	2.2 kΩ, 1/20 W Chip Resistor	ERJ-1GNJ222C	Panasonic
PCB	Rogers RO4350B, 0.020″, ε_r = 3.67	D98121	MTL

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.

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Figure 3. Product Marking

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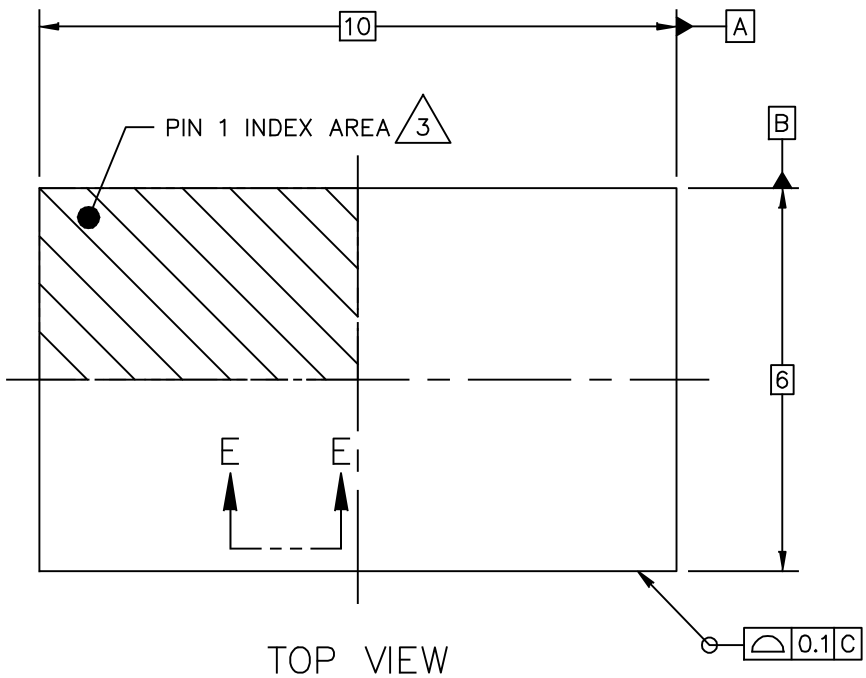
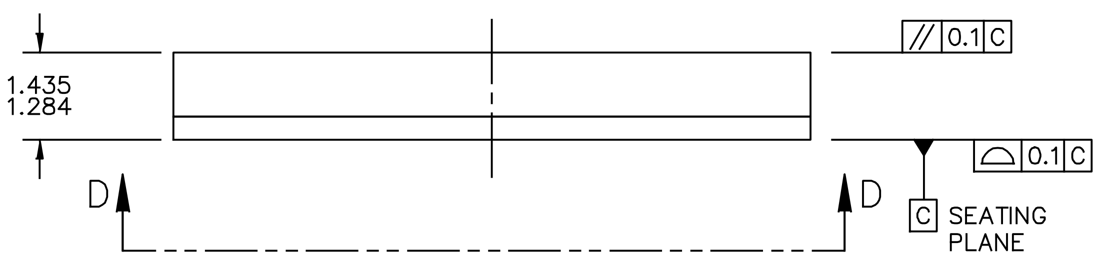
H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2





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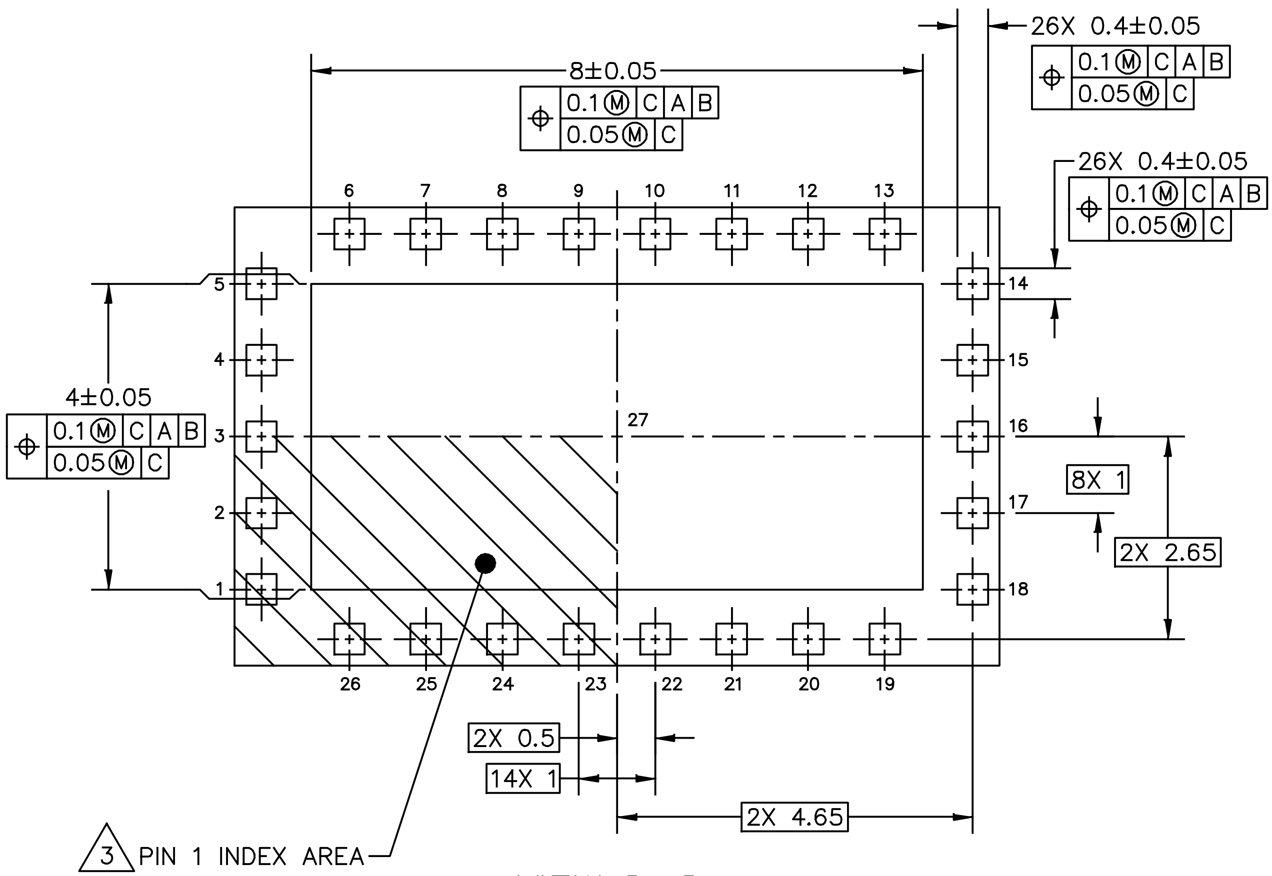
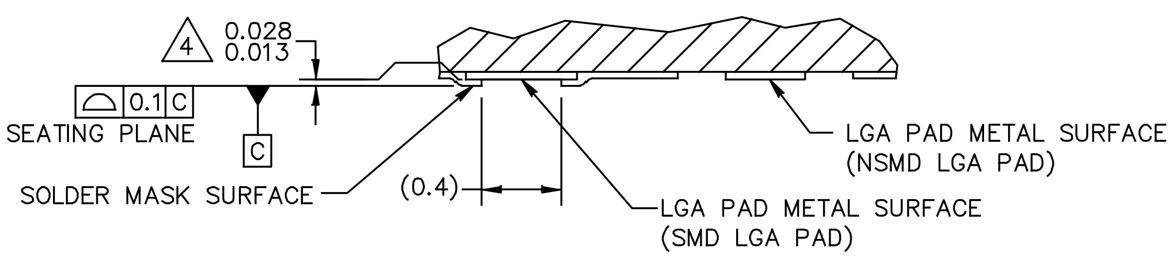


VIEW D-D
(BOTTOM VIEW)



SECTION E-E 5

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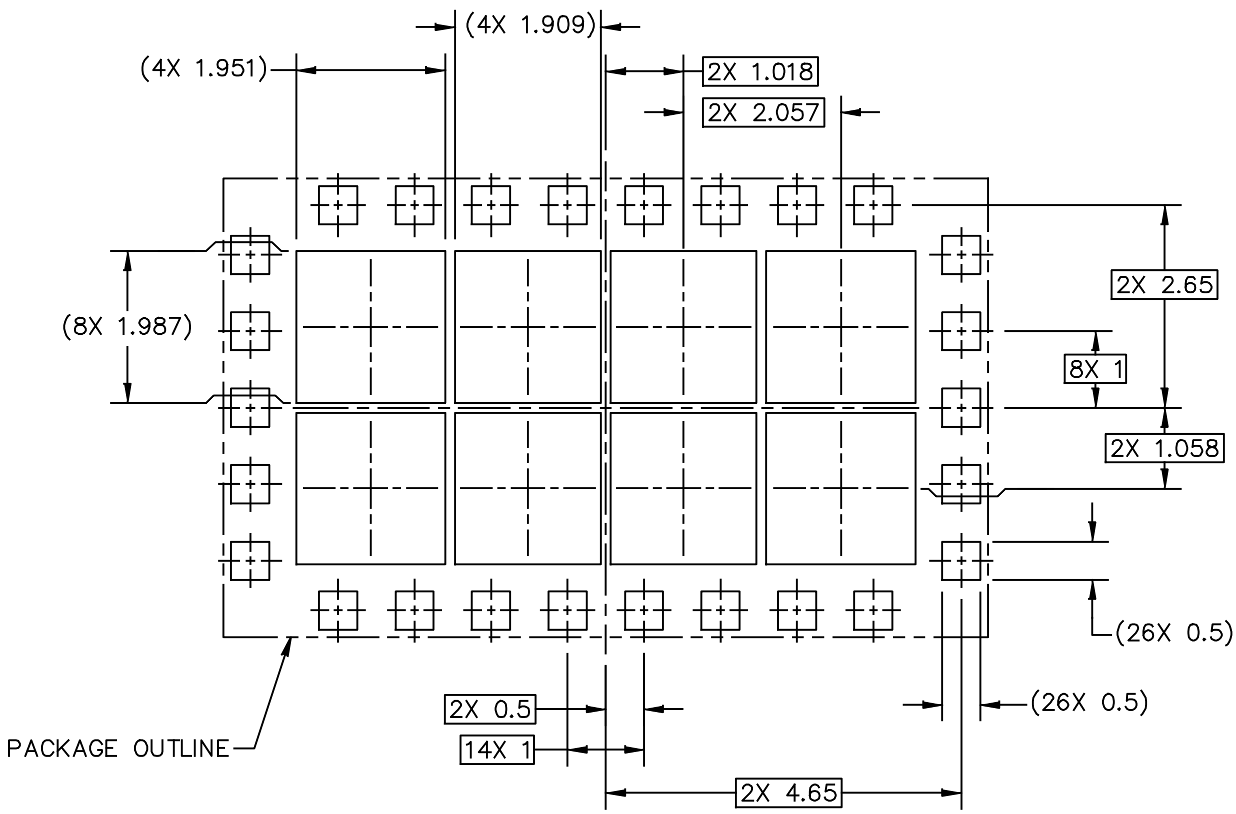

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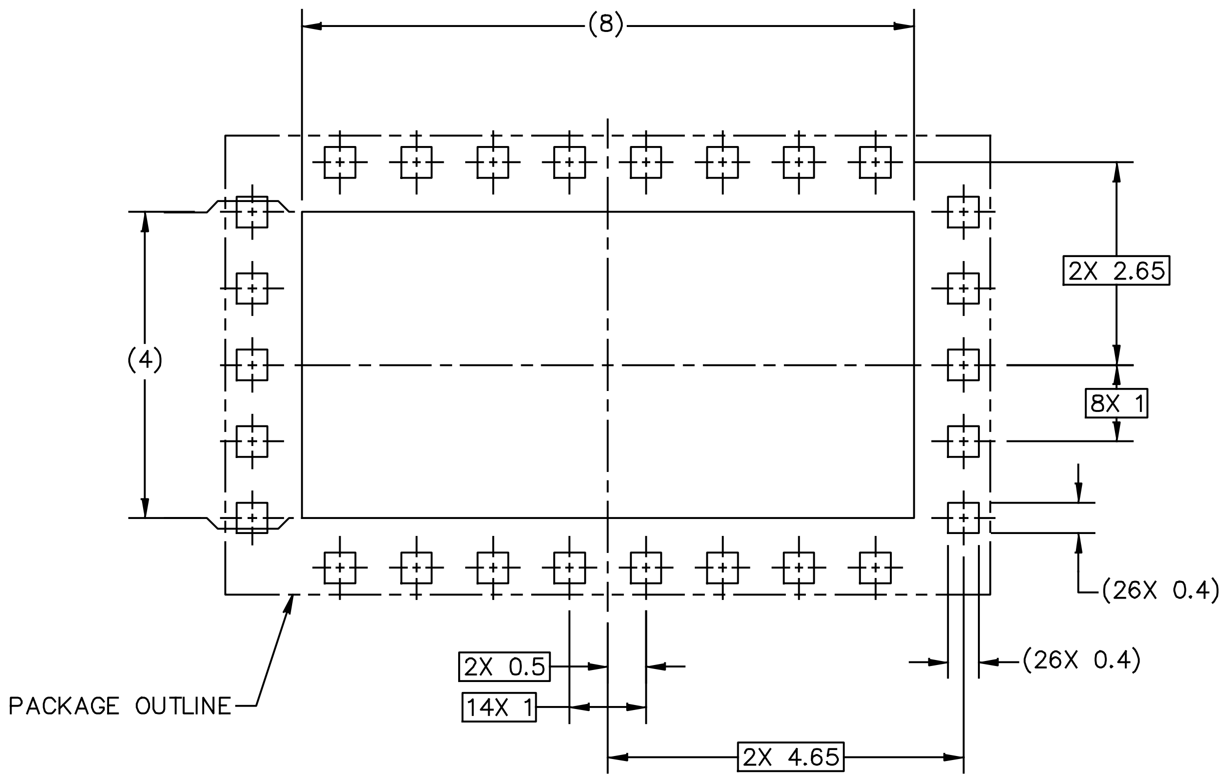

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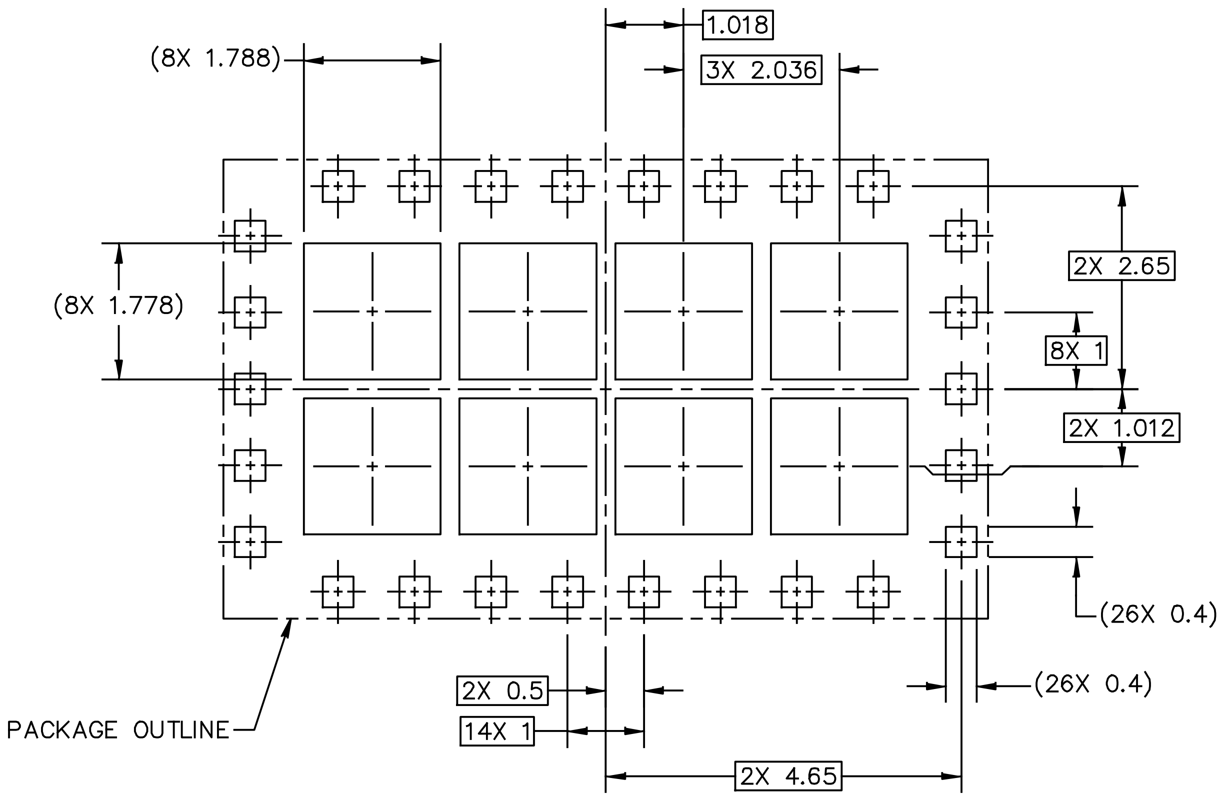

RECOMMENDED STENCIL THICKNESS 0.125

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

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PRODUCT DOCUMENTATION AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Development Tools

- Printed Circuit Boards

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2020	• Initial release of data sheet

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