PCA2117

Automotive LCD driver for character displays

Rev. 4 — 8 April 2015 Product data sheet

1. General description

The PCA2117 is a low-power Liquid Crystal Display (LCD)[1] controller and driver. It is specifically designed to drive LCD dot-matrix displays of 2-lines by 20 characters or 1-line by 40 characters with 5 × 8 dot format. In addition 200 icons can be displayed. The chip contains a character generator and displays alphanumeric characters. The PCA2117 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA2117 offers a programmable temperature compensation of the LCD supply voltage. The PCA2117 can be easily connected to a microcontroller by either the two-line I^2C-bus or a four-line bidirectional SPI-bus.

Various character sets can be manufactured on request. In addition up to 48 user-defined symbols (5 × 8 dot format) can be stored in three selectable RAM columns with 16 characters each.

For a selection of NXP LCD character drivers, see Table 58 on page 97.

2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Single-chip LCD controller and driver
- Extended operating temperature range from −40 °C to +105 °C
- 2-line display of up to 20 characters plus 200 icons or 1-line display of up to 40 characters plus 200 icons
- 5 × 7 character format plus cursor and user-defined symbols
- Icon blink function
- On-chip:
  - Programmable 4, 3, or 2 times voltage multiplier generating LCD supply voltage (external supply also possible)
  - Integrated temperature sensor with temperature readout
  - Selectable linear temperature compensation of on-chip generated V_{LCD}
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Readout of RAM, CGROM, and all registers possible
- Diagnostic features:
  - Checksum on I^2C and SPI bus
- Frame frequency: programmable from 45 Hz to 360 Hz
- Display Data RAM (DDRAM): 80 characters

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Character Generator ROM (CGROM): 240, 224, or 208 characters (5 × 8) depending on the selected RAM size
- Character Generator RAM (CGRAM): 16, 32, or 48 characters (5 × 8); ICON-RAM: 400 bit
- Two-line I^2C-bus interface or four-line SPI bus selectable through input pin
- Inversion modes
  - n-line (n = 1 to 7) inversion
  - Frame inversion
- Large supply voltage range: V_{DD1}: 2.5 V to 5.5 V (chip can be driven with battery cells)
- Analog supply voltage V_{DD2}: 2.5 V to 5.5 V
- LCD supply voltage V_{LCD}: 4 V to 16 V
- Direct mode to save current consumption for icon mode and multiplex drive mode 1:9 (depending on V_{DD2} value and LCD properties)
- Power-down mode pin
- Very low current consumption (20 μA to 200 μA):
  - Power-down mode: < 2 μA
  - Icon mode: < 25 μA
- Icon mode is used to save current. When only icons are displayed, a much lower LCD operating voltage can be used and the switching frequency of the LCD driver outputs is reduced. In this case, for most applications it is possible to use V_{DD} as LCD supply voltage

3. Applications

- Automotive
  - Instrument clusters
  - Climate control display
  - Car entertainment
  - Car radio
- Industrial
  - Medical and health care
  - Measuring equipment
  - Machine control systems
  - Information boards
  - General-purpose display modules
- Consumer
  - White goods
  - Home entertainment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA2117DUGR	bare die	244 bumps	PCA2117DUG
PCA2117DUGS			

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA2117DUGR/DA	935301518033	PCA2117DUGR/DAZ	1	character set R; chips with gold bumps in tray
PCA2117DUGS/DA	935303241033	PCA2117DUGS/DAZ	1	character set S; chips with gold bumps in tray

5. Marking

Each die has a laser marking on the rear side. The format is LLLLLLLWWXXXXXX having the following meaning:

LLLLLLL - wafer lot number

WW - wafer number

XXXXXX - die identification number

6. Block diagram

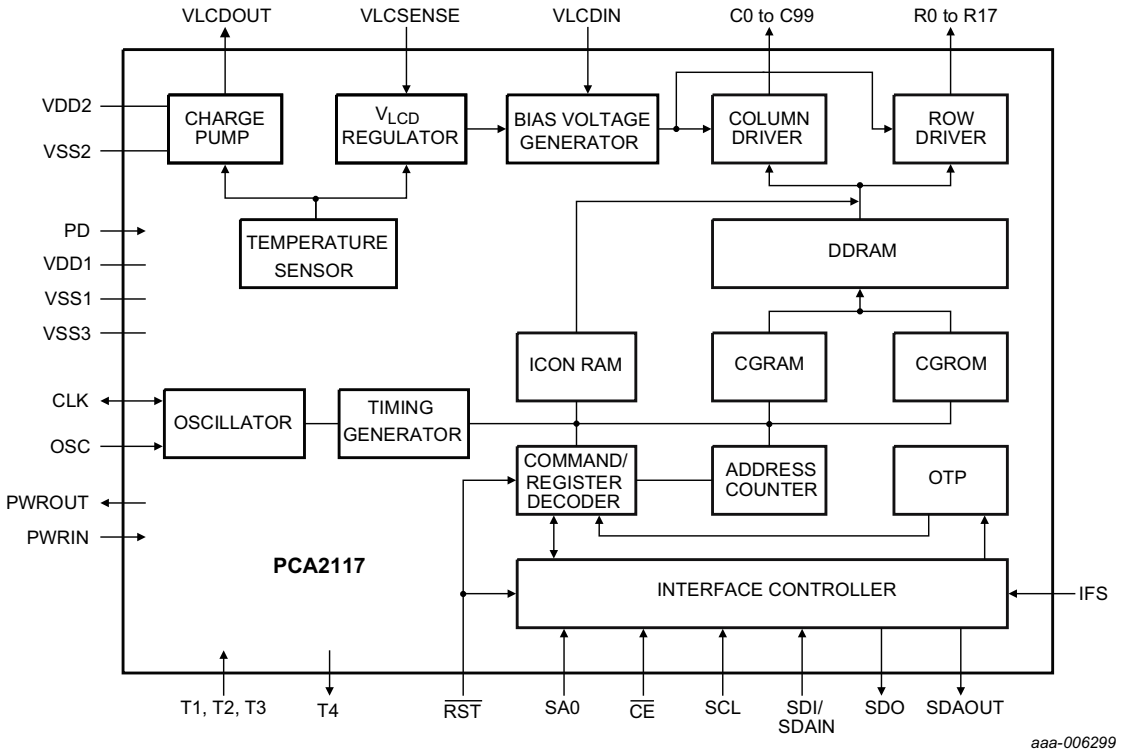
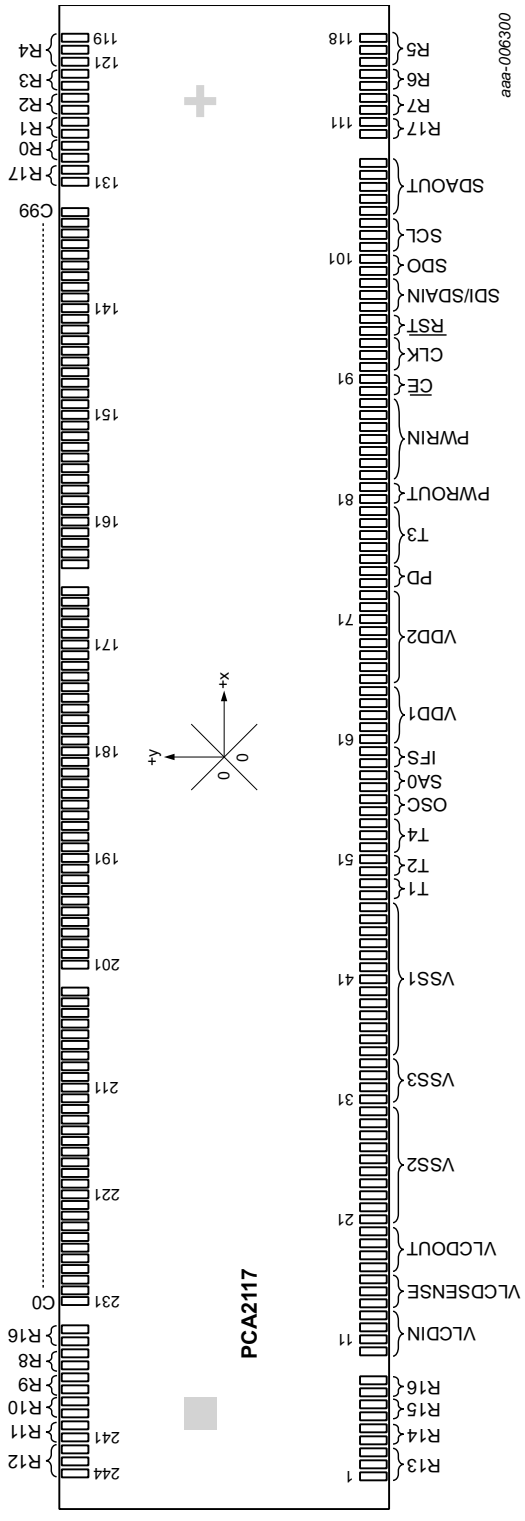


Fig 1. Block diagram of PCA2117

7. Pinning information

7.1 Pinning



Viewed from active side. For mechanical details, see Figure 61 on page 89.

Fig 2. Pinning diagram of PCA2117DUGx

7.2 Pin description

Table 3. Pin description of PCA2117DUGx

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
Row output pins			
R13	1 to 3	output	LCD row driver output
R14	4, 5		
R15	6, 7		
R16	8, 9, 232, 233	output	LCD row driver output for driving the icons
R17	110, 111, 130, 131		
R7	112, 113	output	LCD row driver output
R6	114, 115		
R5	116 to 118		
R4	119 to 121		
R3	122, 123		
R2	124, 125		
R1	126, 127		
R0	128, 129		
R8	234, 235		
R9	236, 237		
R10	238, 239		
R11	240, 241		
R12	242 to 244		
Column output pins			
C99 to C0	132 to 231	output	LCD column driver output
V_{LCD} pins			
VLCDIN	10 to 13	supply	V_{LCD} input
VLCDSENSE	14 to 16	input	V_{LCD} regulation input
VLCDOUT	17 to 20	output	V_{LCD} output
Supply pins			
VSS2[1]	21 to 30	supply	ground supply
VSS3[1]	31 to 34		
VSS1[1]	35 to 47		
VDD1	61 to 65	supply	supply voltage 1
VDD2	66 to 73	supply	supply voltage 2
PWROUT	81, 82	output	regulated voltage output; must be connected to PWRIN
PWRIN	83 to 89	input	regulated voltage input; must be connected to PWROUT
Test pins			
T1	48, 49	input	not accessible; must be connected to V_{SS1}
T2	50, 51		
T4	52 to 54	output	not accessible; must be left open

Table 3. Pin description of PCA2117DUGx *…continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description	
T3	76 to 80	input	not accessible; must be connected to PWROUT	
Oscillator, synchronization, and reset pins				
OSC[2]	55, 56	input	clock (internal/external) selector	
PD	74, 75	input	power-down mode select • for normal operation, pin PD must be LOW • for power-down mode, pin PD must be HIGH	
CLK	92 to 94	input/output	internal oscillator output, external oscillator input	
$\overline{RST}$	95, 96	input	active LOW reset input	
Bus-related pins				
			SPI-bus	**I²C-bus**
SA0	57, 58	input	unused; • connect to V_{SS1}	slave address selector; • connect to V_{SS1} for logic 0 • connect to V_{DD1} for logic 1
IFS	59, 60	input	interface selector input • connect to V_{SS1}	interface selector input • connect to V_{DD1}
$\overline{CE}$	90, 91	input	chip enable input (active LOW)	unused • connect to V_{DD1}
SDI/SDAIN	97 to 99	input	SPI-bus data input	I²C-bus serial data input
SDO	100, 101	output	SPI serial data output	unused • must be left open
SCL	102 to 104	input	serial clock input	serial clock input
SDAOUT	105 to 109	output	unused • must be connected to V_{SS1}	serial data output

[1] The substrate (rear side of the die) is at V_{SS1} potential and must not be connected.

[2] If pin OSC is tied to V_{SS1}, CLK is the output pin of the internal oscillator. If pin OSC is tied to V_{DD1}, CLK is the input pin for the external oscillator.

8. Functional description

8.1 Commands of PCA2117

The commands defined in Table 5 control the PCA2117.

The sequence to execute a command is like shown in Table 4:

Table 4. Command execution sequence

Bus	Byte 1	Byte 2	Byte 3
I^2C	slave address[1] + R/$\overline{W}$[2]	CO + RS[1:0][3]	command
SPI	R/$\overline{W}$[2] + subaddress[4]	CO + RS[1:0][3]	command

[1] More about the slave address, see Section 9.2.7.

[2] See Section 9.2.7 and Section 9.3.1.

[3] See Section 9.1.

[4] More about the subaddress, see Section 9.3.1.

Remark: Any other combinations of operation code bits that are not mentioned in this document can lead to undesired operation modes of PCA2117.

Table 5. Commands of PCA2117

Command name	R/$\overline{W}$	Register select		Bits								Reference
		RS[1:0]		7	6	5	4	3	2	1	0	
General control commands												
Register_update	0	0	0	0	0	0	0	0	0	0	0	Section 8.1.1.1
Initialize				0	0	0	0	0	0	0	1	Section 8.1.1.2
Clear_reset_flag				0	0	0	1	1	1	1	1	Section 8.1.1.3
OTP_refresh				0	0	0	0	0	0	1	0	Section 8.1.1.4
Clock_out_ctrl				0	0	1	0	0	0	0	COE	Section 8.1.1.5
Read_reg_select				0	0	0	0	0	1	XC	SO	Section 8.1.1.6
Read_status_reg	1			TD[7:0]								Section 8.1.1.7
				CS[7:0]								
				Status_Register_1 to Status_Register_9								
RAM_ROM_config	0			0	1	0	1	0	0	RR[1:0]		Section 8.1.1.8
Sel_mem_bank				0	0	0	1	0	SMB[2:0]			Section 8.1.1.9
Set_mem_addr				1	ADD[6:0]							Section 8.1.1.10
Read_data	1	0	1	RD[7:0]								Section 8.1.1.11
				0	0	0	RD[4:0]					
Write_data	0			WD[7:0]								Section 8.1.1.12
				0	0	0	WD[4:0]					

Table 5. Commands of PCA2117 *…continued*

Command name	R/$\overline{W}$	Register select		Bits								Reference
		RS[1:0]		7	6	5	4	3	2	1	0	
Display control commands												
Clear_display	0	1	0	0	0	0	0	0	0	0	0	Section 8.1.2.1
Return_home				0	0	0	0	0	0	0	1	Section 8.1.2.2
Entry_mode_set				0	0	1	0	1	0	I_D	S	Section 8.1.2.3
Function_set				0	0	1	1	0	0	M	SL	Section 8.1.2.4
Inversion_mode	0	1	0	0	1	0	0	0	INV[2:0]			Section 8.1.2.5
Frame_frequency				1	0	0	FF[4:0]					Section 8.1.2.6
Display_control				0	0	1	0	0	D	C	B	Section 8.1.2.7
Cursor_display_shift				0	0	0	1	0	0	SC	RL	Section 8.1.2.8
Screen_config				0	0	0	0	0	0	1	L	Section 8.1.2.9
Display_config				0	0	0	0	0	1	P	Q	Section 8.1.2.10
Icon_config				0	0	0	0	1	0	IM	IB	Section 8.1.2.11
Charge pump and LCD bias control commands												
Charge_pump_ctrl	0	1	1	1	0	0	0	0	CPE	CPC[1:0]		Section 8.1.3.1
Set_VLCD_A				1	0	1	VLCDA[8:4]					Section 8.1.3.2
				1	0	0	1	VLCDA[3:0]				
Set_VLCD_B				1	1	0	VLCDB[8:4]					Section 8.1.3.2
				1	1	1	0	VLCDB[3:0]				
Temperature compensation control commands												
Temperature_ctrl	0	1	1	0	0	0	0	0	TCE	TMF	TME	Section 8.1.4.1
TC_slope				0	0	0	0	1	TSA[2:0]			Section 8.1.4.2
				0	0	0	1	0	TSB[2:0]			
				0	0	0	1	1	TSC[2:0]			
				0	0	1	0	0	TSD[2:0]			

8.1.1 General control commands

8.1.1.1 Command: Register_update

This command updates registers of the PCA2117. It must be sent after the Return_home command or Cursor_display_shift command if no other command follows.

Table 6. Register_update - Register update command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00000000	**update register**

8.1.1.2 Command: Initialize

This command generates a chip-wide reset by setting all command registers to their default values. It must be sent to the PCA2117 after power-on. For further information, see Section 8.2.1 on page 27.

Table 7. Initialize - Initialize command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00000001	**initialize**

8.1.1.3 Command: Clear_reset_flag

The Clear_reset_flag command clears the reset flag CRF, see Table 12 on page 11.

Table 8. Clear_reset_flag - Clear_reset_flag command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00011111	**clear reset status flag**

8.1.1.4 Command: OTP_refresh

In order to achieve the specified accuracy of the V_{LCD}, the frame frequency, and the temperature measurement, each IC is calibrated during production. These calibration values are stored in One Time Programmable (OTP) cells. Their content is loaded into the associated registers every time when the Initialize command or the OTP_refresh command is sent. This command takes approximately 10 ms to finish.

Table 9. OTP_refresh - OTP_refresh command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00000010	**refresh register settings from OTP**

8.1.1.5 Command: Clock_out_ctrl

When pin CLK is configured as an output pin, the Clock_out_ctrl command enables or disables the clock output on pin CLK.

Table 10. Clock_out_ctrl - CLK pin input/output switch command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0010000	fixed value
0	COE		**CLK pin setting**
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

For lower power consumption, the clock is only active when display (see Table 25), charge pump (see Table 30), or temperature measurement (see Table 32) is enabled.

8.1.1.6 Command: Read_reg_select

The Read_reg_select command allows choosing to read out the temperature or the status registers (Checksum to Status_Register_9) of the device (see Table 12).

Table 11. Read_reg_select - select registers for readout command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	000001	fixed value
1	XC		**checksum mode setting**
		0[1]	XOR checksum
		1	CRC-8 checksum
0	SO		**readout select**
		0[1]	temperature
		1	status registers

[1] Default value.

[2] Only valid for RAM. See .Section 8.5.2 “Checksum”

8.1.1.7 Command: Read_status_reg

With the Read_status_reg command the temperature, checksum, and the status registers can be read out. The behavior of the Read_status_reg command is controlled by the SO bit of the Read_reg_select command (see Table 11).

Table 12. Read_status_reg - readout register command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	1	fixed value
-	RS[1:0]	00	fixed value
Temperature readout if SO = 0 (see Table 11)			
7 to 0	TD[7:0]	00000000 to 11111111[1]	**temperature readout**
Status readout if SO = 1 (see Table 11)			
Checksum			
7 to 0	CS[7:0]	00000000[1] to 11111111	**checksum result** from RAM writing with checksum mode set by bit XC (see Table 11)
Status_Register_1			
7, 6	-	00	fixed value
5, 4	RR[1:0]	see Table 13	**CGRAM and CGROM select status**
3	I_D	see Table 20	**address stepping select status**
2	S		**display shift select status**
1	M	see Table 21	**display lines setting status**
0	SL		**multiplex drive mode setting status**
Status_Register_2			
7 to 5	INV[2:0]	see Table 22	**inversion mode setting status**
4 to 0	FF[4:0]	see Table 24	**frame frequency setting status**

Table 12. Read_status_reg - readout register command bit description *...continued*

Bit	Symbol	Value	Description
Status_Register_3			
7	D	see Table 25	**display setting status**
6	C		**cursor setting status**
5	B		**character blink setting status**
4	SC	see Table 26	**shift or move setting status**
3	RL		**shift or move direction setting status**
2	L	see Table 27	**screen configuration** setting status
1	P	see Table 28	**display column setting status**
0	Q		**display row setting status**
Status_Register_4			
7	-	0	fixed value
6	IM	see Table 29	**icon mode setting status**
5	IB		**icon blink select status**
4	CPE	see Table 30	**charge pump setting status**
3	-	0	fixed value
2, 1	CPC[1:0]	see Table 30	**charge pump voltage multiplier setting status**
0	VLCDA8	see Table 31	**value of VLCDA**
Status_Register_5			
7 to 0	VLCDA[7:0]	see Table 31	**value of VLCDA**
Status_Register_6			
7	TCE	see Table 32	**temperature compensation setting status**
6	TMF		**temperature measurement filter setting status**
5 to 3	TSA[2:0]	see Table 33	**temperature compensation slope A setting status**
2 to 0	TSB[2:0]		**temperature compensation slope B setting status**
Status_Register_7			
7	TME	see Table 32	**temperature measurement setting status**
6 to 4	TSC[2:0]	see Table 33	**temperature compensation slope C setting status**
3 to 1	TSD[2:0]		**temperature compensation slope D setting status**
0	VLCDB8	see Table 31	value of VLCDB
Status_Register_8			
7 to 0	VLCDB[7:0]	see Table 31	**value of VLCDB**

Table 12. Read_status_reg - readout register command bit description *...continued*

Bit	Symbol	Value	Description
Status_Register_9			
7 to 3	-	00000	fixed value
2	QPR		**charge pump charge status**
		0	charge pump has not reached programmed value
		1	charge pump has reached programmed value
1	CRF		**reset flag status** the reset flag is set whenever a reset occurs; it should be cleared for reset monitoring (see Table 8)
		0	no reset has occurred since the reset flag register was cleared last time
		1[1]	reset has occurred since the reset flag register was cleared last time
0	COE	see Table 10	**CLK pin setting status**

[1] Start-up value.

8.1.1.8 Command: RAM_ROM_config

The RAM_ROM_config command allows configuring the display memory.

Table 13. RAM_ROM_config - display memory configuration command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	010100	fixed value
1, 0	RR[1:0]		**CGRAM and CGROM select** (see Section 8.5)
		00[1]	column 1 (address 0001) = CGROM column 2 (address 0010) = CGROM
		01	column 1 (address 0001) = CGROM column 2 (address 0010) = CGRAM
		10	column 1 (address 0001) = CGRAM column 2 (address 0010) = CGROM
		11	column 1 (address 0001) = CGRAM column 2 (address 0010) = CGRAM

[1] Default value.

8.1.1.9 Command: Sel_mem_bank

The Sel_mem_bank command determines which memory to access.

Table 14. Sel_mem_bank - RAM access configuration command

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	00010	fixed value
2 to 0	SMB[2:0]		**RAM access select**
		000[1]	DDRAM is selected
		001	column 0 (0000) of CGRAM is selected
		010	column 1 (0001) of CGRAM is selected
		011	column 2 (0010) of CGRAM is selected
		100	ICON-RAM is selected
		101	CGROM
		110 to 111	not implemented

[1] Default value.

8.1.1.10 Command: Set_mem_addr

The Set_mem_addr command allows setting the RAM address in the address counter to access. The Sel_mem_bank command (see Section 8.1.1.9) determines whether to access the CGRAM, DDRAM, or ICON-RAM.

Table 15. Set_mem_addr - memory address command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7	-	1	fixed value
6 to 0	ADD[6:0]	0000000[1] to 1111111	**RAM address**

[1] Default value.

8.1.1.11 Command: Read_data

The Read_data command reads binary 8-bit data from the CGRAM, CGROM, DDRAM or ICON-RAM.

Table 16. Read_data - data read bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	1	fixed value
-	RS[1:0]	01	fixed value
DDRAM and CGROM			
7 to 0	RD[7:0]	00000000 to 11111111	**read data from DDRAM and CGROM**
CGRAM and ICON-RAM			
7 to 5	-	000	fixed value
4 to 0	RD[4:0]	00000 to 11111	**read data from CGRAM and ICON-RAM**

The Sel_mem_bank command (see Section 8.1.1.9) determines whether to read from the CGRAM, CGROM, DDRAM, or ICON-RAM. After reading, the address counter automatically increments or decrements by 1 in accordance with the setting of bit I_D of the Entry_mode_set command (see Section 8.1.2.3).

Only bit 4 to bit 0 of the CGRAM or ICON-RAM data are valid. Bit 7 to bit 5 are set logic 0.

8.1.1.12 Command: Write_data

The Write_data command writes binary 8-bit data to the CGRAM, DDRAM or ICON-RAM.

Table 17. Write_data - data write bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	01	fixed value
DDRAM			
7 to 0	WD[7:0]	00000000 to 11111111	**write data to DDRAM**
CGRAM and ICON-RAM			
7 to 5	-	000	not implemented
4 to 0	WD[4:0]	00000 to 11111	**write data to CGRAM and ICON-RAM**

The Sel_mem_bank command determines whether to write data into the CGRAM, DDRAM or ICON-RAM. After writing, the address counter automatically increments or decrements by 1 in accordance with the setting of bit I_D of the Entry_mode_set command (see Section 8.1.2.3).

Only bit 4 to bit 0 of the CGRAM or ICON-RAM data are valid. Bit 7 to bit 5 are not implemented and should always be logic 0. The cursor and the character blink have to be turned off when writing to the CGRAM (see Table 25 on page 20).

- The ICON-RAM to display mapping is given in Section 8.5.5 “ICON-RAM”.
- The DDRAM to display mapping is given in Section 8.5.6 “DDRAM”.

8.1.2 Display control commands

8.1.2.1 Command: Clear_display

The Clear_display command clears the entire display.

Table 18. Clear_display - clear display bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 0	-	00000000	**clear display**

Clear_display: Writes the character code 20h (blank pattern) into all DDRAM addresses except for the character set ‘R’ where the character code 20h is not a blank pattern.

When using character set ‘R’, use the following alternative instruction:

1. Switch off display (Display_control, bit D = 0).
2. Write a blank pattern into all DDRAM addresses (Write_data).
3. Switch on display (Display_control, bit D = 1).

The address counter remains on the previously accessed pointer, bit I_D keeps the previously programmed value.

8.1.2.2 Command: Return_home

The Return_home command sets the cursor to the left top corner of the display.

Table 19. Return_home - return home bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 0	-	00000001	**return home**

Return_home: Sets the address counter to logic 0 and switches a shifted display back to an unshifted state. The DDRAM content remains unchanged. The cursor or blink position goes to the left of the first display line. Bit I_D and bit S of the Entry_mode_set instruction remain unchanged. If no other command follows, this command must be terminated with the Register_update command.

8.1.2.3 Command: Entry_mode_set

The Entry_mode_set command sets the address stepping and the shift of the display.

Table 20. Entry_mode_set - entry mode bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	001010	fixed value
1	I_D		**address stepping select**
		0	DDRAM, CGRAM or ICON-RAM address decrements by 1, cursor moves to the left
		1[1]	DDRAM, CGRAM or ICON-RAM address increments by 1, cursor moves to the right
0	S		**display shift select**
		0[1]	display does not shift
		1	display shifts

[1] Default value.

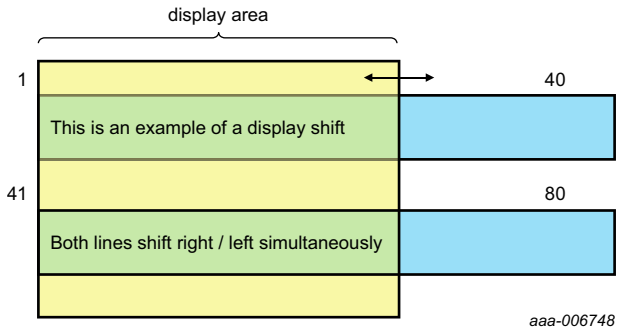
Bit I_D: When bit I_D = 1 the DDRAM, CGRAM, or ICON-RAM address increments by 1 when data is written into or read from the DDRAM, CGRAM or ICON-RAM. The cursor or blink position moves to the right.

When bit I_D = 0 the DDRAM, CGRAM, or ICON-RAM address decrements by 1 when data is written into or read from the DDRAM, CGRAM or ICON-RAM. The cursor or blink position moves to the left.

Bit S: When bit S = 0, the display does not shift.

During DDRAM write, when bit S = 1 and bit I_D = 0, the entire display shifts to the right. When bit S = 1 and bit I_D = 1, the entire display shifts to the left.

Thus it appears as if the cursor remains and the display moves. The display does not shift when reading from the DDRAM, CGRAM or ICON-RAM or when writing to or from the DDRAM, CGRAM or ICON-RAM.



Command: Entry_mode_set, S = 1, display line setting: 2 line × 20 characters.

Fig 3. Example of the display shift

8.1.2.4 Command: Function_set

The Function_set command allows setting the display lines and the multiplex drive mode.

Table 21. Function_set - function set bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	001100	fixed value
1	M		**display lines setting**
		0[1]	1 line × 40 characters
		1	2 line × 20 characters
0	SL		**multiplex drive mode setting**
		0[1]	1:18 multiplex drive mode, 1 × 40 character or 2 × 20 character display
		1	1:9 multiplex drive mode, 1 × 20 character display

[1] Default value.

8.1.2.5 Command: Inversion_mode

The Inversion_mode command allows changing the drive scheme inversion mode.

The waveforms used to drive an LCD (see Figure 27 to Figure 29) inherently produce a DC voltage across the display cell. The PCA2117 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of the compensation method is determined with INV[2:0] in Table 22.

Table 22. Inversion_mode - inversion mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01000	fixed value
2 to 0	INV[2:0]		**inversion mode setting**
		000[1]	frame inversion mode
		001	1-line inversion mode
		010	2-line inversion mode
		011	3-line inversion mode
		100	4-line inversion mode
		101	5-line inversion mode
		110	6-line inversion mode
		111	7-line inversion mode

[1] Default value.

Line inversion mode (driving scheme A): In line inversion mode, the DC value is compensated every n^{th} line. Changing the inversion mode to line inversion mode reduces the possibility for flickering but increases the power consumption.

Frame inversion mode (driving scheme B): In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is the possibility for flicker to occur.

8.1.2.6 Command: Frame_frequency

With this command, the clock and frame frequency can be programmed when using the internal clock. The default frame frequency of 80 Hz is factory calibrated.

Table 23. Frame-frequency - frame frequency select command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 5	-	100	fixed value
4 to 0	FF[4:0]	see Table 24	**frame frequency setting**

The duty cycle depends on the frequency chosen (see Table 24).

Table 24. Clock and frame frequency values

Duty cycle definition: % HIGH-level time : % LOW-level time.

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)
00000	45	36000	50 : 50
00001	50	39724	44 : 56
00010	55	44308	38 : 62
00011	60	48000	33 : 67
00100	65	52364	27 : 73
00101	70	54857	23 : 77
00110	75	60632	15 : 85
00111[1]	80	64000	11 : 89
01000	85	67765	5 : 95
01001	90	72000	50 : 50
01010	95	76800	46 : 54
01011	100	82286	42 : 58
01100	110	88615	38 : 62
01101	120	96000	33 : 67
01110	130	104727	27 : 73
01111	145	115200	20 : 80
10000	160	128000	11 : 89
10001	180	144000	50 : 50
10010	210	164571	42 : 58

Table 24. Clock and frame frequency values *...continued*

Duty cycle definition: % HIGH-level time : % LOW-level time.

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)
10011	240	192000	33 : 67
10100	290	230400	20 : 80
10101 to 11111	360	288000	50 : 50

[1] Default value.

8.1.2.7 Command: Display_control

With the Display_control command the entire display, the cursor, and the cursor blinking can be switched on or off.

Table 25. Display_control - Display control bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00100	fixed value
2	D		**display setting**
		0[1]	display is off
		1	display is on
1	C		**cursor setting**
		0[1]	cursor is off
		1	cursor is on
0	B		**character blink setting**
		0[1]	character blink is off
		1	character blink is on

[1] Default value

Bit D: The display is on when bit D = 1 and off when bit D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting bit D = 1.

Bit C: The cursor is displayed when bit C = 1 and inhibited when bit C = 0. The cursor is displayed using 5 dots in the eighth line.

Bit B: The character, indicated by the cursor, blinks when bit B = 1. The character blink is displayed by switching between display characters and all dots on with a period of 1 second.

8.1.2.8 Command: Cursor_display_shift

The Cursor_display_shift command configures whether the cursor or the display moves or shifts to right or left.

Table 26. Cursor_display_shift - cursor display shift bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	000100	fixed value
1	SC		**shift or move cursor setting**
		0[1]	move cursor
		1	cursor shift
0	RL		**shift or move direction setting**
		0[1]	left shift or move
		1	right shift or move

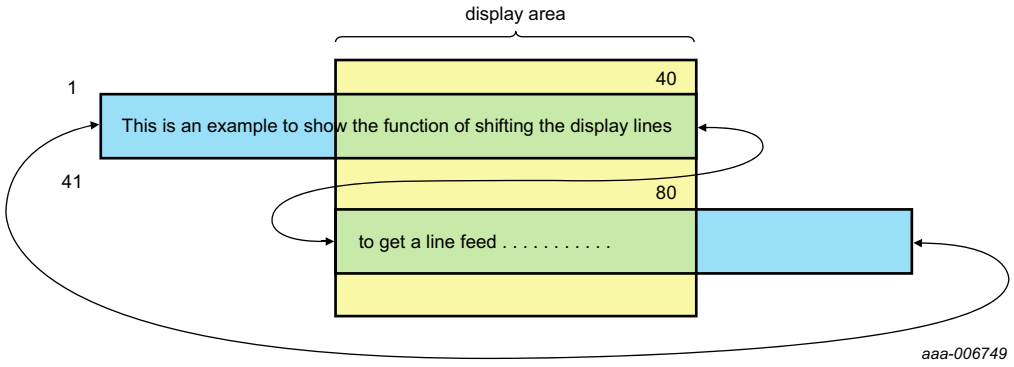
[1] Default value.

Bits SC and RL: Cursor_display_shift moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display.

In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly, all lines shift at the same time; displayed characters do not shift into the next line.

If shift display (SC = 1) is the only action performed, the address counter content does not change. But increments or decrements with shift cursor (SC = 0).

If no other command follows, this command must be terminated with the Register_update command.



Display line setting: 1 line × 40 characters; possible setups:

(1) Command Entry_mode_set: S = 1, command Cursor_display_shift: RL = 1.

(2) Command Entry_mode_set: S = 1, command Cursor_display_shift: SC = 1, RL = 1.

Fig 4. Example of a linefeed

8.1.2.9 Command: Screen_config

Table 27. Screen_config - screen configuration bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 1	-	0000001	fixed value
0	L		**screen configuration setting**
		0[1]	split screen standard connection
		1	split screen mirrored connection

[1] Default value.

Screen_config:

- If bit L = 0, then the two halves of a split screen are connected in a standard way, that is column 0/100, 1/101 to 99/199.
- If bit L = 1, then the two halves of a split screen are connected in a mirrored way, that is column 0/199, 1/198 to 99/100. This feature allows a single layer PCB or glass layout.

8.1.2.10 Command: Display_config

The Display_config command allows setting how the data is displayed.

Table 28. Display_config - display configuration bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	000001	fixed value
1	P		**display column setting**
		0[1]	column data: left to right; column data is displayed from column 0 to column 99
		1	column data: right to left; column data is displayed from column 99 to column 0
0	Q		**display row setting**
		0[1]	row data: top to bottom; row data is displayed from row 0 to row 15 and icon row data in row 16 and row 17 in single-line mode (SL = 1) row data is displayed from row 0 to row 7 and icon row data in row 16
		1	row data: bottom to top; row data is displayed from row 15 to row 0 and icon row data in row 17 and row 16 in single-line mode (SL = 1) row data is displayed from row 15 to row 8 and icon row data in row 17

[1] Default value.

Bit P: The P bit flips the display left to right by mirroring the column data.

Bit Q: The Q bit flips the display top to bottom by mirroring the row data.

Combination of bit P and bit Q: A combination of bit P and bit Q allows the display to be rotated horizontally and vertically by 180 degrees.

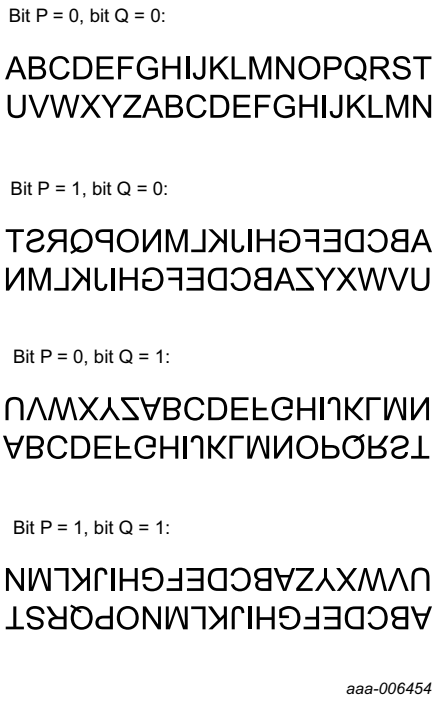


Fig 5. Illustration of the display configuration bits

8.1.2.11 Command: Icon_config

The PCA2117 can drive up to 200 icons. With the Icon_config command the displaying of the icons can be configured.

Table 29. Icon_config - icon display configuration bit description

See Table 38 for the ICON-RAM to ICON mapping.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	000010	fixed value
1	IM		**icon mode setting**
		0[1]	character mode, full display; V_{LCD} programming with the Set_VLCD_A command
		1	icon mode, only icons displayed; V_{LCD} programming with the Set_VLCD_B command

Table 29. Icon_config - icon display configuration bit description *...continued*
See Table 38 for the ICON-RAM to ICON mapping.

Bit	Symbol	Value	Description
0	IB		**icon blink setting**
		0[1]	icon blink disabled
		1	icon blink enabled

[1] Default value.

Bit IM: When bit IM = 0, the chip is in character mode. In the character mode, both, characters and icons are driven (multiplex drive mode 1:18 or 1:9). The V_{LCD} generator, if used, produces the LCD supply voltage (pin VLCDOUT) programmed with the Set_VLCD_A command.

When bit IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (multiplex drive mode 1:2). The V_{LCD} generator, if used, produces the LCD supply voltage (pin VLCDOUT) programmed with the Set_VLCD_B command.

Bit IB: The icon blink control is independent of the cursor/character blink function.

When bit IB = 0, the icon blink is disabled. In this case, the even phase of icon data is used which is stored in the ICON-RAM 00h to 27h.

When bit IB = 1, the icon blink is enabled. In this case, each icon is controlled by 2 bits. The blinking consists of two half phases (corresponding to the cursor on and off phases, called even and odd phases in the following). The Icon states for the even phase are stored in the ICON-RAM 00h to 27h. These bits also define the icon state when icon blinking is not used. The Icon states for the odd phase are stored in the ICON-RAM 28h to 4Fh.

8.1.3 Charge pump and LCD bias control commands

8.1.3.1 Command: Charge_pump_ctrl

The Charge_pump_ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier setting.

Table 30. Charge_pump_ctrl - charge pump control command bit description

Bit	Symbol	Binary value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 3	-	10000	fixed value
2	CPE		**charge pump setting**
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled
1 to 0	CPC[1:0]		**charge pump voltage multiplier setting**
		00[1]	$V_{LCD} = 2 \times V_{DD2}$
		01	$V_{LCD} = 3 \times V_{DD2}$
		10	$V_{LCD} = 4 \times V_{DD2}$
		11	$V_{LCD} = V_{DD2}$ (direct mode)

[1] Default value.

8.1.3.2 Command: Set_VLCD_A and Set_VLCD_B

The Set_VLCD_A and Set_VLCD_B commands allow programming the V_{LCD} value of the character and icon mode, respectively. The generated V_{LCD} is independent of the power supply, allowing battery operation of the PCA2117.

Table 31. Set_VLCD_A and Set_VLCD_B - set V_{LCD} command bit description
See Section 8.4.3.1.

Bit	Symbol	Value	Description
Set_VLCD_A command bit description			
The 5 MSB of VLCDA			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 5	-	101	fixed value
4 to 0	VLCDA[8:4]	00000[1] to 11111	**V_{LCD} value of VLCDA**
The 4 LSB of VLCDA			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 4	-	1001	fixed value
3 to 0	VLCDA[3:0]	0000[1] to 1111	**V_{LCD} value of VLCDA**
Set_VLCD_B command bit description			
The 5 MSB of VLCDB			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 5	-	110	fixed value
4 to 0	VLCDB[8:4]	00000[1] to 11111	**V_{LCD} value of VLCDB**
The 4 LSB of VLCDB			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 4	-	1110	fixed value
3 to 0	VLCDB[3:0]	0000[1] to 1111	**V_{LCD} value of VLCDB**

[1] Default value.

8.1.4 Temperature compensation control commands

8.1.4.1 Command: Temperature_ctrl

The Temperature_ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD} (see Section 8.4.5).

Table 32. Temperature_ctrl - temperature measurement control command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 3	-	00000	fixed value
2	TCE		**temperature compensation setting**
		0[1]	temperature compensation of V_{LCD} disabled
		1	temperature compensation of V_{LCD} enabled
1	TMF		**temperature measurement filter** setting
		0[1]	digital temperature filter disabled[2]
		1	digital temperature filter enabled
0	TME		**temperature measurement setting**
		0[1]	temperature measurement disabled; no temperature readout possible
		1	temperature measurement enabled; temperature readout possible

[1] Default value.

[2] The unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation.

8.1.4.2 Command: TC_slope

The TC_slope command allows setting the temperature coefficients of V_{LCD} corresponding to 4 temperature intervals.

Table 33. TC_slope - V_{LCD} temperature compensation slope command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
TC-slope-A			
7 to 3	-	00001	fixed value
2 to 0	TSA[2:0]	000[1] to 111	**temperature factor A setting**[2]
TC-slope-B			
7 to 3	-	00010	fixed value
2 to 0	TSB[2:0]	000[1] to 111	**temperature factor B setting**[2]
TC-slope-C			
7 to 3	-	00011	fixed value
2 to 0	TSC[2:0]	000[1] to 111	**temperature factor C setting**[2]
TC-slope-D			
7 to 3	-	00100	fixed value
2 to 0	TSD[2:0]	000[1] to 111	**temperature factor D setting**[2]

[1] Default value.

[2] See Table 35 on page 43.

8.2 Start-up and shut-down

8.2.1 Initialization

The first command sent to the device after power-on or a reset by using the $\overline{RST}$ pin must be the Initialize command (see Section 8.1.1.2).

The Initialize command resets the PCA2117 to the following starting conditions:

1. All row and column driver outputs are set to V_{SS1}.
2. Selected drive mode is the 1 × 40 character mode.
3. The address counter is cleared (set logic 0).
4. Temperature measurement is disabled.
5. Temperature filter is disabled.
6. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
7. The V_{LCD} temperature compensation is disabled.
8. The display is disabled.

The reset state is as shown in Table 34.

Table 34. Reset state of PCA2117

Command name	Bits							
	7	6	5	4	3	2	1	0
General control commands								
Clock_out_ctrl	0	0	1	0	0	0	0	0
Read_reg_select	0	0	0	0	0	1	0	0
RAM_ROM_config	0	0	0	0	1	0	0	0
Sel_mem_bank	0	0	0	1	0	0	0	0
Set_mem_addr	1	0	0	0	0	0	0	0
Display control commands								
Entry_mode_set	0	0	1	0	1	0	1	0
Function_set	0	0	1	1	0	0	0	0
Inversion_mode	0	1	0	0	0	0	0	0
Frame_frequency	1	0	0	0	0	1	1	1
Display_control	0	0	1	0	0	0	0	0
Cursor_display_shift	0	0	0	1	0	0	0	0
Screen_config	0	0	0	0	0	0	1	0
Display_config	0	0	0	0	0	1	0	0
Icon_config	0	0	0	0	1	0	0	0
Charge pump and LCD bias control commands								
Charge_pump_ctrl	1	0	0	0	0	0	0	0
Set_VLCD_A	1	0	1	0	0	0	0	0
	1	0	0	1	0	0	0	0
Set_VLCD_B	1	1	0	0	0	0	0	0
	1	1	1	0	0	0	0	0
Temperature compensation control commands								
Temperature_ctrl	0	0	0	0	0	0	0	0
TC_slope	0	0	0	0	1	0	0	0
	0	0	0	1	0	0	0	0
	0	0	0	1	1	0	0	0
	0	0	1	0	0	0	0	0

Remarks:

1. Do not transfer data for at least 1 ms after a power-on.
2. After power-on and before enabling the display, the DDRAM content must be brought to a defined status
   - by sending the Clear_display command
   - or by writing meaningful display content by loading a character code

   otherwise unwanted display artifacts can appear on the display.

8.2.2 Reset pin function

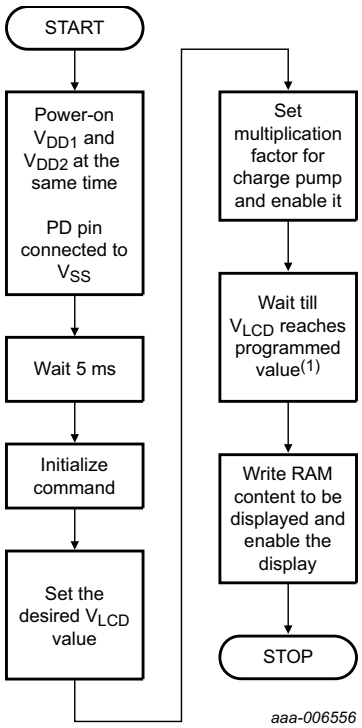
The reset pin ($\overline{RST}$) of the PCA2117 resets all the registers to their default state. The reset state is given in Table 34. The RAM contents remain unchanged. After the reset signal is released, the Initialize command must be sent to complete the initialization of the chip.

8.2.3 Power-down pin function

When connected to V_{DD1}, the internal circuits are switched off, leaving only 2 μA (typical) as an overall current consumption. When connected to V_{SS1}, the PCA2117 runs or starts up to normal mode again. For the start-up and power-down sequences, see Section 8.2.4 and Section 8.2.5.

8.2.4 Recommended start-up sequences

This section describes how to proceed with the initialization of the chip in different application modes.



(1) The QPR flag (see Table 12) indicates if the programmed LCD voltage value was reached. The latency time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of 50 ms to 60 ms is expected.

Fig 6. Recommended start-up sequence when using the internal charge pump and the internal clock signal

When using the internal V_{LCD} generation, the display must not be enabled before the generation of V_{LCD} with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.

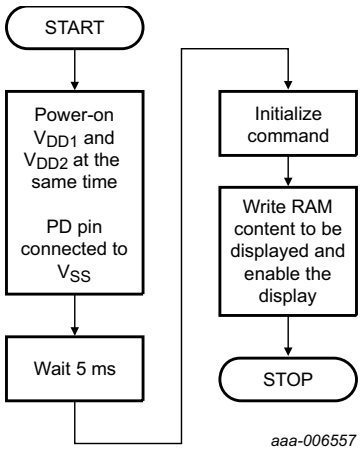
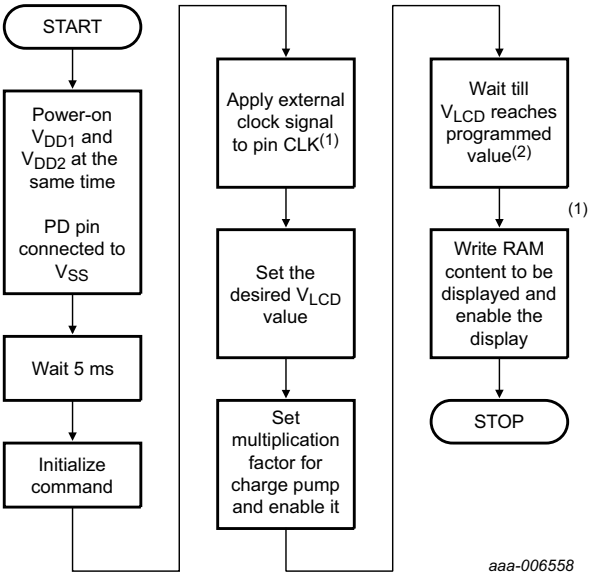


Fig 7. Recommended start-up sequence when using an externally supplied V_{LCD} and the internal clock signal



(1) Alternatively, the external clock signal can be applied after the generation of the V_{LCD} voltage.

(2) The QPR flag (see Table 12) indicates if the programmed LCD voltage value was reached. The latency time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of 50 ms to 60 ms is expected.

Fig 8. Recommended start-up sequence when using the internal charge pump and an external clock signal

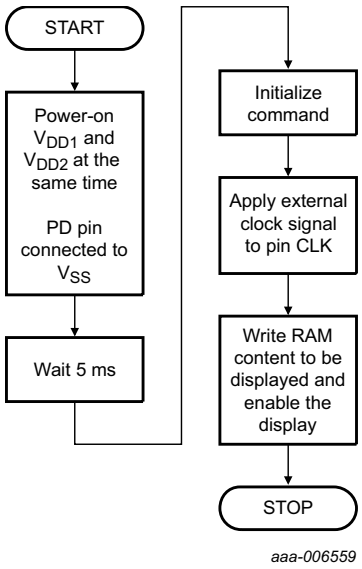
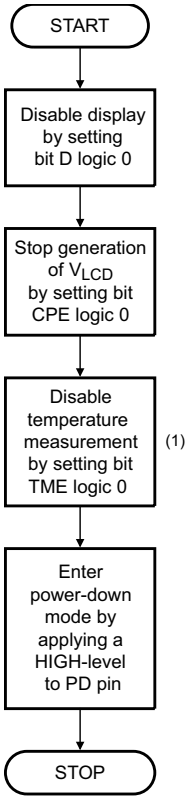


Fig 9. Recommended start-up sequence when using an externally supplied V_{LCD} and an external clock signal

8.2.5 Recommended power-down sequences

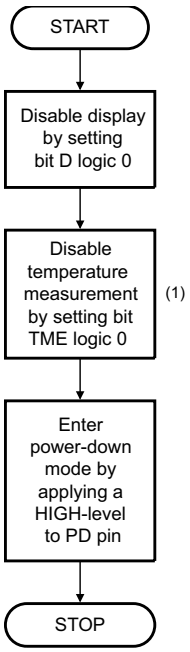
With the following sequences, the PCA2117 can be set to a state of minimum power consumption, called power-down mode.



(1) If previously enabled.

Remark: When bits D (Table 25 on page 20), CPE (Table 30 on page 24), and TME (Table 32 on page 26) are logic 0, the internal clock signal is switched off.

Fig 10. Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal



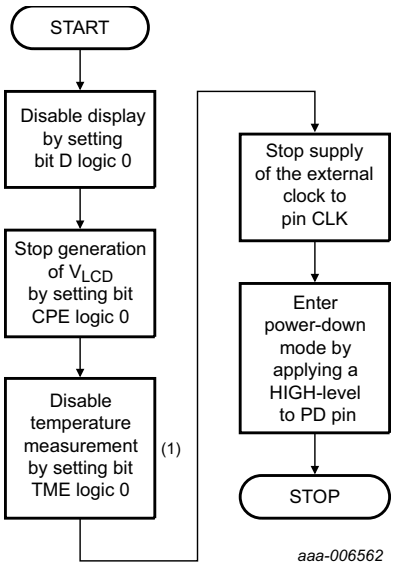
(1) If previously enabled.

Remark: When bits D (Table 25 on page 20), CPE (Table 30 on page 24), and TME (Table 32 on page 26) are logic 0, the internal clock signal is switched off.

Fig 11. Recommended power-down sequence when using an externally supplied V_{LCD} and the internal clock signal

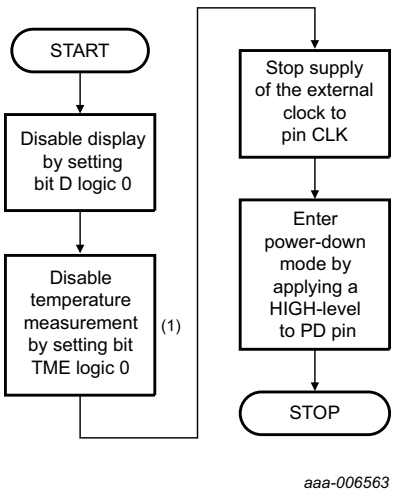
The chip can be put into power-down mode by applying a HIGH-level to pin PD. In power-down mode, all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAM and the chip state are not preserved. Instruction execution during power-down is not possible.



(1) If previously enabled.

Fig 12. Recommended power-down sequence when using the internal charge pump and an external clock signal



(1) If previously enabled.

Fig 13. Recommended power-down sequence when using an externally supplied V_{LCD} and an external clock signal

Remarks:

1. It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (refer to Section 10 on page 76). Otherwise it may cause unwanted display artifacts. Uncontrolled removal of supply voltages does not damage the PCA2117.

2. Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD1} and V_{DD2}) is off, or the other way round. This may cause unwanted display artifacts. To avoid such artifacts, external V_{LCD}, V_{DD1}, and V_{DD2} must be applied or removed together.
3. A clock signal must always be supplied to the device when the device is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. Disable the display first and then remove the clock signal afterwards.

8.3 Possible display configurations

The PCA2117 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of character displays (see Figure 14 and Figure 15).

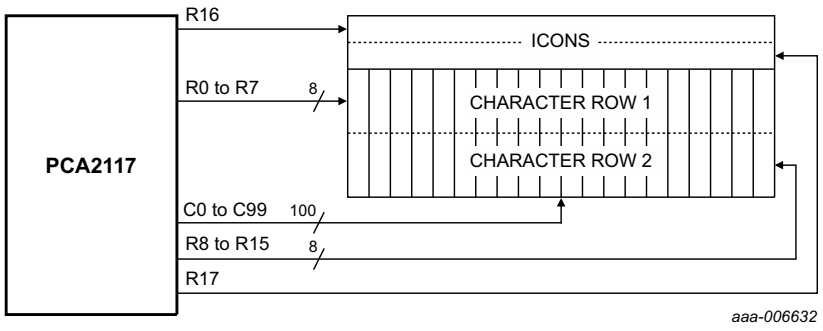


Fig 14. Connecting PCA2117 with a 2 × 20 character LCD

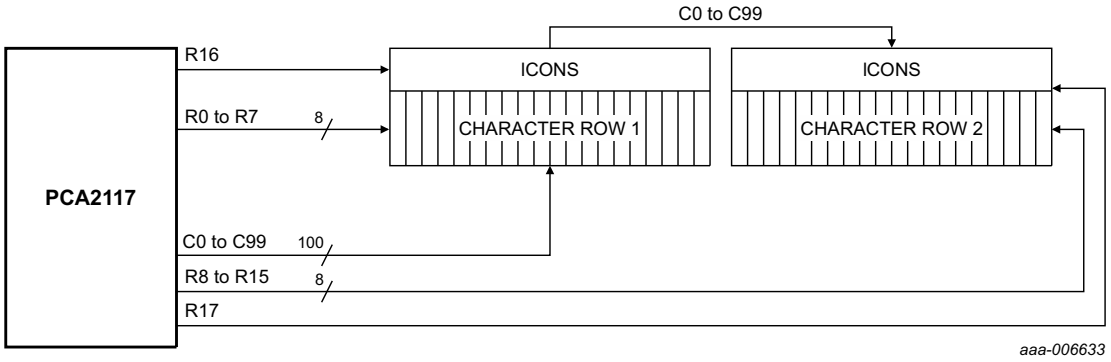


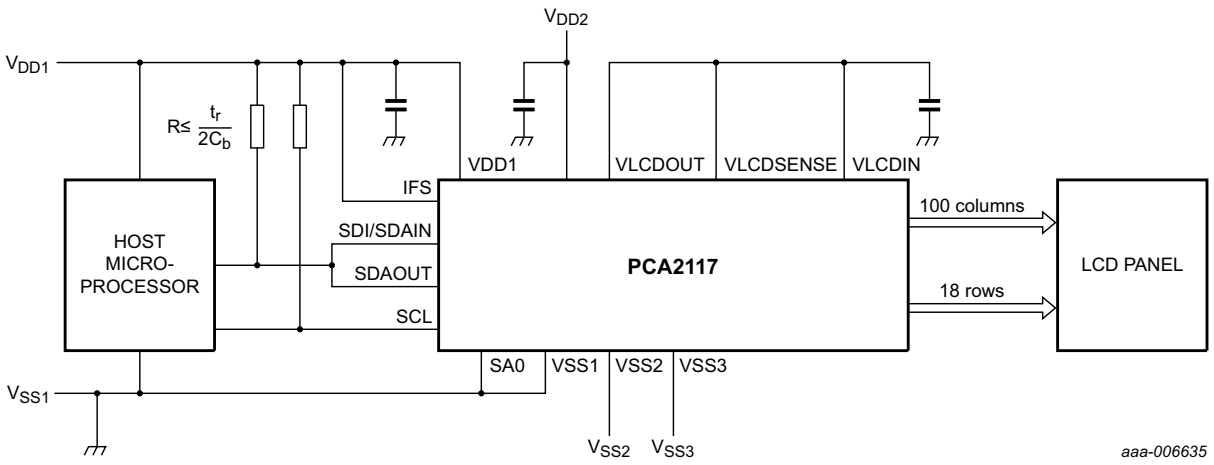
Fig 15. Connecting PCA2117 with a 1 × 40 character LCD

The host microcontroller maintains the communication channel with the PCA2117. The only other connections required to complete the system are the power supplies (VDD1, VDD2, and VSS1 to VSS3), the V_{LCD} pins (VLCDOUT, VLCDSENSE, VLCDIN), the external capacitors, and the LCD panel selected for the application. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally.

External capacitors of 100 nF minimum are required on each of the pins VDD1 and VDD2. If they are connected to the same power supply (not recommended if V_{LCD} is generated internally), a capacitor of 300 nF minimum is required.

VSS1 to VSS3 have to be connected to the same ground supply.

The V_{LCD} pins (VLCDOUT, VLCDSENSE, VLCDIN) can be connected, whether V_{LCD} is generated internally or supplied from external. An external capacitor of 300 nF minimum is recommended for V_{LCD}. For high display loads, 1 μF is suggested.

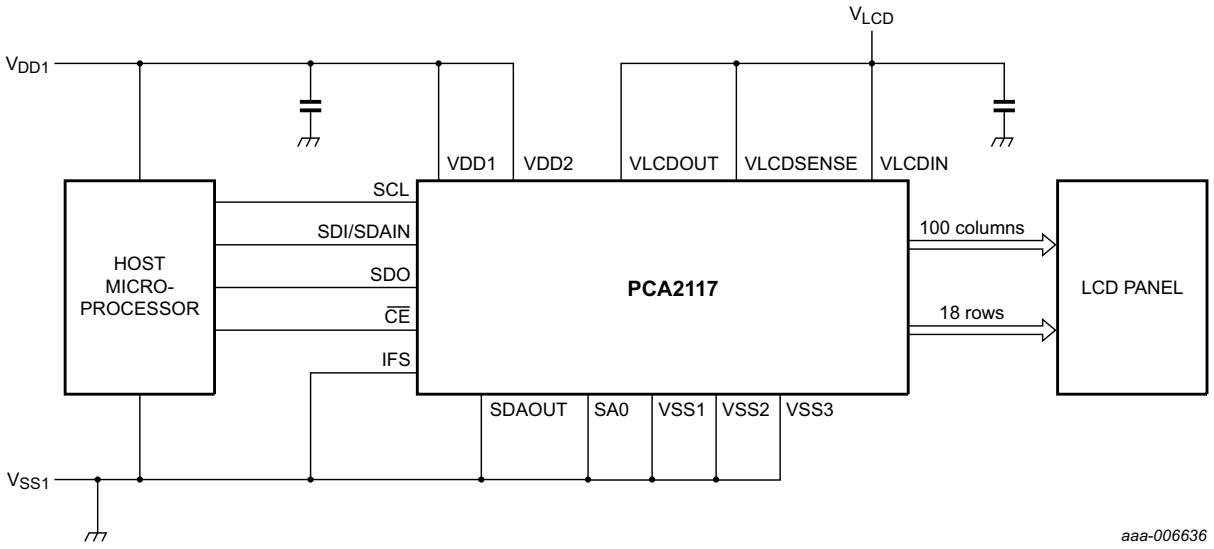


V_{DD1} and V_{DD2} from 2.5 V to 5.5 V. Values for t_r and C_b, see Table 52.

V_{DD1} and V_{DD2} can be connected to the same power supply.

V_{SS1} to V_{SS3} can be connected to the same ground supply.

Fig 16. Typical system configuration if using the internal V_{LCD} generation and I²C-bus



V_{DD1} and V_{DD2} from 2.5 V to 5.5 V.

Fig 17. Typical system configuration if using the external V_{LCD} and SPI-bus

8.4 LCD voltage

8.4.1 V_{LCD} pins

The PCA2117 has 3 V_{LCD} pins:

VLCDIN — V_{LCD} supply input

VLCDOUT — V_{LCD} voltage output

VLCDSENSE — V_{LCD} regulation circuitry input

The V_{LCD} voltage can be generated on-chip or externally supplied.

8.4.2 External V_{LCD} supply

When the external V_{LCD} supply is selected, the V_{LCD} voltage must be supplied to the pin VLCDIN. The pins VLCDOUT and VLCDSENSE can be left unconnected or alternatively connected to VLCDIN. The V_{LCD} voltage is available at the row and column drives of the device through the chosen bias system.

The internal charge pump must not be enabled, otherwise high internal currents may flow as well as high currents via pin VDD2 and pin VLCDOUT. No internal temperature compensation occurs on the externally supplied V_{LCD} even if bit TCE is set logic 1 (see Section 8.1.4.1). Also programming VLCDA[8:0] and VLCDB[8:0] has no effect on the externally supplied V_{LCD}.

8.4.3 Internal V_{LCD} generation

When the internal V_{LCD} generation is selected, the V_{LCD} voltage is available on pin VLCDOUT. The pins VLCDIN and VLCDSENSE must be connected to the pin VLCDOUT.

The Charge_pump_ctrl command (see Table 30 on page 24) controls the charge pump. It can be enabled with the CPE bit. The multiplier setting can be configured with the CPC[1:0] bits. The charge pump can generate a V_{LCD} up to $4 \times V_{DD2}$.

8.4.3.1 V_{LCD} programming

V_{LCD} can be programmed by two bit-fields: VLCDA[8:0] and VLCDB[8:0]. VLCDA[8:0] is programmed with the voltage for the character mode and VLCDB[8:0] with the voltage for the icon mode.

The final value of V_{LCD} is a combination of the programmed VLCDA[8:0] respectively VLCDB[8:0] value and in addition the output of the temperature compensation block. The system is exemplified in Figure 18.

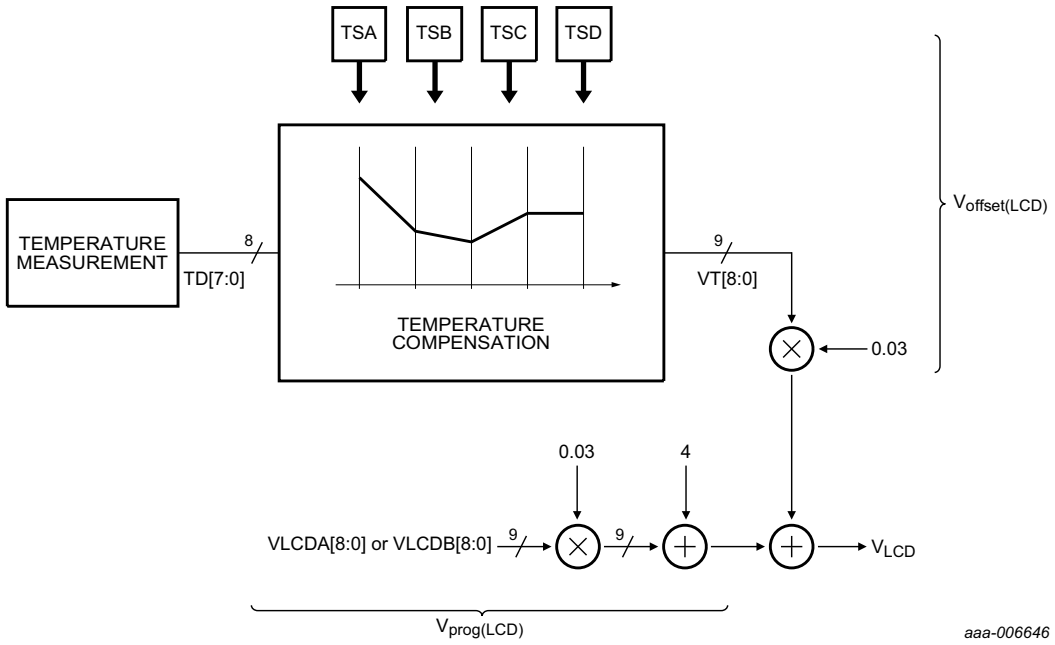


Fig 18. V_{LCD} generation including temperature compensation

Equation 1 to Equation 3 exemplify the V_{LCD} generation with temperature compensation.

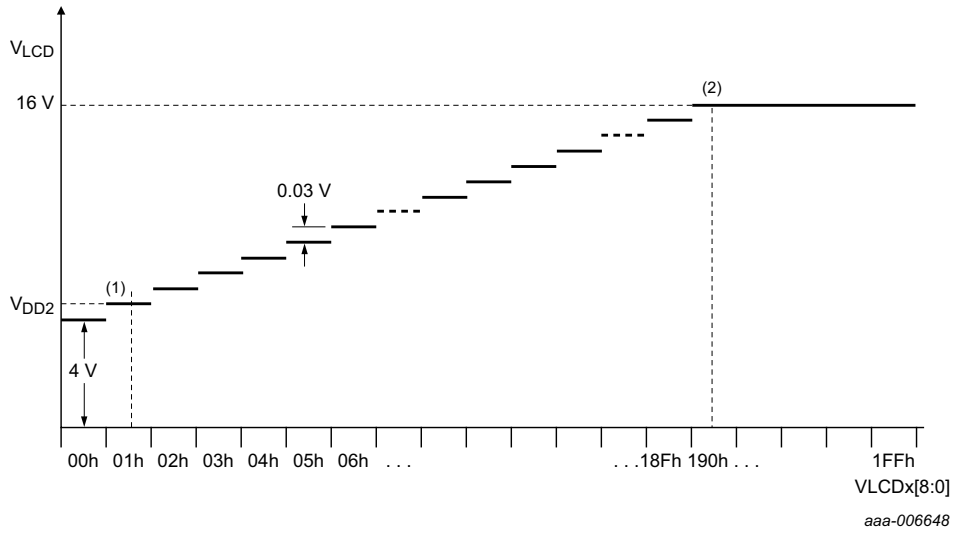
$$V_{prog(LCD)} = \text{VLCDx} \times 0.03\ \text{V} + 4\ \text{V} \quad (1)$$

$$V_{offset(LCD)} = \text{VT} \times 0.03\ \text{V} \quad (2)$$

$$V_{LCD} = V_{prog(LCD)} + V_{offset(LCD)} = \text{VLCDx} \times 0.03\ \text{V} + 4\ \text{V} + \text{VT} \times 0.03\ \text{V} \quad (3)$$

1. VLCDx is the decimal value of the programmed VLCD factor (VLCDA[8:0] or VLCDB[8:0]).
2. VT is the binary value of the calculated temperature compensating factor (VT[8:0]) of the temperature compensation block (see Table 36). The temperature compensation block provides the value which is a two's complement with the value of 0h at 20 °C.

Figure 19 shows how the V_{LCD} changes with the programmed value of VLCDx[8:0].



(1) VLCDx[8:0] must be set such that $V_{LCD} > V_{DD2}$.

(2) Automatic limitation for $V_{LCD} > 16$ V.

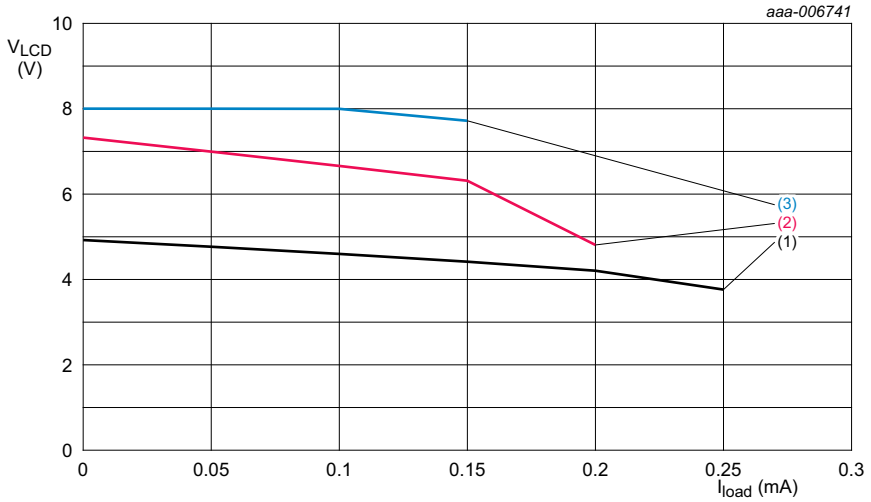
Fig 19. V_{LCD} programming of PCA2117 (assuming VT[8:0] = 0h)

Remarks:

1. VLCDx[8:0] has to be set to such a value that the resultant V_{LCD}, including the temperature compensation, is higher than V_{DD2}.
2. The programmable range of VLCDx[8:0] is from 0h to 1FFh. It would allow achieving a V_{LCD} of higher voltages but the PCA2117 has a built-in automatic limitation set to 16 V.

8.4.4 V_{LCD} drive capability

Figure 20 to Figure 22 illustrate the drive capability of the internal charge pump for various conditions. V_{LCD} is internally limited to 16 V.



Conditions: V_{DD2} = 2.5 V; V_{LCD} = 8 V; T_{amb} = 25 °C; $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

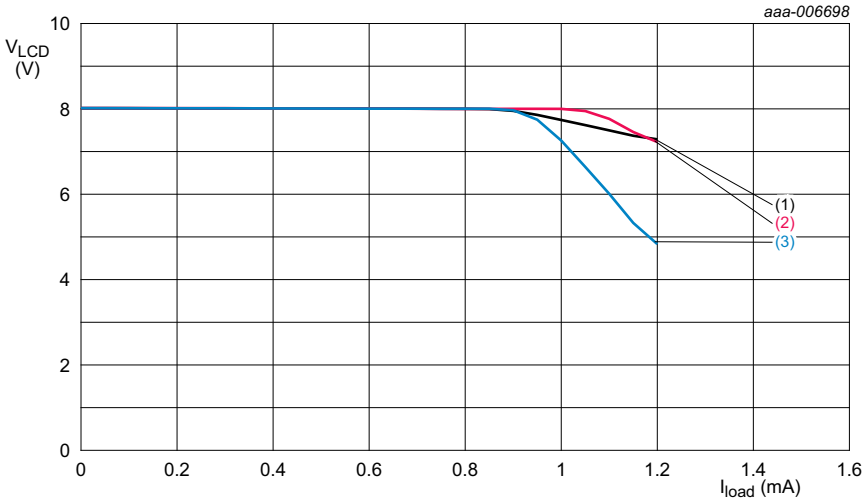
(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

I_{load} is the overall current sink of the column and row outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 20. V_{LCD} with respect to I_{load} at V_{DD2} = 2.5 V



Conditions: V_{DD2} = 5 V; V_{LCD} = 8 V; T_{amb} = 25 °C; $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

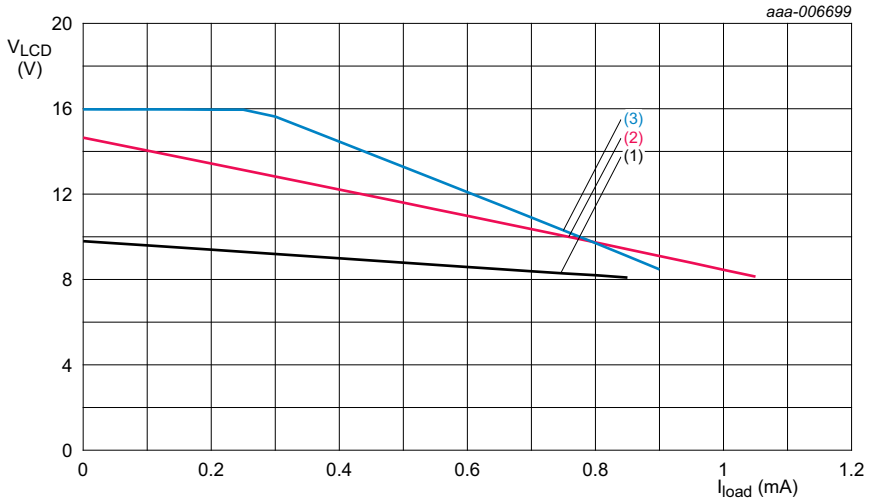
(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

I_{load} is the overall current sink of the column and row outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 21. V_{LCD} with respect to I_{load} at V_{DD2} = 5 V



Conditions: V_{DD2} = 5 V; V_{LCD} = 16 V; T_{amb} = 25 °C; $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

I_{load} is the overall current sink of the column and row outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 22. V_{LCD} with respect to I_{load} at V_{DD2} = 5 V

8.4.5 Temperature measurement and temperature compensation of V_{LCD}

8.4.5.1 Temperature readout

The PCA2117 has a built-in temperature sensor which provides an 8-bit digital value (TD[7:0]) of the ambient temperature. This value can be read by command (see Section 8.1.1.6 on page 11). The actual temperature is determined from TD[7:0] using Equation 4.

$$T(°C) = 0.6275 \times TD - 40 \quad (4)$$

TD[7:0] = FFh means that no temperature readout is available or was performed. FFh is the default value after initialization. The measurement needs about 8 ms to complete. It is repeated periodically every second as long as bit TME is set logic 1 (see Table 32 on page 26).

Due to the nature of a temperature sensor, oscillations may occur. To avoid it, a filter has been implemented in PCA2117. A control bit, TMF, is implemented to enable or disable the digital temperature filter (see Table 32 on page 26). The system is exemplified in Figure 23.

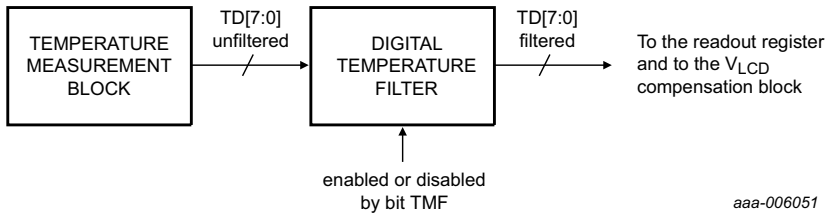
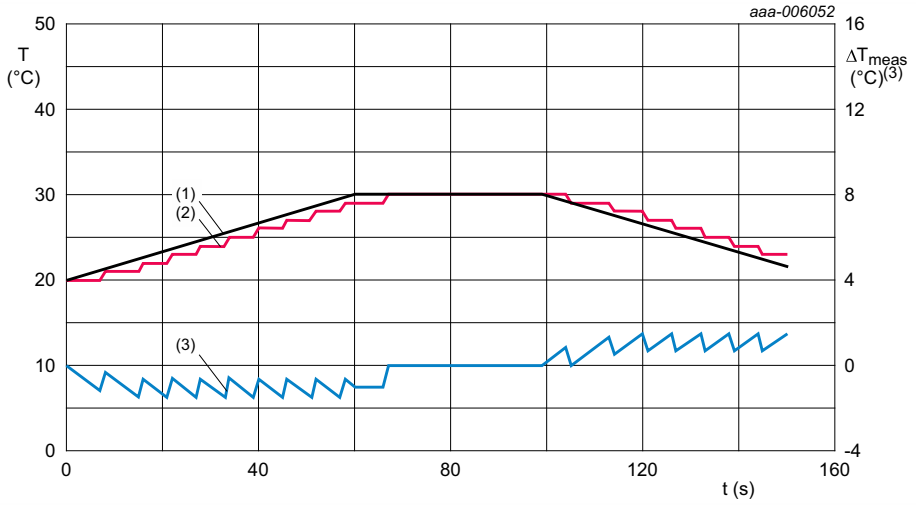


Fig 23. Temperature measurement block with digital temperature filter

The digital temperature filter introduces a certain delay in the measurement of the temperature. This behavior is illustrated in Figure 24.



(1) Environment temperature, T1 (°C).

(2) Measured temperature, T2 (°C).

(3) Measurement temperature variation, ΔT_{meas} = T2 − T1.

Fig 24. Temperature measurement delay

8.4.5.2 Temperature adjustment of the V_{LCD}

Due to the temperature dependency of the liquid crystal viscosity, the LCD supply voltage may have to be adjusted at different temperatures to maintain optimal contrast. The temperature characteristics of the liquid are provided by the LCD manufacturer. The slope has to be set to compensate for the liquid behavior. Internal temperature compensation can be enabled via bit TCE (see Table 32 on page 26).

The ambient temperature range is split up into 4 regions (see Figure 25) and to each a different temperature coefficient can be applied.

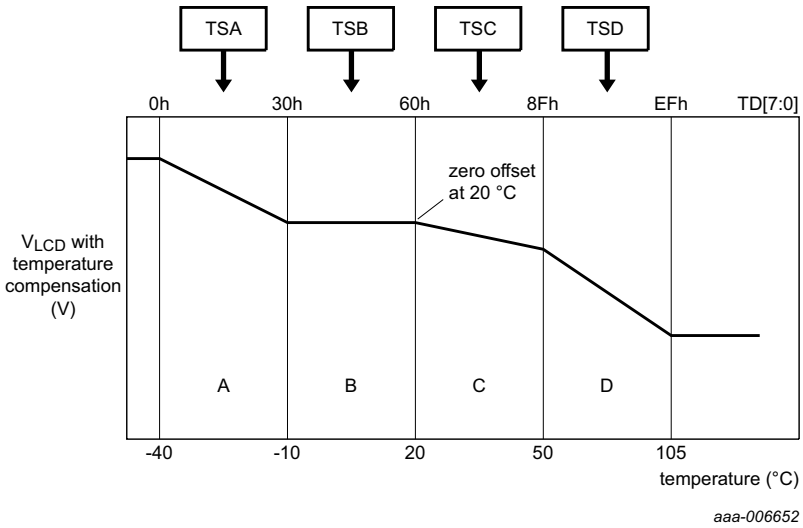


Fig 25. Example of segmented temperature coefficients

The temperature coefficients can be selected from a choice of eight different slopes. Each one of theses coefficients is independently selected via the TC_slope command (see Section 8.1.4.2 on page 26).

Table 35. Temperature coefficients

TSA[2:0] to TSD[2:0] value	Slope factor (mV/°C)	Temperature factor TSA to TSD[1]
000[2]	0	0.000
001	–6	–0.125
010	–12	–0.250
011	–24	–0.500
100	–60	–1.250
101	+6	+0.125
110	+12	+0.250
111	+24	+0.500

[1] The relationship between the temperature coefficients TSA to TSD and the slope factor is derived from Equation 5. where LSB of VLCDx[8:0] ≅ 30 mV.

[2] Default value.

$$TSn = \frac{0.6275(°C)}{30\ (\mathrm{mV})} \times \text{slope factor}\ (\mathrm{mV}/°C) \quad (5)$$

The value of the temperature compensated factor VT[8:0] is calculated according to Table 36.

Table 36. Calculation of the temperature compensating factor VT

Temperature range (°C)	Decimal value of TD[7:0]	Equations of factor VT
$T \leq -40\ °C$	0	$VT = -48 \times TSB - 48 \times TSA$
$-40°C < T \leq -10\ °C$	0 to 48	$VT = -48 \times TSB - (48 - \text{TD[7:0]}) \times TSA$
$-10\ °C < T \leq 20\ °C$	49 to 96	$VT = -(96 - \text{TD[7:0]}) \times TSB$
$20\ °C < T \leq 50\ °C$	97 to 143	$VT = (\text{TD[7:0]} - 96) \times TSC$
$50\ °C < T < 105\ °C$	144 to 230	$VT = 47 \times TSC + (\text{TD[7:0]} - 143) \times TSD$
$105\ °C \leq T$ [1]	231	$VT = 47 \times TSC + 88 \times TSD$

[1] No temperature compensation is possible above 105 °C. Above this value, the system maintains the compensation value from 105 °C.

8.4.5.3 Example calculation of $V_{offset(LCD)}$

Assumed that T_{amb} = −8 °C

1. Choose a temperature factor from Table 35, for example TSB[2:0] = 001, which gives a slope factor of −0.125.
2. Calculate the decimal value of TD[7:0] with Equation 4:

$$TD = \frac{-8 + 40}{0.6275} \approx 51 .$$

3. Calculate the temperature compensating factor VT with the appropriate equation from Table 36:

$$VT = -(96 - 51) \times -0.125 = 5.625 .$$

4. Calculate $V_{offset(LCD)}$ with Equation 2:

$$V_{offset(LCD)} = 5.625 \times 0.03\ \text{V} = 0.169\ \text{V} .$$

8.4.6 LCD bias voltage generator

The intermediate bias voltages for the LCD are generated on-chip. It removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels.

The intermediate bias levels for the different multiplex rates are shown in Table 37. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 37. Bias levels as a function of multiplex rate

Multiplex rate	LCD bias configuration	Bias voltages					
		V_1	V_2	V_3	V_4	V_5	V_6
1:18	1/4	V_{LCD}	$\frac{3}{4}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{4}V_{LCD}$	V_{SS}
1:9	1/4	V_{LCD}	$\frac{3}{4}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{4}V_{LCD}$	V_{SS}
1:2	1/3	V_{LCD}	$\frac{2}{3}V_{LCD}$	$\frac{2}{3}V_{LCD}$	$\frac{1}{3}V_{LCD}$	$\frac{1}{3}V_{LCD}$	V_{SS}

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 6 and the RMS off-state voltage ($V_{off(RMS)}$) with Equation 7:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (6)$$

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (7)$$

where the values of a are

a = 2 for $\frac{1}{3}$ bias

a = 3 for $\frac{1}{4}$ bias

and the values for n are

n = 2 for 1:2 multiplex rate

n = 9 for 1:9 multiplex rate

n = 18 for 1:18 multiplex rate.

Discrimination (D) is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 8. Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a + 1)^2 + (n - 1)}{(a - 1)^2 + (n - 1)}} \quad (8)$$

Remark:

- Row and column outputs comprise a series resistance R_O (see Table 50).
- V_{LCD} is sometimes referred as the LCD operating voltage.

8.4.6.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determines the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 26. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (9)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (10)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see Equation 6), n (see Equation 8), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

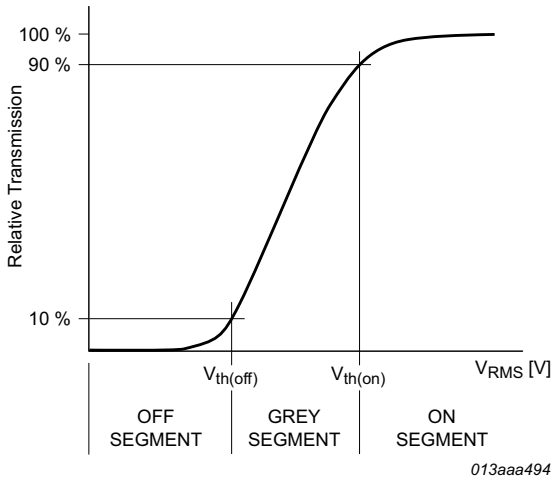
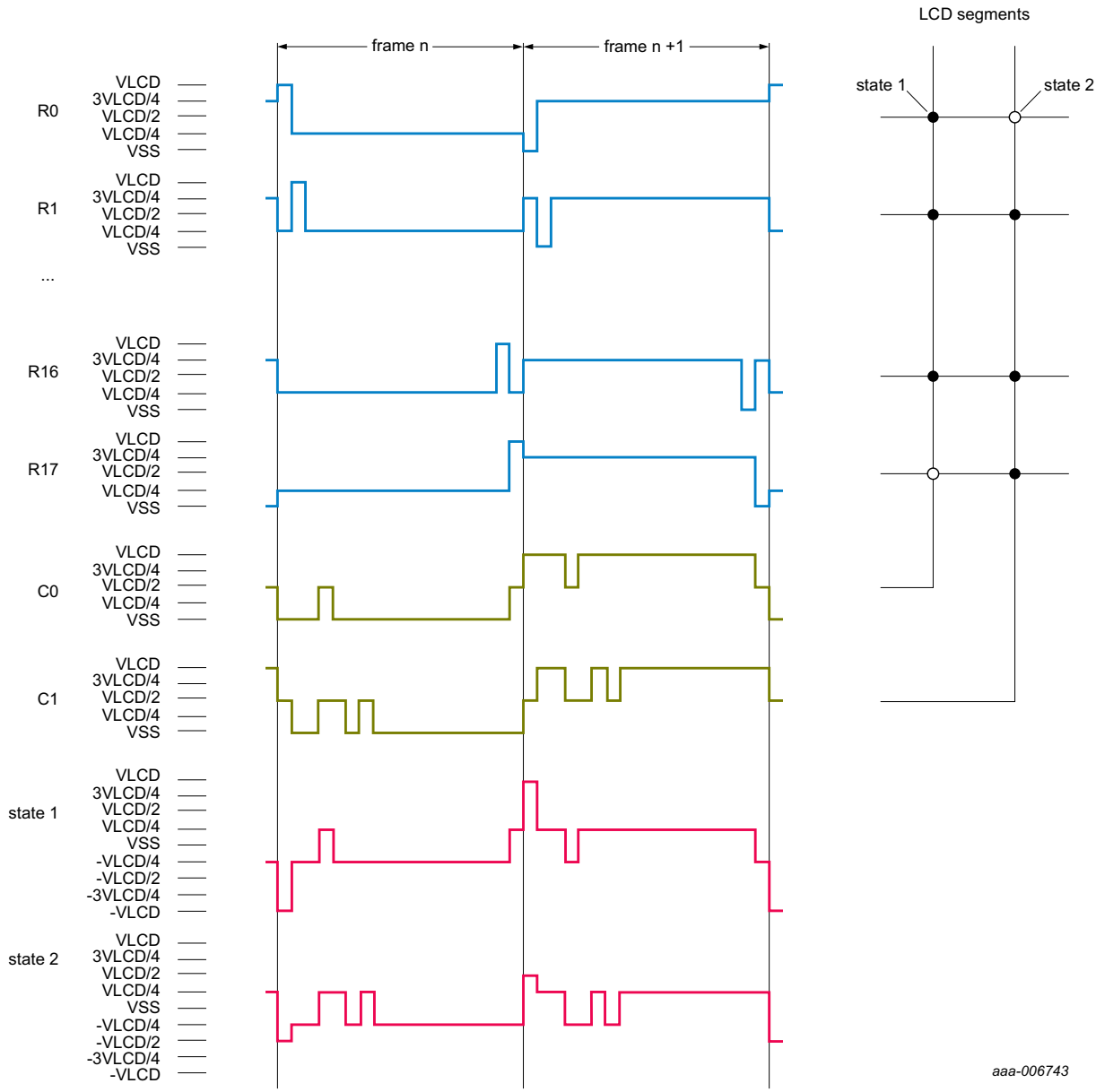


Fig 26. Electro-optical characteristic: relative transmission curve of the liquid

8.4.7 LCD drive mode waveforms

The PCA2117 contains 18 row and 100 column drivers, which drive the appropriate LCD bias voltages in sequence to the display and in accordance with the data to be displayed. R16 and R17 drive the icon rows. Unused outputs should be left open.

The bias voltages and the timing are automatically selected when the number of lines in the display is selected. Figure 27 to Figure 29 show typical waveforms.



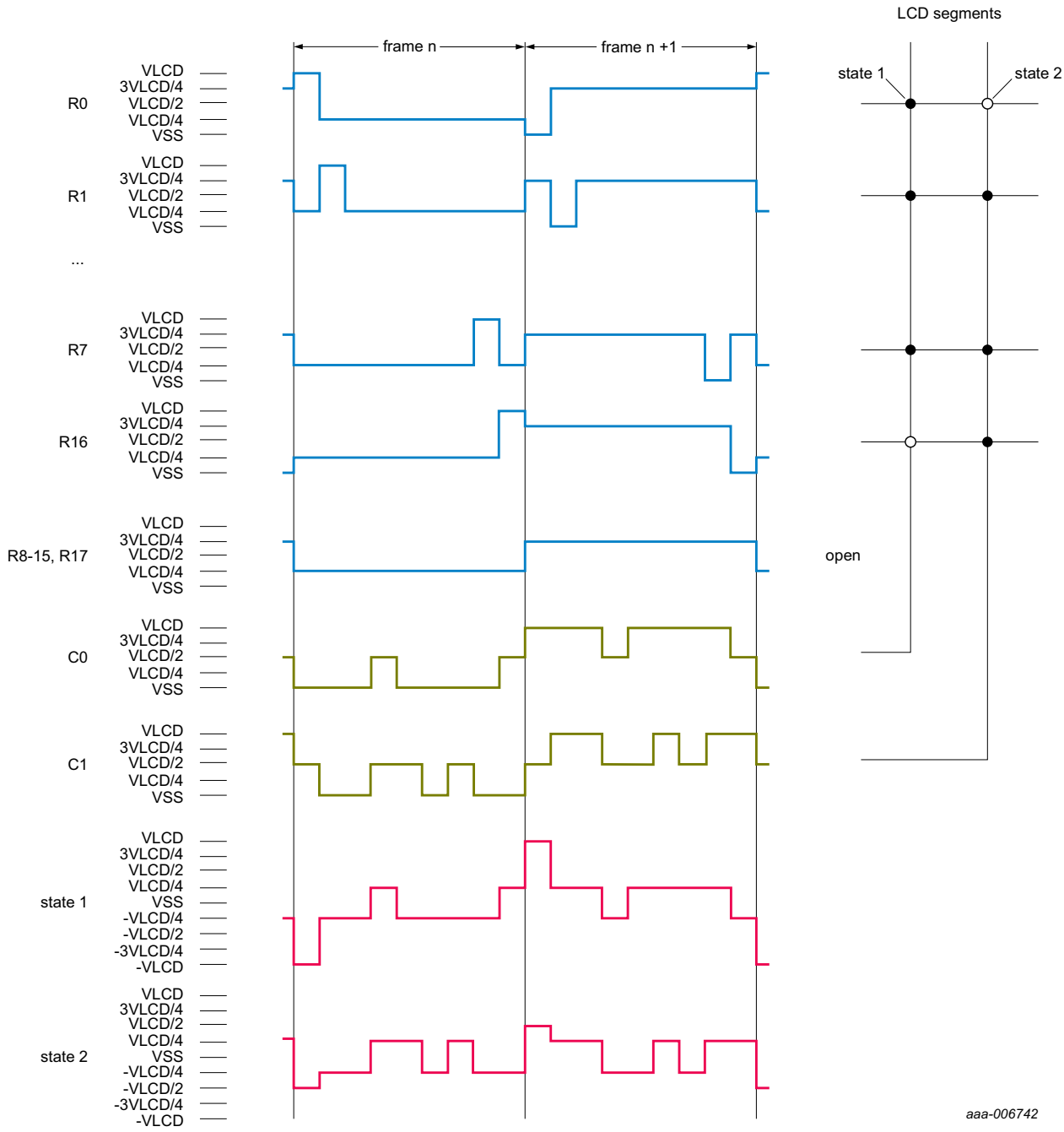
State(n) marks intersection(row(x),col(n)) of LCD element(x,n).

$V_{state(n)}(t) = V_{C(n)}(t) - V_{R(x)}(t)$.

$V_{state1}(t) = V_{C0}(t) - V_{R0}(t)$.

$V_{state2}(t) = V_{C1}(t) - V_{R0}(t)$.

Fig 27. Waveforms for the 1:18 multiplex drive mode. 5 bias levels, character mode, frame inversion mode



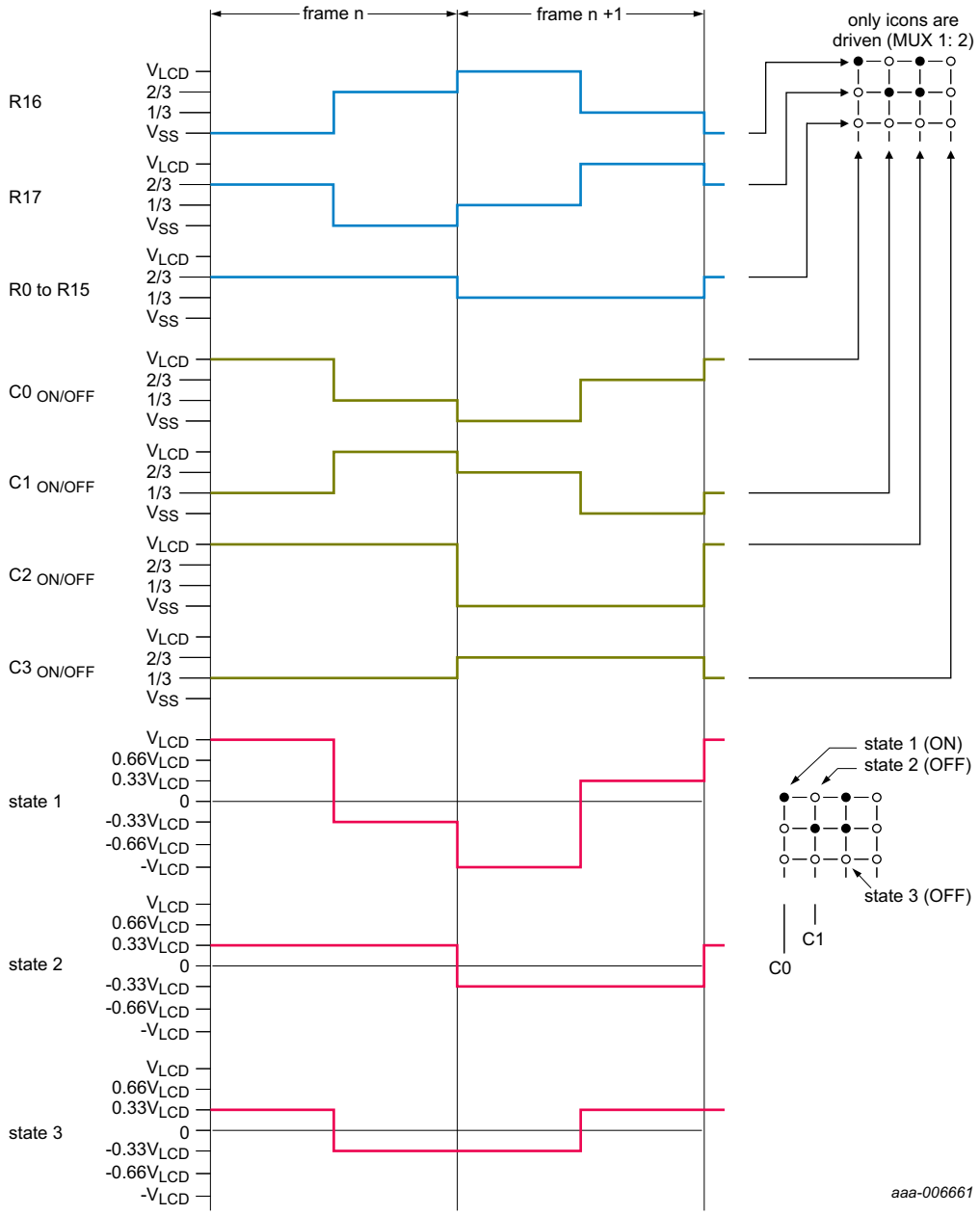
State(n) marks intersection(row(x),col(n)) of LCD element(x,n).

$V_{state(n)}(t) = V_{C(n)}(t) - V_{R(x)}(t)$.

$V_{state1}(t) = V_{C0}(t) - V_{R0}(t)$.

$V_{state2}(t) = V_{C1}(t) - V_{R0}(t)$.

Fig 28. Waveforms for the 1:9 multiplex drive mode, 5 bias levels, character mode, R8 to R15 and R17 open, frame inversion mode



State(n) marks intersection(row(x),col(n)) of LCD element(x,n).

$V_{state(n)}(t) = V_{C(n)}(t) - V_{R(x)}(t)$.

$V_{state1}(t) = V_{C0}(t) - V_{R16}(t)$.

$V_{state2}(t) = V_{C1}(t) - V_{R16}(t)$.

$V_{state3}(t) = V_{C2}(t) - V_{R1\ to\ 15}(t)$.

Fig 29. Waveforms for the 1:2 multiplex drive mode, 4 bias levels, icon mode, frame inversion mode

8.5 Display data RAM and ROM

The PCA2117 has a CGROM containing the character set, a CGRAM for user-defined characters, an ICON-RAM for user-defined icons and a DDRAM which contains the display data from the CGROM and CGRAM. There is a one-to-one correspondence between the bits in the DDRAM and the LCD elements. The whole dataflow is exemplified in Figure 30.

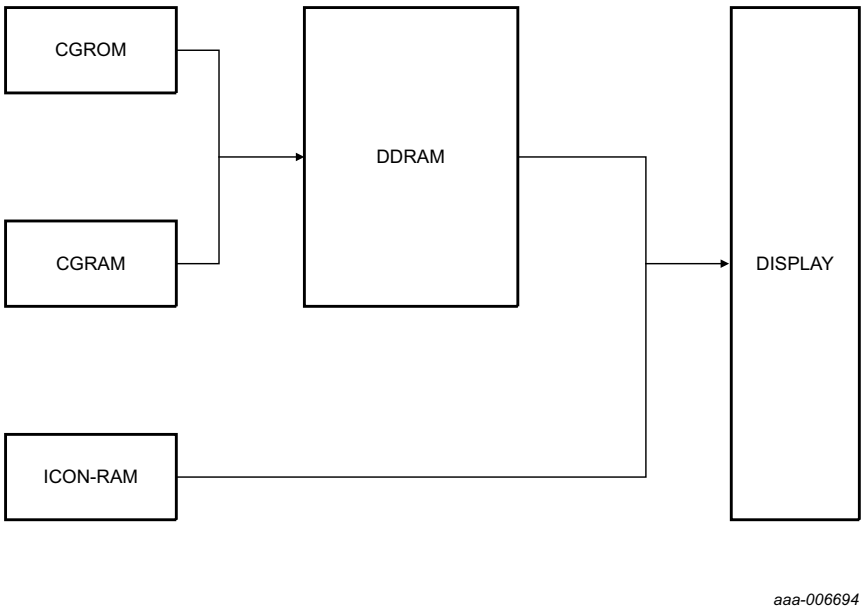


Fig 30. Dataflow from CGROM, CGRAM and ICON-RAM to the display

8.5.1 RAM/ROM access

The RAM and ROM access of the PCA2117 is exemplified in Figure 31

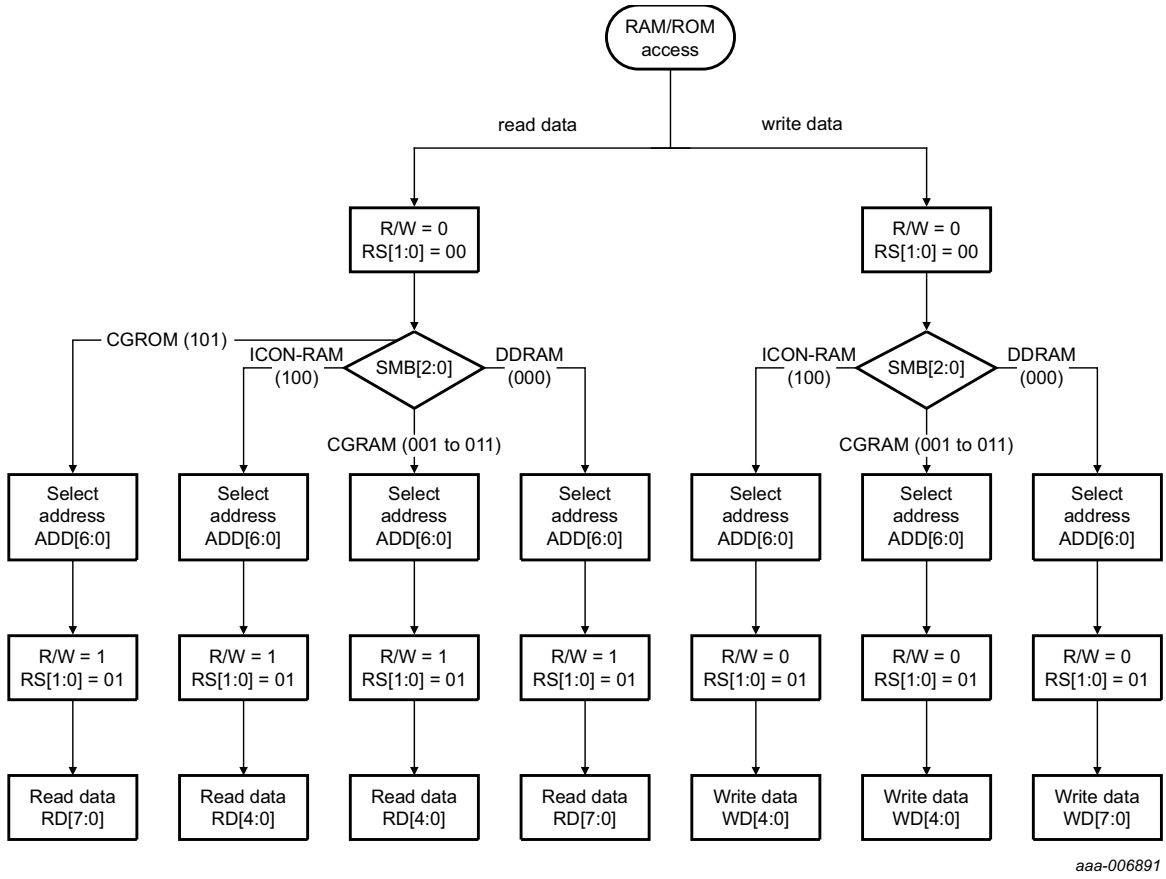


Fig 31. RAM/ROM access flowchart

8.5.2 Checksum

In order to detect transmission failures for RAM content transfers, the PCA2117 has a checksum calculator providing an XOR or CRC-8 checksum. The checksum calculator can be configured with bit XC of the Read_reg_select command (see Section 8.1.1.6). The checksum result can be read out with the Read_status_reg command (see Section 8.1.1.7).

The checksum results are:

- when XC = 0 (XOR checksum)
  - The checksum is the result of the XOR operation on the values loaded with the Write_data command and the previous register content.
  - The checksum result is reset when the bits of the command select RS[1:0] or R/$\overline{W}$ are changed.
- when XC = 1 (CRC-8 checksum)

- The checksum is the result of the CRC-8 operation on the values loaded with the Write_data command and the previous register content. The polynomial used is $x^8 + x^5 + x^4 + 1$.
- The checksum result is reset when the bits of the command select RS[1:0] or R/$\overline{W}$ are changed.

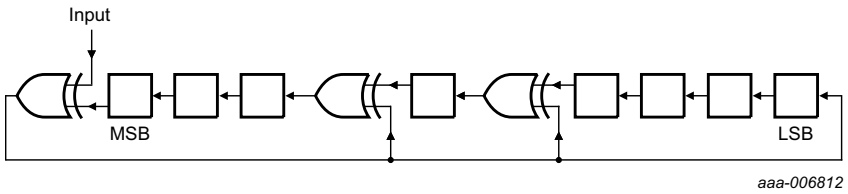


Fig 32. Logic diagram of the CRC8 generator

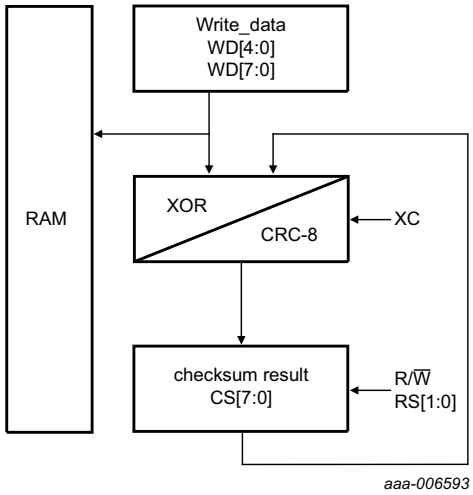


Fig 33. Checksum generation

8.5.3 CGROM

The Character Generator ROM (CGROM) contains 240 character patterns in a 5 × 8 dot format from 8-bit character codes. The PCA2117 has the character set shown in Figure 34. It can be provided with other character sets on request.

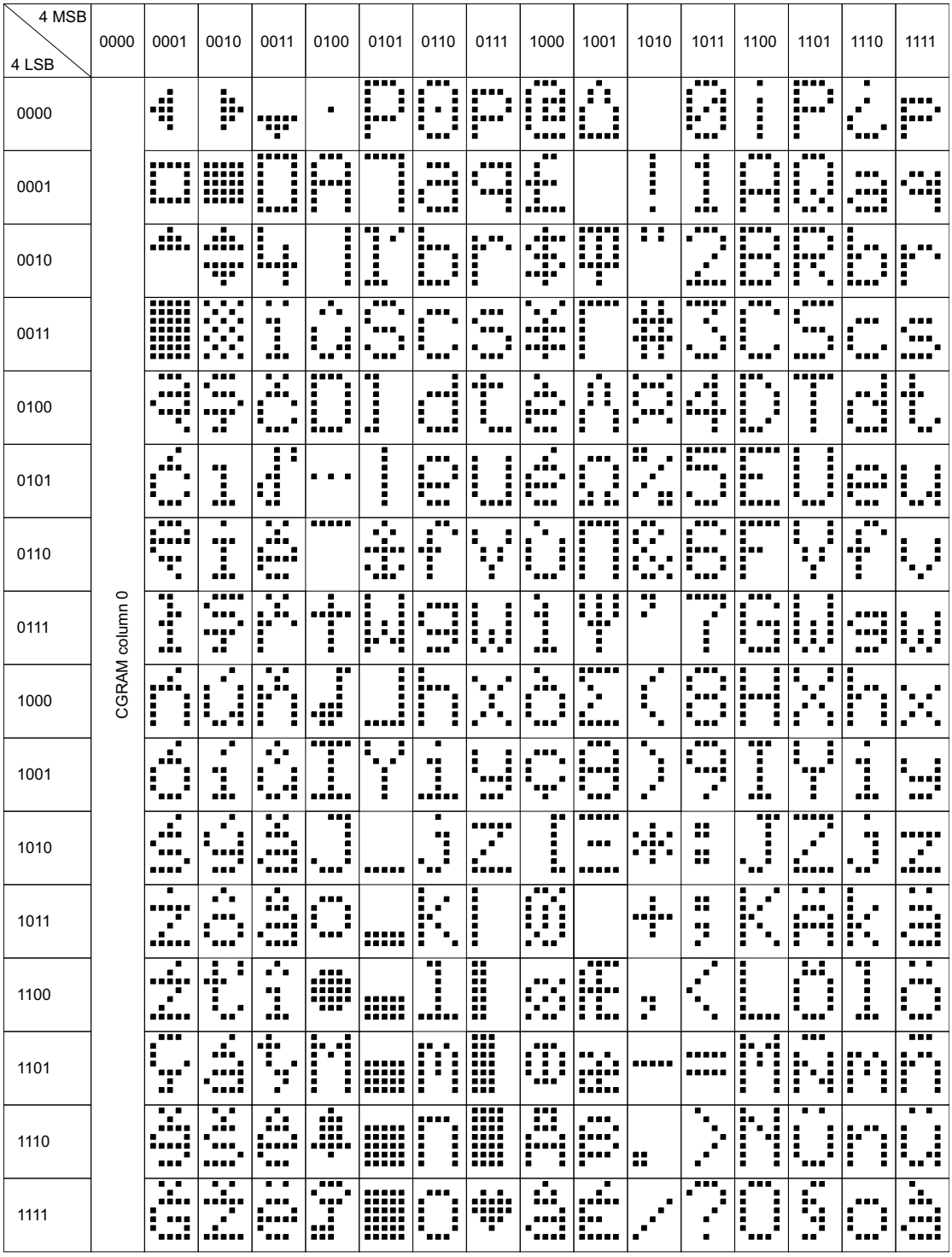


Fig 34. Character set ‘R’ in CGROM

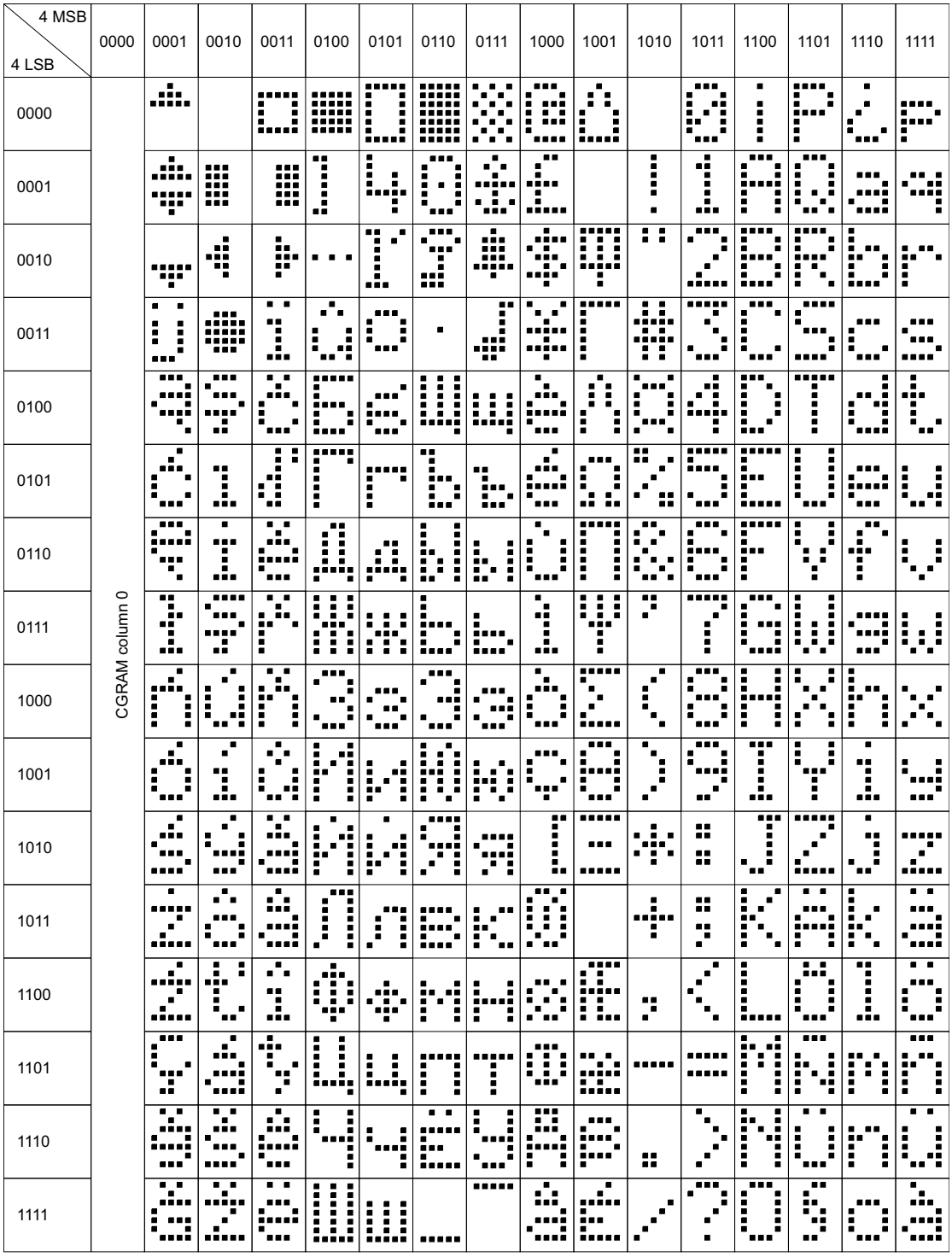


Fig 35. Character set ‘S’ in CGROM

8.5.3.1 CGROM addressing

To display a character from the CGROM, it has to be written to the DDRAM with WD[7:0} of the Write_data command. The addressing sequence is “4 MSB 4 LSB” (see Figure 31).

Addressing examples:

- 1101 0000 points to character P
- 1110 0010 points to character b

8.5.4 CGRAM

Up to 48 user-defined characters may be stored in the Character Generator RAM (CGRAM), depending on the configuration of CGRAM and CGROM (RR[1:0]) with the RAM_ROM_config command (see Section 8.1.1.8).

With the RAM_ROM_config command, the CGROM column 1 and column 2 can be overlaid with the corresponding CGRAM columns.

RR[1:0] = 00 — 16 CGRAM characters in CGRAM column 0

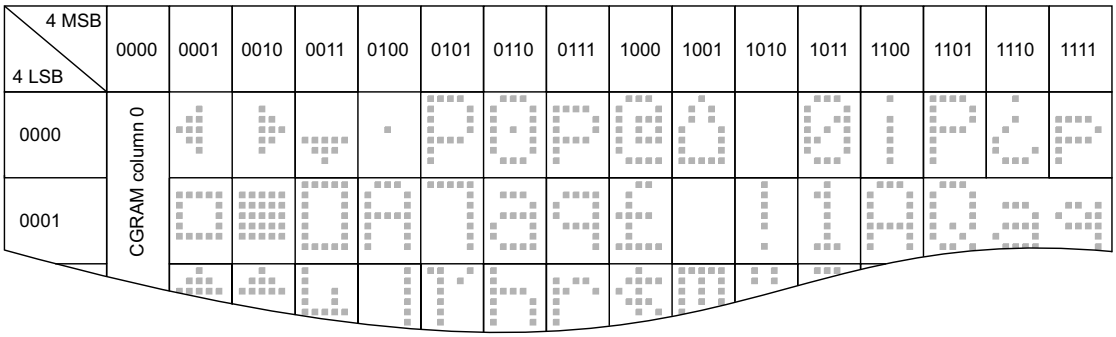
RR[1:0] = 01 — 32 CGRAM characters in CGRAM column 0 and CGRAM column 2

RR[1:0] = 10 — 32 CGRAM characters in CGRAM column 0 and CGRAM column 1

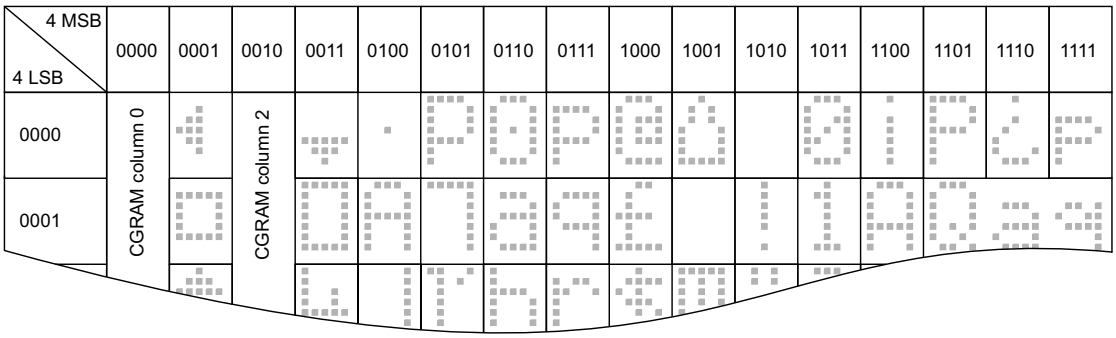
RR[1:0] = 11 — 48 CGRAM characters in CGRAM column 0, CGRAM column 1 and CGRAM column 2

Figure 36 exemplifies the overlay of the CGROM with the CGRAM columns.

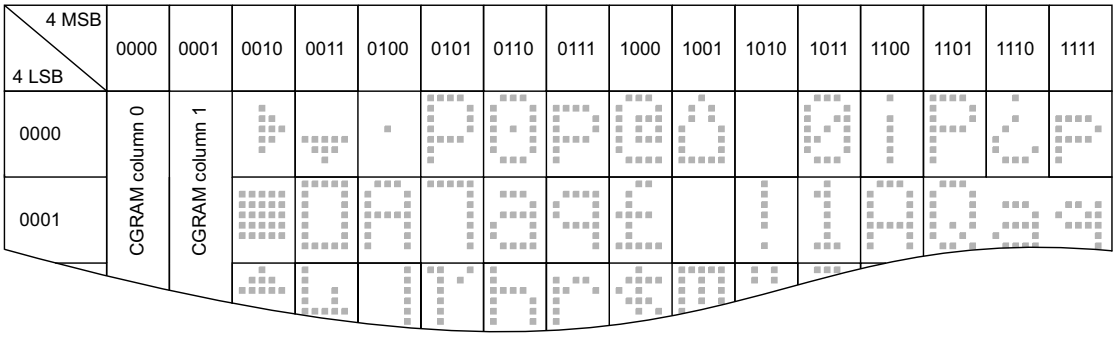
CGRAM and CGROM configuration with RR[1:0] = 00



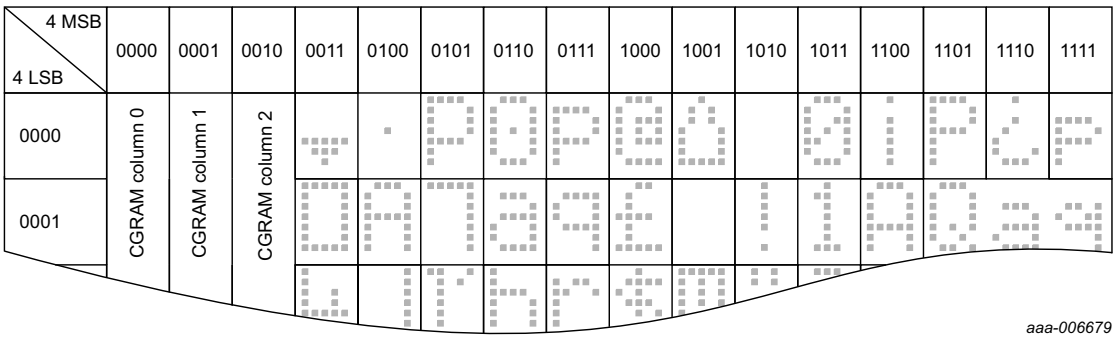
CGRAM and CGROM configuration with RR[1:0] = 01



CGRAM and CGROM configuration with RR[1:0] = 10



CGRAM and CGROM configuration with RR[1:0] = 11



aaa-006679

Fig 36. Configuration of CGROM and CGRAM with RR[1:0]

8.5.4.1 CGRAM addressing

For addressing, the CGRAM the following steps have to be taken (see Figure 31):

- Select the column of the CGRAM (SMB[2:0]) with the Sel_mem_bank command (see Section 8.1.1.9)
- Set the requested address counter (ADD[6:0]) with the Set_mem_addr command (see Section 8.1.1.10)
- Write data to the CGRAM with the Write_data command (WD[4:0]) (see Section 8.1.1.12)
- Read the data from the CGRAM with the Read_data command (RD[4:0]) (see Section 8.1.1.11)

8.5.4.2 User-defined characters and symbols

User-defined characters can be stored in the CGRAM. The content of the CGRAM is lost during power-down, therefore the CGRAM has to be rewritten after every power-on.

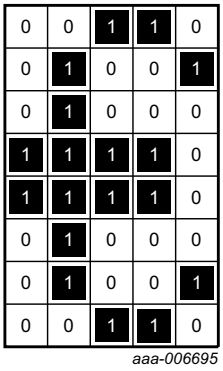


Fig 37. User-defined euro currency sign

Below some source code is printed, which shows how a user-defined character can be coded - in this case the euro currency sign. The display used is a 2 lines by 20 characters display and the interface is the I^2C-bus:

```
// Write a user-defined character into the CGRAM
startI2C();
// PCA2117 slave address for write, SA0 is connected to VDD
SendI2CAddress(0x76);
// MSB (Continuation bit CO) = 0, no more control bytes will follow, RS[1:0]= 10
// next byte is command byte on register page "10"
i2c_write(0x40);
// 2 lines x 20 chars, 1/18 duty. Next byte will be another command.
i2c_write(0x32);
// Repeated Start condition
startI2C();
SendI2CAddress(0x76);
// MSB (Continuation bit CO) = 0, no more control bytes will follow, RS[1:0]= 00
// next bytes are command bytes on register page "00"
i2c_write(0x00);
// Select Memory Bank 1: Column 0 of CGRAM
```

```
i2c_write(0x11);
// Select Memory Address 0: Point to first row in the CGRAM
i2c_write(0x80);
// Repeated Start condition
startI2C();
SendI2CAddress(0x76);
// MSB (Continuation bit CO) = 0, no more control bytes will follow, RS[1:0]= 01
// next bytes are RAM data bytes written in the CGRAM column 0
i2c_write(0x20);
// Here the data bytes to define the character
// Behind the write commands the 5x8 dot matrix is shown, the 1 represents a on pixel.
// The Euro currency character can be recognized by the 0/1 pattern (see Figure 37)
// 00110
i2c_write(0x06); // 00110
i2c_write(0x09); // 01001
i2c_write(0x08); // 01000
i2c_write(0x1E); // 11110
i2c_write(0x1E); // 11110
i2c_write(0x08); // 01000
i2c_write(0x09); // 01001
i2c_write(0x06); // 00110
i2c_stop();
// Until here the definition of the character and writing it into the CGRAM. Now it
// still has to be displayed. See below.
// PCA2117, setting of proper display modes
startI2C();
// PCA2117 slave address for write, SA0 is connected to VDD
SendI2CAddress(0x76);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 10
// next byte is a command byte on register page "10"
i2c_write(0xC0);
// Set display configuration to right to left, column 80 to 1. Row data displ. top to
// bottom 1 to 16. P-bit='1' Q-bit = '1
i2c_write(0x06);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 10
// next byte is a command byte on register page "10"
i2c_write(0xC0);
// Set to character mode, full display, icon blink disabled
i2c_write(0x08);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 11
// next byte is a command byte on register page "11"
i2c_write(0xE0);
// Set voltage multiplier to 2 and enable chargepump
i2c_write(0x84);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 11
// next byte is a command byte on register page "11"
i2c_write(0xE0);
// Set Vlcda MSB
i2c_write(0xA2);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 11
// next byte is a command byte on register page "11"
```

```
i2c_write(0xE0);
// Set Vlcda LSB
i2c_write(0x90);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 10
// next byte is a command byte on register page "10"
i2c_write(0xC0);
// Display control: set display on, cursor off, no blink
i2c_write(0x24);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 00
// next byte is a command byte on register page "00"
i2c_write(0x80);
// Select Memory Bank 0: DDRAM
i2c_write(0x10);
// MSB (Continuation bit CO) = 1, more control bytes will follow, RS[1:0]= 00
// next byte is a command byte on register page "00"
i2c_write(0x80);
// Set Memory Address to be 0
i2c_write(0x80);
// MSB (Continuation bit CO) = 0, last control bytes, RS[1:0]= 10
// next bytes are command bytes on register page "10"
i2c_write(0x40);
// Entry mode set, increase DDRAM after access, no shift
i2c_write(0x2A);
// Clear entire display
i2c_write(0x00);
// Return home, set DDRAM address 0 in address counter
i2c_write(0x01);
// Repeated Start condition because RS bits need to point to RAM data registers
startI2C();
// PCA2117 slave address for write, SA0 is connected to VDD
SendI2CAddress(0x76);
// MSB (Continuation bit CO) = 0, last control bytes, RS[1:0]= 01
// next bytes are RAM data bytes written in DDRAM at address 0
i2c_write(0x20);
// Write the character at address 0, which is the previously defined Euro currency
// character
i2c_write(0x00):
i2c_stop();
```

8.5.5 ICON-RAM

To display an icon, see Figure 31:

1. Select the ICON-RAM with SMB[2:0] = 100 of the Sel_mem_bank command.
2. Set the address with the Set_mem_addr command.
3. Write the data with WD[4:0] of the Write_data command.

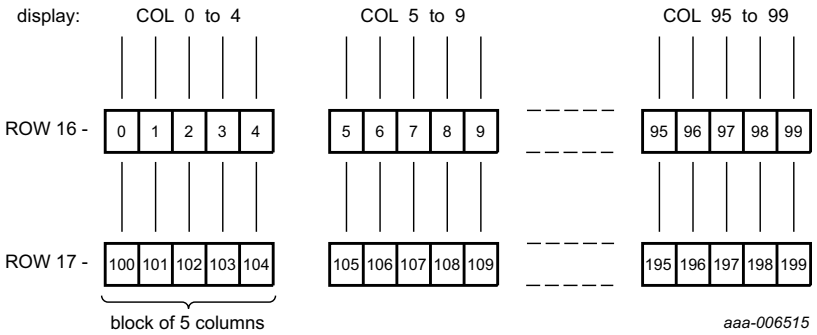


Fig 38. Icon to row/column mapping

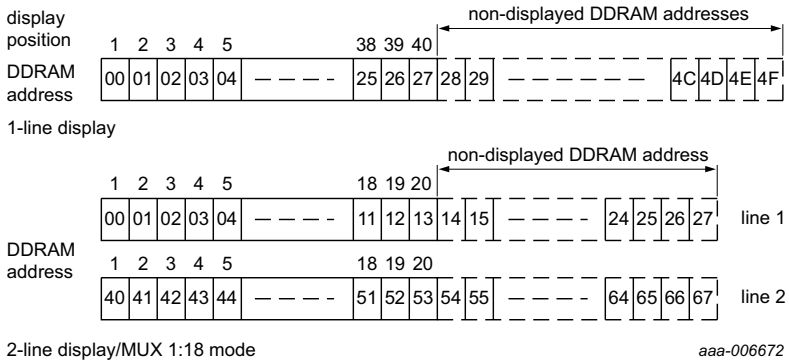
Table 38. Icon to ICON-RAM mapping table

ICON-RAM address	blink phase	ICON-RAM bits							
		7	6	5	4	3	2	1	0
00h	even	-	-	-	icon 0	icon 1	icon 2	icon 3	icon 4
01h	even	-	-	-	icon 5	icon 6	icon 7	icon 8	icon 9
02h	even	-	-	-	icon 10	icon 11	icon 12	icon 13	icon 14
03h	even	-	-	-	icon 15	icon 16	icon 17	icon 18	icon 19
:	:	:	:	:	:	:	:	:	:
26h	even	-	-	-	icon 190	icon 191	icon 192	icon 193	icon 194
27h	even	-	-	-	icon 195	icon 196	icon 197	icon 198	icon 199
28h	odd	-	-	-	icon 0	icon 1	icon 2	icon 3	icon 4
29h	odd	-	-	-	icon 5	icon 6	icon 7	icon 8	icon 9
:	:	:	:	:	:	:	:	:	:
4Ch	odd	-	-	-	icon 180	icon 181	icon 182	icon 183	icon 184
4Dh	odd	-	-	-	icon 185	icon 186	icon 187	icon 188	icon 189
4Eh	odd	-	-	-	icon 190	icon 191	icon 192	icon 193	icon 194
4Fh	odd	-	-	-	icon 195	icon 196	icon 197	icon 198	icon 199

8.5.6 DDRAM

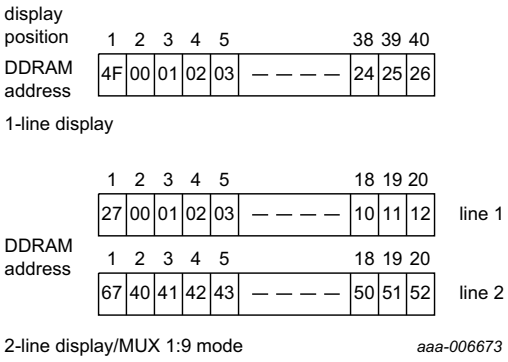
The Display Data RAM (DDRAM) stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general-purpose RAM.

The basic RAM to display addressing scheme is shown in Figure 39 to Figure 41. With no display shift, the characters represented by the codes in the first 40 RAM locations starting at address 00h are displayed in line 1.



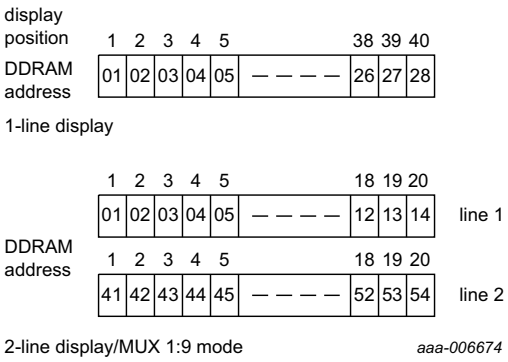
All addresses are shown in hex.

Fig 39. DDRAM to display mapping: no shift



All addresses are shown in hex.

Fig 40. DDRAM to display mapping: right shift



All addresses are shown in hex.

Fig 41. DDRAM to display mapping: left shift

When data is written to or read from the DDRAM, wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together. The address ranges and wrap-around operations for the various modes are shown in Table 39.

Table 39. Address space and wrap-around operation

Mode	1 × 40	2 × 20	1 × 20
Address space	00h to 4Fh	00h to 27h; 40h to 67h	00h to 27h
Read/write wrap-around (moves to next line)	4Fh to 00h	27h to 40h; 67h to 00h	27h to 00h
Display shift wrap-around (stays within line)	4Fh to 00h	27h to 00h; 67h to 40h	27h to 00h

8.5.7 Cursor control circuit

The cursor control circuit generates the cursor underline and/or cursor blink as shown in Figure 42 at the DDRAM address contained in the address counter.

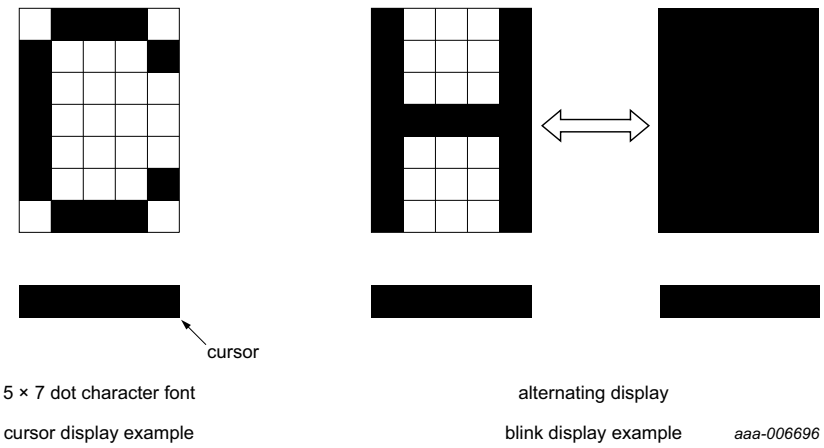


Fig 42. Cursor and blink display examples

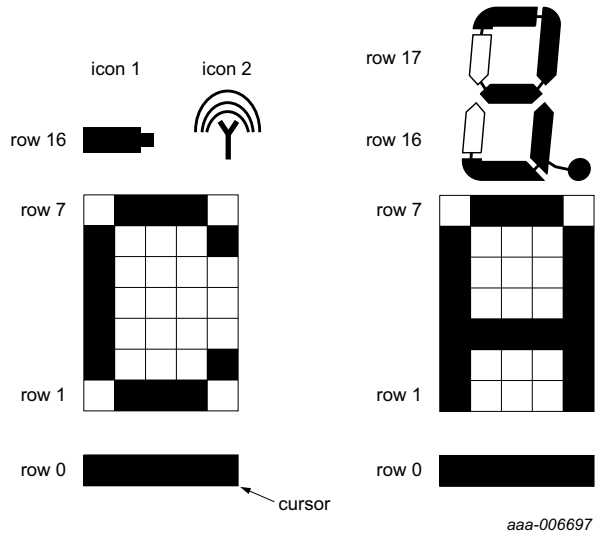


Fig 43. Display example with icons

9. Bus interfaces

9.1 Control byte and register selection

After initiating the communication over the bus and sending the slave address (I^2C-bus, see Section 9.2) or subaddress (SPI-bus, see Section 9.3), a control byte follows. The purpose of this byte is to indicate both, the content for the following data bytes (RAM or command) and to indicate that more control bytes will follow.

Typical sequences could be:

- Slave address/subaddress - control byte - command byte - control byte - command byte - control byte - command byte - end
- Slave address/subaddress - control byte - RAM byte - RAM byte - RAM byte - end
- Slave address/subaddress - control byte - command byte - control byte - RAM byte - end

This allows sending a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access. In this way, it is possible to configure the device and then fill the display RAM with little overhead. The display bytes are stored in the display RAM at the address specified by the data pointer.

Table 40. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6 to 5	RS[1:0]		**register selection**
		00, 10, 11	command register
		01	RAM data
4 to 0	-	-	unused

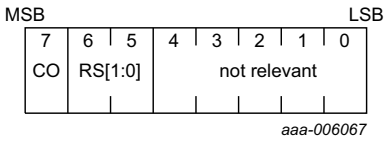


Fig 44. Control byte format

9.2 I^2C interface

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

In Chip-On-Glass (COG) applications, where the track resistance between the SDA output pin to the system SDA input line can be significant, the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance may generate a voltage divider. As a

consequence it may be possible that the acknowledge cycle, generated by the LCD driver, cannot be interpreted as logic 0 by the master. Therefore it is an advantage for COG applications to have the acknowledge output separated from the data line. For that reason, the SDA line of the PCA2117 is split into SDAIN and SDAOUT.

In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAOUT pin to the system SDAIN line to guarantee a valid LOW level.

By splitting the SDA line into SDAIN and SDAOUT (having the SDAOUT open circuit), the device could be used in a mode that ignores the acknowledge cycle. Separating the acknowledge output from the serial data line can avoid design efforts to generate a valid acknowledge level. However, in that case the I^2C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

By connecting pin SDAOUT to pin SDAIN the SDAIN line becomes fully I^2C-bus compatible (see Figure 45). The following definition assumes that SDAIN and SDAOUT are connected and refers to the pair as SDA.

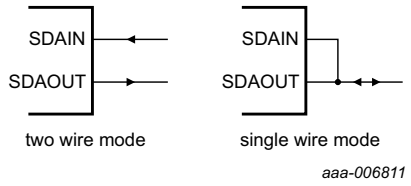


Fig 45. SDAOUT and SDAIN configuration

9.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 46).

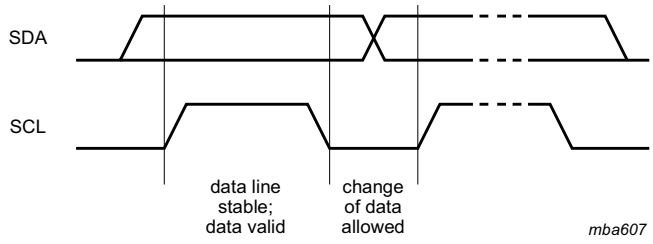


Fig 46. Bit transfer

9.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

2. For further information, consider the NXP application note: Ref. 1 “AN10170”.

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 47.

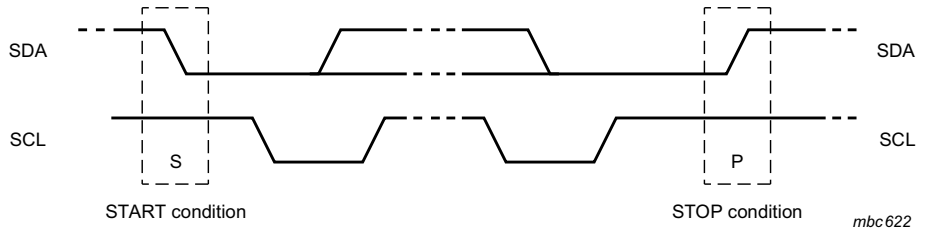


Fig 47. Definition of START and STOP conditions

9.2.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 48.

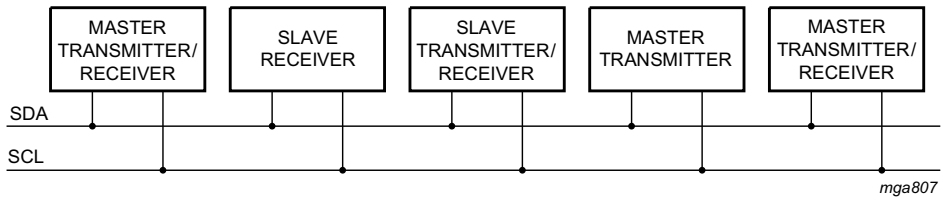


Fig 48. System configuration

9.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^2C-bus is shown in Figure 49.

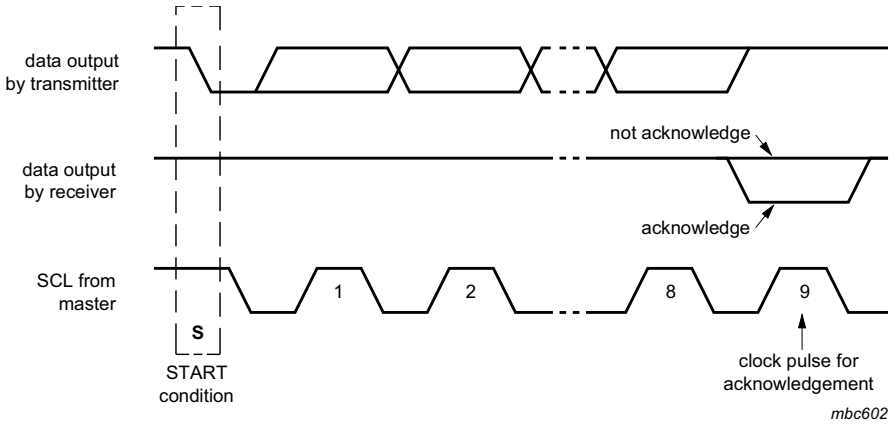


Fig 49. Acknowledgement on the I²C-bus

9.2.5 I²C-bus controller

The PCA2117 acts as an I²C-bus slave. It does not initiate I²C-bus transfers.

9.2.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

9.2.7 I²C-bus slave address

Device selection depends on the I²C-bus slave address.

Two different I²C-bus slave addresses can be used to address the PCA2117 (see Table 41).

Table 41. I²C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
slave address	0	1	1	1	0	1	SA0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$ (see Table 42).

Table 42. R/$\overline{W}$-bit description

R/$\overline{W}$	**Description**
0	write data
1	read data

Bit 1 of the slave address is defined by connecting the input SA0 to either V_{SS1} (logic 0) or V_{DD1} (logic 1). Therefore, two instances of PCA2117 can be distinguished on the same I²C-bus.

9.2.8 I²C-bus protocol

Table 43. Example: Writing to RAM by I²C-bus

Bits labeled as - are ignored.

Commands and signals	Values							
1. Select RAM bank and set address pointer								
I²C-START	*S*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Acknowledge from PCA2117	*A*							
Command: Sel_mem_bank	0	0	0	1	0	SMB[2:0]		
DDRAM						0	0	0
Acknowledge from PCA2117	*A*							
Command: Set_mem_addr	1	ADD[6:0]						
address 0h		0	0	0	0	0	0	0
Acknowledge from PCA2117	*A*							
2. Select write RAM data								
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	1	-	-	-	-	-
Acknowledge from PCA2117	*A*							
Command: Write_data	writing 0 to n byte							
Acknowledge from master after each byte	*A*							
I²C-STOP	*P*							

The I²C-bus protocol is shown in Table 43. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two slave addresses available. All PCA2117 with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCA2117 with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte (see Section 9.1) follows which defines if the next byte is RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data.

In this way, it is possible to configure the device and then fill the display RAM with little overhead.

The display bytes are stored in the display RAM at the address specified by the data pointer.

The acknowledgement after each byte is made only by the addressed PCA2117. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a repeated START may be issued to RESTART an I²C-bus access.

If a register readout is made, the R/$\overline{W}$ bit must be logic 1 and then the next data byte following is provided by the PCA2117 as shown in Table 44.

Table 44. Example: Reading from RAM by I²C-bus

Bits labeled as - are ignored.

Commands and signals	Values							
1. Straight forward example								
1.1 Select RAM bank and set address pointer								
I²C-START	*S*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Acknowledge from PCA2117	*A*							
Command: Sel_mem_bank	0	0	0	1	0	SMB[2:0]		
DDRAM						0	0	0
Acknowledge from PCA2117	*A*							
Command: Set_mem_addr	1	ADD[6:0]						
address 0h		0	0	0	0	0	0	0
Acknowledge from PCA2117	*A*							
1.2 Select read RAM data								
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	1	-	-	-	-	-
Acknowledge from PCA2117	*A*							
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								1
Acknowledge from PCA2117	*A*							
Command: Read_data	reading 0 to n byte							
Acknowledge from master after each byte	*A*							
I²C-STOP	*P*							

Table 44. Example: Reading from RAM by I²C-bus *…continued*

Bits labeled as - are ignored.

Commands and signals	Values							
2. Extended example: select new mem address								
2.1 Setting the address pointer[1]								
I²C-START	*S*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Acknowledge from PCA2117	*A*							
Command: Set_mem_addr	1	ADD[6:0]						
address 40h		1	0	0	0	0	0	0
Acknowledge from PCA2117	*A*							
2.2 Select read RAM data from new mem address								
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	1	-	-	-	-	-
Acknowledge from PCA2117	*A*							
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								1
Acknowledge from PCA2117	*A*							
Command: Read_data	reading 0 to n byte							
Acknowledge from master after each byte	*A*							
I²C-STOP	*P*							
3. Extended example: decrementing address pointer								
3.1 Setting the address pointer[1]								
I²C-START	*S*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Acknowledge from PCA2117	*A*							
Command: Set_mem_addr	1	ADD[6:0]						
address 4Fh		1	0	0	1	1	1	1
Acknowledge from PCA2117	*A*							

Table 44. Example: Reading from RAM by I²C-bus *...continued*

Bits labeled as - are ignored.

Commands and signals	Values							
3.2 Select decrement address pointer								
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		1	0	-	-	-	-	-
Acknowledge from PCA2117	*A*							
Command: Entry_mode_set	0	0	1	0	1	0	0	0
Acknowledge from PCA2117	*A*							
3.3 Select read RAM data								
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								0
Acknowledge from PCA2117	*A*							
CO	0							
RS[1:0]		0	1	-	-	-	-	-
Acknowledge from PCA2117	*A*							
I²C-RESTART	*Sr*							
Slave address	0	1	1	1	0	1	SA0	
R/$\overline{W}$								1
Acknowledge from PCA2117	*A*							
Command: Read_data	reading 0 to n byte							
Acknowledge from master after each byte	*A*							
I²C-STOP	*P*							

[1] Assuming that general-purpose RAM was already selected.

9.3 SPI interface

Data transfer to the device is made via a four-line SPI-bus (see Table 45). The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is inactive.

Table 45. Serial interface

Symbol	Function	Description
$\overline{CE}$	chip enable input; active LOW[1]	when HIGH, the interface is reset
SCL	serial clock input	input may be higher than V_{DD1}
SDI/SDAIN	serial data input	input may be higher than V_{DD1}; input data is sampled on the rising edge of SCL
SDO	serial data output	-

[1] The chip enable must not be wired permanently LOW.

9.3.1 SPI-bus data transfer

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the MSB sent first.

The transmission is controlled by the active LOW chip enable signal $\overline{CE}$. The first byte transmitted is the subaddress byte.

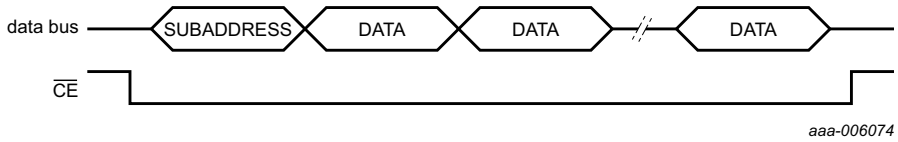


Fig 50. SPI data transfer overview

The subaddress byte opens the communication with a read/write bit and a subaddress. The subaddress is used to identify multiple devices on one SPI bus.

Table 46. Subaddress byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		**data read or write selection**
		0	write data
		1	read data
6 to 5	SA	01	**Subaddress**; other codes cause the device to ignore data transfer
4 to 0	-		unused

After the subaddress byte, a control byte follows (see Section 9.1). The purpose of this byte is to indicate the content for the following data bytes (RAM, command or control byte).

In this way, it is possible to send a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access.

Table 47. Example: Writing to RAM by SPI-bus

Bits labeled as - are ignored.

Commands and signals	Values							
1.1 Select RAM bank and set address pointer								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Command: Sel_mem_bank	0	0	0	1	0	SMB[2:0]		
DDRAM						0	0	0
Command: Set_mem_addr	1	ADD[6:0]						
address 0h		0	0	0	0	0	0	0
$\overline{CE}$ *HIGH*								
1.2 Select write RAM data								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	1	-	-	-	-	-
Command: Write_data	writing 0 to n byte							
$\overline{CE}$ *HIGH*								

Table 48. Example: Reading from RAM by SPI-bus

Bits labeled as - are ignored.

Commands and signals	Values							
1. Straight forward example								
1.1 Select RAM bank and set address pointer								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Command: Sel_mem_bank	0	0	0	1	0	SMB[2:0]		
DDRAM						0	0	0
Command: Set_mem_addr	1	ADD[6:0]						
address 0h		0	0	0	0	0	0	0
$\overline{CE}$ *HIGH*								
1.2 Select read RAM data								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	1	-	-	-	-	-
$\overline{CE}$ *HIGH*								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	1							
Subaddress		0	1	-	-	-	-	-
Command: Read_data	reading 0 to n byte							
$\overline{CE}$ *HIGH*								
2. Extended example: select new mem address								
2.1 Setting the address pointer[1]								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Command: Set_mem_addr	1	ADD[6:0]						
address 40h		1	0	0	0	0	0	0
$\overline{CE}$ *HIGH*								
2.2 Select read RAM data from new mem address								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	1	-	-	-	-	-

Table 48. Example: Reading from RAM by SPI-bus *...continued*

Bits labeled as - are ignored.

Commands and signals	Values							
$\overline{CE}$ *HIGH*								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	1							
Subaddress		0	1	-	-	-	-	-
Command: Read_data	reading 0 to n byte							
$\overline{CE}$ *HIGH*								
3. Extended example: decrementing address pointer								
3.1 Setting the address pointer[1]								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	0	-	-	-	-	-
Command: Set_mem_addr	1	ADD[6:0]						
address 4Fh		1	0	0	1	1	1	1
$\overline{CE}$ *HIGH*								
3.2 Select decrement address pointer								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		1	0	-	-	-	-	-
Command: Entry_mode_set	0	0	1	0	1	0	0	0
$\overline{CE}$ *HIGH*								
3.3 Select read RAM data								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	0							
Subaddress		0	1	-	-	-	-	-
CO	0							
RS[1:0]		0	1	-	-	-	-	-
$\overline{CE}$ *HIGH*								
$\overline{CE}$ *LOW*								
R/$\overline{W}$	1							
Subaddress		0	1	-	-	-	-	-
Command: Read_data	reading 0 to n byte							
$\overline{CE}$ *HIGH*								

[1] Assuming that general-purpose RAM was already selected.

10. Internal circuitry

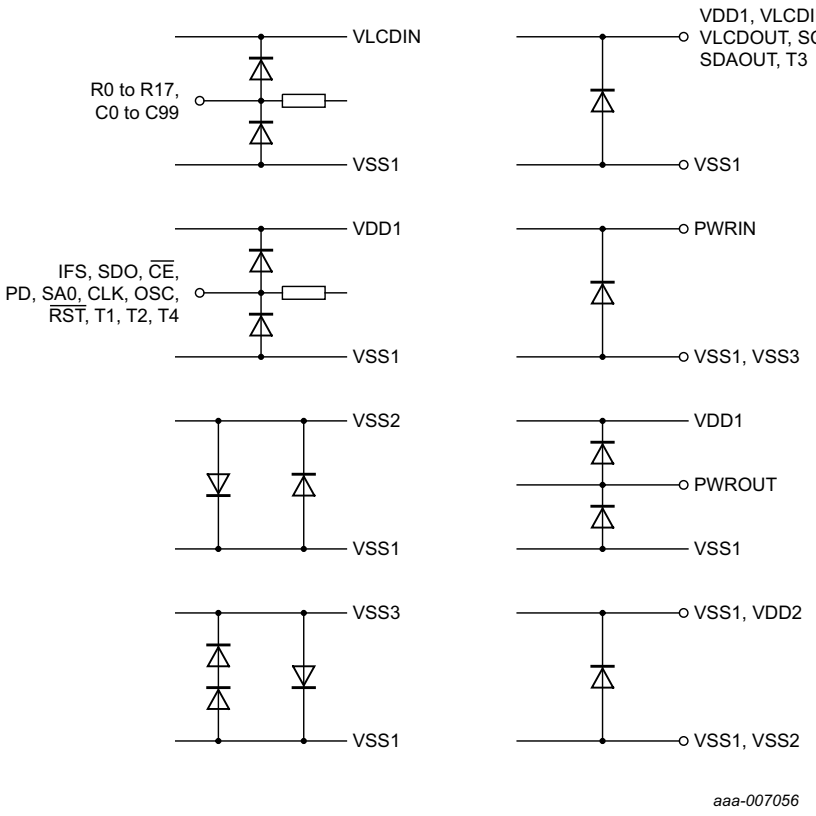


Fig 51. Device protection diagram

11. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

12. Limiting values

Table 49. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD1}	supply voltage 1	analog and digital	–0.5	+6.5	V
V_{DD2}	supply voltage 2	charge pump	–0.5	+6.5	V
I_{DD1}	supply current 1	analog and digital	–50	+50	mA
I_{DD2}	supply current 2	charge pump	–50	+50	mA
V_{LCD}	LCD supply voltage	external supply, input on pin VLCDIN	–0.5	+20	V
$I_{DD(LCD)}$	LCD supply current		–50	+50	mA
V_i	input voltage	on pins CLK, OSC, $\overline{RST}$, $\overline{PD}$, IFS, SCL, SDI/SDAIN, SA0, $\overline{CE}$	–0.5	+6.5	V
		on pin VLCDSENSE	–0.5	+20	V
I_I	input current		–10	+10	mA
V_O	output voltage	on pins C0 to C99, R0 to R17, VLCDOUT	–0.5	+20	V
		on pins SDO, SDAOUT, CLK	–0.5	+6.5	V
I_O	output current		–10	+10	mA
I_{SS}	ground supply current		–50	+50	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	±3000	V
I_{lu}	latch-up current	[2]	-	100	mA
T_{stg}	storage temperature	[3]	–65	+150	°C
T_{amb}	ambient temperature	operating device	–40	+105	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 8 “JESD22-A114”.

[2] Pass level; latch-up testing according to Ref. 10 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[3] According to the store and transport requirements (see Ref. 13 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

13. Static characteristics

Table 50. Static characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD1}	supply voltage 1		2.5	-	5.5	V
V_{DD2}	supply voltage 2		2.5	-	5.5	V
V_{LCD}	LCD supply voltage	$V_{LCD} \geq V_{DD2}$				
		external supply, input on pin VLCDIN	4.0	-	16.0	V
		internal supply, output on pin VLCDOUT	4.0	-	16.0	V
I_{DD1}	supply current 1	on pin V_{DD1}; see Figure 52				
		default condition after power-on and Initialize command	-	40[1]	59[2]	µA
		display enabled; internal clock	-	95[1]	-	µA
I_{DD2}	supply current 2	on pin V_{DD2}				
		default condition after power-on and Initialize command; charge pump off	-	0	-	µA
		V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled; see Figure 53	-	25	-	µA
$I_{DD(LCD)}$	LCD supply current	on pin VLCDIN; external V_{LCD} = 8 V				
		display disabled	-	7	12	µA
		MUX 1:18; 1/4 bias; f_{fr} = 80 Hz; all display elements on; frame inversion mode; display enabled; no display attached; see Figure 54	-	70	-	µA
$I_{DD(pd)}$	power-down mode supply current	on pin VDD1; pin PD is HIGH; V_{DD1} = 5 V; T_{amb} = 25 °C	-	2	-	µA

Table 50. Static characteristics *...continued*

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Accuracy						
ΔV_{LCD}	LCD voltage variation	on pin VLCDOUT; internal V_{LCD}; V_{LCD} = 8 V; T_{amb} = 25 °C; see Figure 55	7.9	8	8.1	V
Δf_{fr}	frame frequency variation	internal clock; f_{fr} = 80 Hz; T_{amb} = 25 °C; see Figure 56	77	80	83	Hz
ΔT_{meas}	measurement temperature variation	T_{amb} = 25 °C	22	25	28	°C
Output resistance						
R_O	output resistance	on pin R0 to R17; external V_{LCD} = 8 V	-	1	-	kΩ
		on pin C0 to C99; external V_{LCD} = 8 V	-	2.5	-	kΩ
Logic						
On pins CLK, OSC, PD, $\overline{RST}$, IFS, SA0						
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	V_{DD1} + 0.3	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	μA
On pin CLK						
V_{OH}	HIGH-level output voltage		$0.8V_{DD1}$	-	V_{DD1} + 0.3	V
V_{OL}	LOW-level output voltage		−0.3	-	$0.2V_{DD1}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD1} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD1} = 5 V	1	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD1}$ or V_{SS1}	-	0	-	μA
I^2C-bus						
On pins SCL, SDI/SDAIN						
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	5.5	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	μA

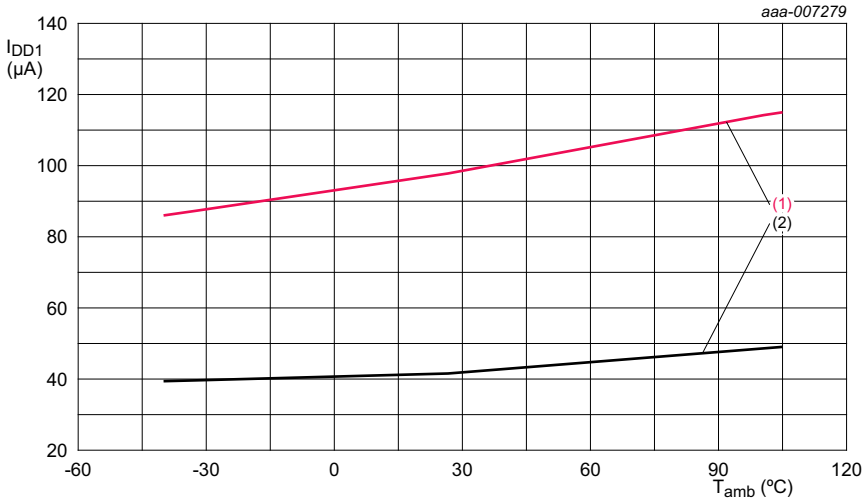
Table 50. Static characteristics *...continued*

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On pin SDAOUT						
V_O	output voltage		−0.5	-	+5.5	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V	6	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	µA
I_{LO}	output leakage current	$V_O = V_{SS1}$	-	0	-	µA
SPI-bus						
On pins SCL, SDI/SDAIN, $\overline{CE}$						
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	V_{DD1} + 0.3	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	µA
On pin SDO						
V_{OH}	HIGH-level output voltage		$0.8V_{DD1}$	-	V_{DD1} + 0.3	V
V_{OL}	LOW-level output voltage		−0.3	-	$0.2V_{DD1}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD1} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD1} = 5 V	1	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD1}$ or V_{SS1}	-	0	-	µA

[1] V_{DD1} = 5 V; T_{amb} = 25 °C.

[2] V_{DD1} = 5.5 V; T_{amb} = 105 °C.

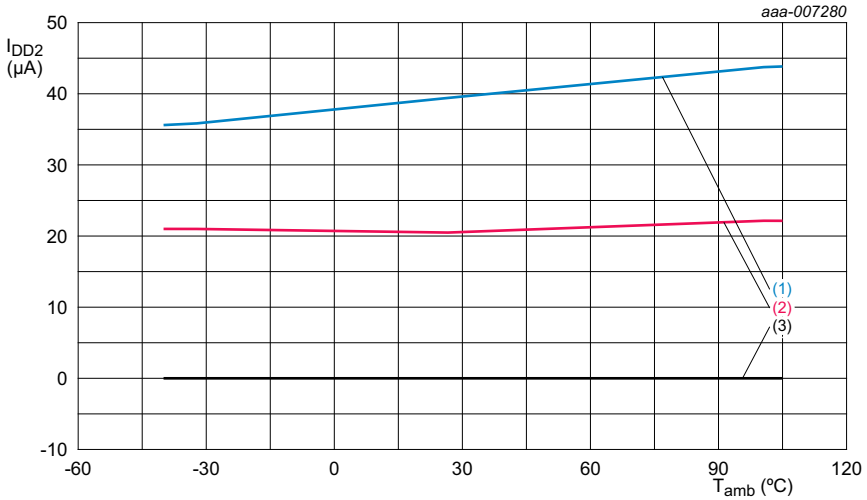


V_{DD1} = 5 V.

(1) Display enabled, oscillator enabled.

(2) Default conditions after power-on and initialization.

Fig 52. Typical I_{DD1} with respect to temperature

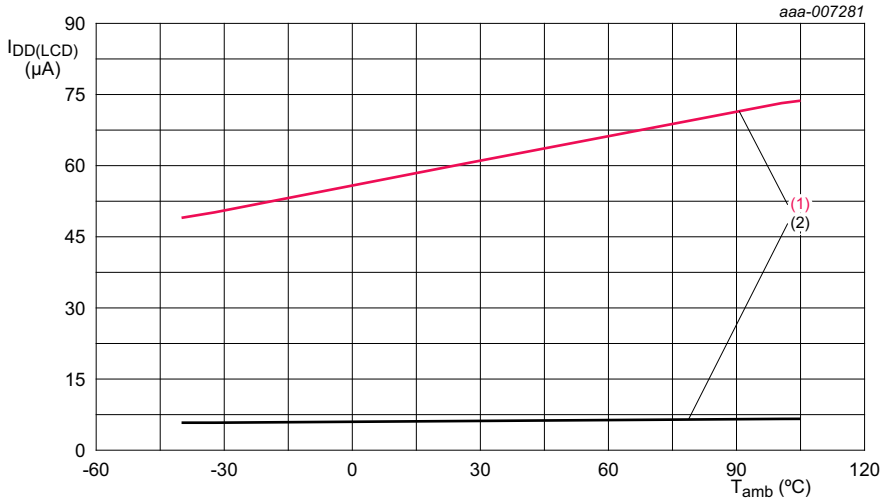


(1) V_{DD2} = 3 V; charge pump at $V_{LCD} = 3 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled.

(2) V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled.

(3) Default conditions after power-on and initialization; charge pump off.

Fig 53. Typical I_{DD2} with respect to temperature

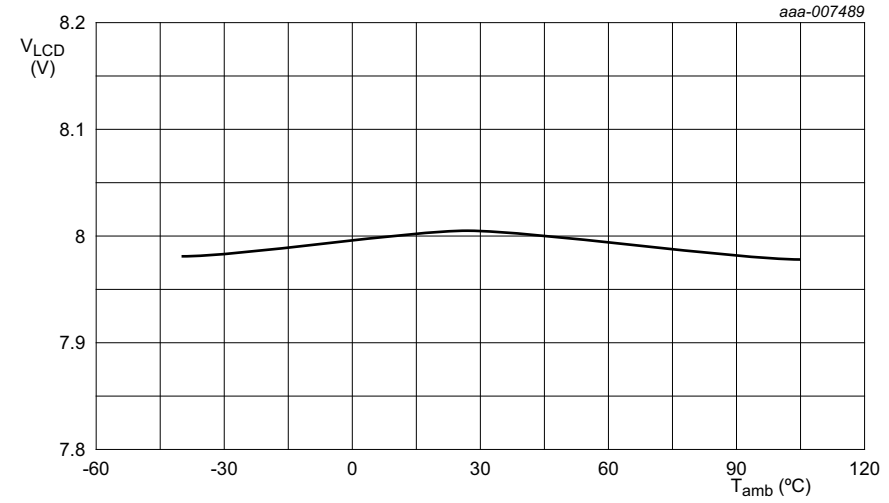


External V_{LCD} = 8 V.

(1) Driving mode 1:18, f_{fr} = 80 Hz; frame inversion; no-load; display enabled.

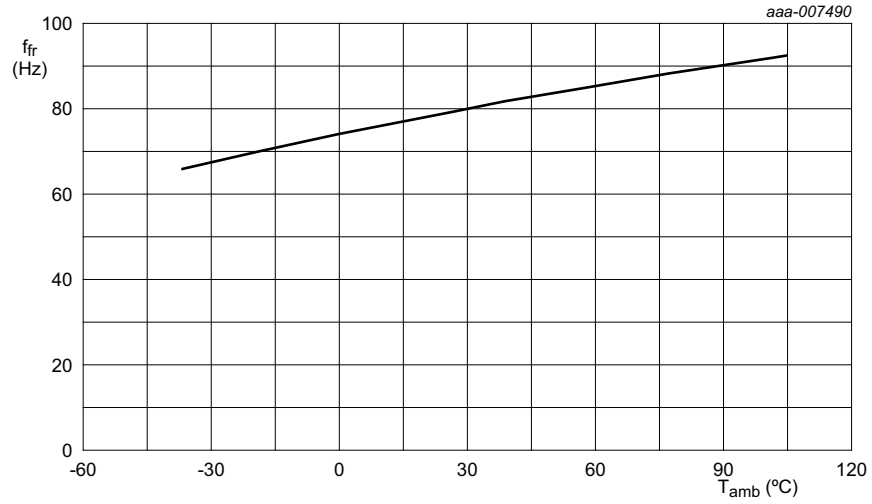
(2) Driving mode 1:18, f_{fr} = 80 Hz; frame inversion; no-load; display disabled.

Fig 54. Typical $I_{DD(LCD)}$ with respect to temperature



Conditions: V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; VLCDx[8:0] = 134h; temperature compensation disabled.

Fig 55. Typical V_{LCD} variation with respect to temperature



Conditions: frame frequency prescaler = 00111; 80 Hz typical.

Fig 56. Typical frame frequency variation with respect to temperature

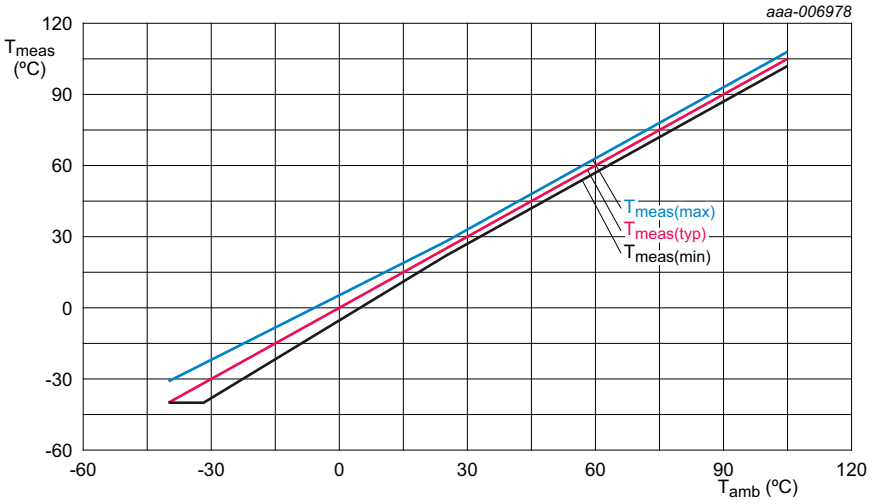


Fig 57. Measurement temperature variation with respect to temperature

14. Dynamic characteristics

14.1 General timing characteristics

Table 51. General dynamic characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(int)}$	internal clock frequency	on pin CLK; T_{amb} = 25 °C; FF[4:0] = 00111	61600	64000	66400	Hz
$f_{clk(ext)}$	external clock frequency	on pin CLK	36000	-	288000	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock source used	5	-	-	µs
$t_{clk(L)}$	LOW-level clock time		5	-	-	µs

14.2 I²C-bus timing characteristics

Table 52. I²C-bus timing characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL frequency		-	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
$t_{VD;DAT}$	data valid time	[2]	-	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	[3]	-	-	0.9	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_f	fall time	of both SDA and SCL signals	-	-	0.3	µs
t_r	rise time	of both SDA and SCL signals	-	-	0.3	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{w(spike)}$	spike pulse width		-	-	50	ns

[1] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1}.

[2] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[3] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

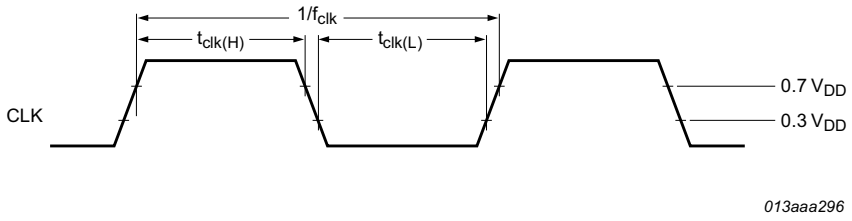


Fig 58. Driver timing waveforms

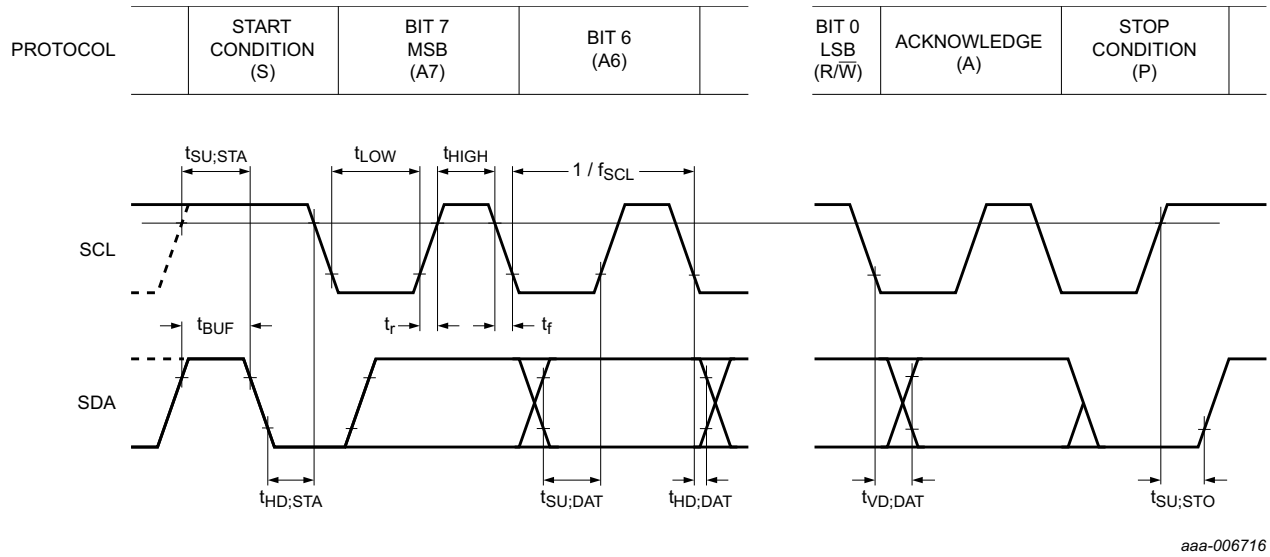


Fig 59. I²C-bus timing diagram

14.3 SPI-bus timing characteristics

Table 53. SPI-bus characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1} (see Figure 60).

Symbol	Parameter	Conditions	Min	Max	Unit
Pin SCL					
$f_{clk(SCL)}$	SCL clock frequency		-	3.0	MHz
t_{SCL}	SCL time		333	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	ns
$t_{clk(L)}$	clock LOW time		150	-	ns
t_r	rise time	for SCL signal	-	100	ns
t_f	fall time	for SCL signal	-	100	ns
Pin $\overline{CE}$					
$t_{su(CE\_N)}$	CE_N set-up time		30	-	ns
$t_{h(CE\_N)}$	CE_N hold time		30	-	ns
$t_{rec(CE\_N)}$	CE_N recovery time		30	-	ns
Pin SDI					
t_{su}	set-up time	set-up time for SDI data	30	-	ns
t_h	hold time	hold time for SDI data	30	-	ns
Pin SDO					
$t_{d(R)SDO}$	SDO read delay time	C_L = 100 pF	-	150	ns
$t_{dis(SDO)}$	SDO disable time	[1]	-	50	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	ns

[1] No load value; bus is held up by bus capacitance; use RC time constant with application values.

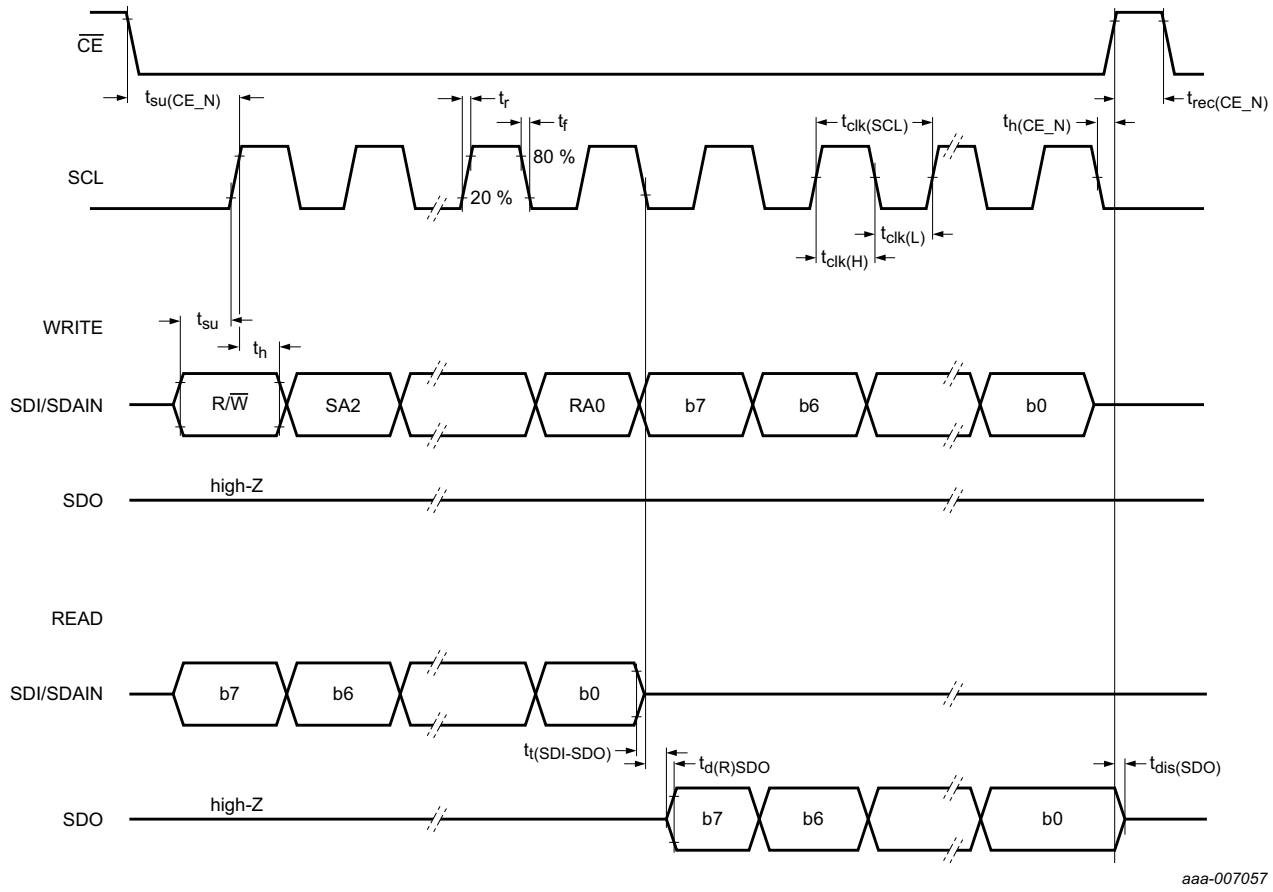


Fig 60. SPI-bus timing

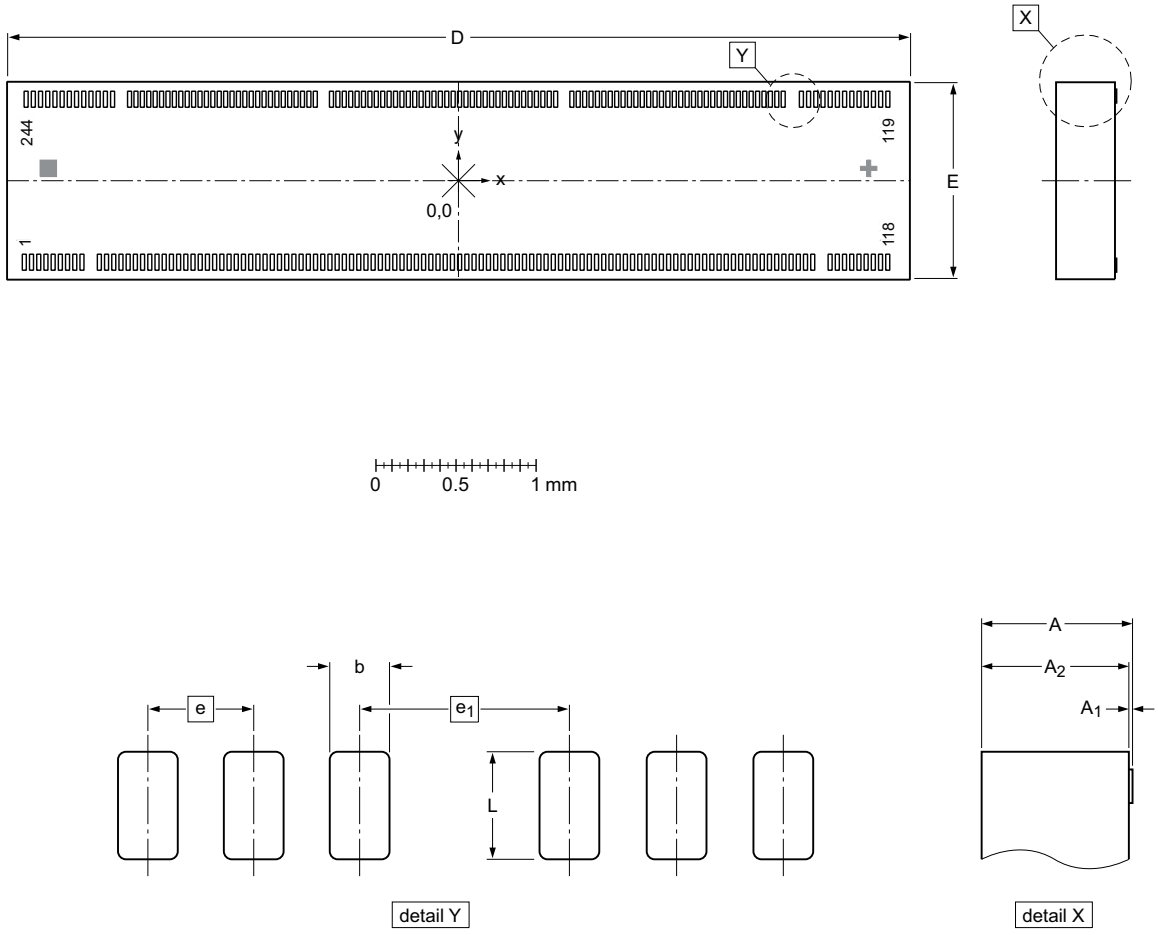
15. Test information

15.1 Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and is suitable for use in automotive applications.

16. Bare die outline

Bare die; 244 bumps **PCA2117DUG**



pca2117dug_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA2117DUG						~~13-03-20~~ 13-06-18

Fig 61. Bare die outline of PCA2117DUGx

Table 54. Dimensions of PCA2117DUGx

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E	e	e_1	L
max	-	0.018	-	-	-	-	-	-	-
nom	0.395	0.015	0.38	0.025	5.64	1.24	0.040	0.114	0.1
min	-	0.012	-	-	-	-	-	-	-

Table 55. Bump locations of PCA2117DUGx

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 61

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
R13	1	–2711.3	–509.0	-	R4	119	2681.5	509.0	-
	2	–2666.3	–509.0	–45.0		120	2636.5	509.0	45.0
	3	–2621.3	–509.0	–45.0		121	2591.5	509.0	45.0
R14	4	–2576.3	–509.0	–45.0	R3	122	2546.5	509.0	45.0
	5	–2531.3	–509.0	–45.0		123	2501.5	509.0	45.0
R15	6	–2486.3	–509.0	–45.0	R2	124	2456.5	509.0	45.0
	7	–2441.3	–509.0	–45.0		125	2411.5	509.0	45.0
R16	8	–2396.3	–509.0	–45.0	R1	126	2366.5	509.0	45.0
	9	–2351.3	–509.0	–45.0		127	2321.5	509.0	45.0
VLCDIN	10	–2242.7	–509.0	–108.6	R0	128	2276.5	509.0	45.0
	11	–2197.7	–509.0	–45.0		129	2231.5	509.0	45.0
	12	–2152.7	–509.0	–45.0	R17	130	2186.5	509.0	45.0
	13	–2107.7	–509.0	–45.0		131	2141.5	509.0	45.0
VLCDSENSE	14	–2062.7	–509.0	–45.0	C99	132	2027.9	509.0	113.6
	15	–2017.7	–509.0	–45.0	C98	133	1987.9	509.0	40.0
	16	–1972.7	–509.0	–45.0	C97	134	1947.9	509.0	40.0
VLCDOUT	17	–1927.7	–509.0	–45.0	C96	135	1907.9	509.0	40.0
	18	–1882.7	–509.0	–45.0	C95	136	1867.9	509.0	40.0
	19	–1837.7	–509.0	–45.0	C94	137	1827.9	509.0	40.0
	20	–1792.7	–509.0	–45.0	C93	138	1787.9	509.0	40.0
VSS2	21	–1747.7	–509.0	–45.0	C92	139	1747.9	509.0	40.0
	22	–1702.7	–509.0	–45.0	C91	140	1707.9	509.0	40.0
	23	–1657.7	–509.0	–45.0	C90	141	1667.9	509.0	40.0
	24	–1612.7	–509.0	–45.0	C89	142	1627.9	509.0	40.0
	25	–1567.7	–509.0	–45.0	C88	143	1587.9	509.0	40.0
	26	–1522.7	–509.0	–45.0	C87	144	1547.9	509.0	40.0
	27	–1477.7	–509.0	–45.0	C86	145	1507.9	509.0	40.0
	28	–1432.7	–509.0	–45.0	C85	146	1467.9	509.0	40.0
	29	–1387.7	–509.0	–45.0	C84	147	1427.9	509.0	40.0
	30	–1342.7	–509.0	–45.0	C83	148	1387.9	509.0	40.0

Table 55. Bump locations of PCA2117DUGx *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 61

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
VSS3	31	−1297.7	−509.0	−45.0	C82	149	1347.9	509.0	40.0
	32	−1252.7	−509.0	−45.0	C81	150	1307.9	509.0	40.0
	33	−1207.7	−509.0	−45.0	C80	151	1267.9	509.0	40.0
	34	−1162.7	−509.0	−45.0	C79	152	1227.9	509.0	40.0
VSS1	35	−1117.7	−509.0	−45.0	C78	153	1187.9	509.0	40.0
	36	−1072.7	−509.0	−45.0	C77	154	1147.9	509.0	40.0
	37	−1027.7	−509.0	−45.0	C76	155	1107.9	509.0	40.0
	38	−982.7	−509.0	−45.0	C75	156	1067.9	509.0	40.0
	39	−937.7	−509.0	−45.0	C74	157	1027.9	509.0	40.0
	40	−892.7	−509.0	−45.0	C73	158	987.9	509.0	40.0
	41	−847.7	−509.0	−45.0	C72	159	947.9	509.0	40.0
	42	−802.7	−509.0	−45.0	C71	160	907.9	509.0	40.0
	43	−757.7	−509.0	−45.0	C70	161	867.9	509.0	40.0
	44	−712.7	−509.0	−45.0	C69	162	827.9	509.0	40.0
	45	−667.7	−509.0	−45.0	C68	163	787.9	509.0	40.0
	46	−622.7	−509.0	−45.0	C67	164	747.9	509.0	40.0
	47	−577.7	−509.0	−45.0	C66	165	707.9	509.0	40.0
T1	48	−532.7	−509.0	−45.0	C65	166	606.9	509.0	101.0
	49	−487.7	−509.0	−45.0	C64	167	566.9	509.0	40.0
T2	50	−442.7	−509.0	−45.0	C63	168	526.9	509.0	40.0
	51	−397.7	−509.0	−45.0	C62	169	486.9	509.0	40.0
T4	52	−352.7	−509.0	−45.0	C61	170	446.9	509.0	40.0
	53	−307.7	−509.0	−45.0	C60	171	406.9	509.0	40.0
	54	−262.7	−509.0	−45.0	C59	172	366.9	509.0	40.0
OSC	55	−217.7	−509.0	−45.0	C58	173	326.9	509.0	40.0
	56	−172.7	−509.0	−45.0	C57	174	286.9	509.0	40.0
SA0	57	−127.7	−509.0	−45.0	C56	175	246.9	509.0	40.0
	58	−82.7	−509.0	−45.0	C55	176	206.9	509.0	40.0
IFS	59	−37.7	−509.0	−45.0	C54	177	166.9	509.0	40.0
	60	7.3	−509.0	−45.0	C53	178	126.9	509.0	40.0
VDD1	61	52.3	−509.0	−45.0	C52	179	86.9	509.0	40.0
	62	97.3	−509.0	−45.0	C51	180	46.9	509.0	40.0
	63	142.3	−509.0	−45.0	C50	181	6.9	509.0	40.0
	64	187.3	−509.0	−45.0	C49	182	−33.1	509.0	40.0
	65	232.3	−509.0	−45.0	C48	183	−73.1	509.0	40.0

Table 55. Bump locations of PCA2117DUGx *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 61

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
VDD2	66	277.3	−509.0	−45.0	C47	184	−113.1	509.0	40.0
	67	322.3	−509.0	−45.0	C46	185	−153.1	509.0	40.0
	68	367.3	−509.0	−45.0	C45	186	−193.1	509.0	40.0
	69	412.3	−509.0	−45.0	C44	187	−233.1	509.0	40.0
	70	457.3	−509.0	−45.0	C43	188	−273.1	509.0	40.0
	71	502.3	−509.0	−45.0	C42	189	−313.1	509.0	40.0
	72	547.3	−509.0	−45.0	C41	190	−353.1	509.0	40.0
	73	592.3	−509.0	−45.0	C40	191	−393.1	509.0	40.0
PD	74	637.3	−509.0	−45.0	C39	192	−433.1	509.0	40.0
	75	682.3	−509.0	−45.0	C38	193	−473.1	509.0	40.0
T3	76	727.3	−509.0	−45.0	C37	194	−513.1	509.0	40.0
	77	772.3	−509.0	−45.0	C36	195	−553.1	509.0	40.0
	78	817.3	−509.0	−45.0	C35	196	−593.1	509.0	40.0
	79	862.3	−509.0	−45.0	C34	197	−633.1	509.0	40.0
	80	907.3	−509.0	−45.0	C33	198	−673.1	509.0	40.0
PWROUT	81	952.3	−509.0	−45.0	C32	199	−713.1	509.0	40.0
	82	997.3	−509.0	−45.0	C31	200	−753.1	509.0	40.0
PWRIN	83	1042.3	−509.0	−45.0	C30	201	−793.1	509.0	40.0
	84	1087.3	−509.0	−45.0	C29	202	−894.1	509.0	101.0
	85	1132.3	−509.0	−45.0	C28	203	−934.1	509.0	40.0
	86	1177.3	−509.0	−45.0	C27	204	−974.1	509.0	40.0
	87	1222.3	−509.0	−45.0	C26	205	−1014.1	509.0	40.0
	88	1267.3	−509.0	−45.0	C25	206	−1054.1	509.0	40.0
	89	1312.3	−509.0	−45.0	C24	207	−1094.1	509.0	40.0
$\overline{CE}$	90	1357.3	−509.0	−45.0	C23	208	−1134.1	509.0	40.0
	91	1402.3	−509.0	−45.0	C22	209	−1174.1	509.0	40.0
CLK	92	1447.3	−509.0	−45.0	C21	210	−1214.1	509.0	40.0
	93	1492.3	−509.0	−45.0	C20	211	−1254.1	509.0	40.0
	94	1537.3	−509.0	−45.0	C19	212	−1294.1	509.0	40.0
$\overline{RST}$	95	1582.3	−509.0	−45.0	C18	213	−1334.1	509.0	40.0
	96	1627.3	−509.0	−45.0	C17	214	−1374.1	509.0	40.0
SDI/SDAIN	97	1672.3	−509.0	−45.0	C16	215	−1414.1	509.0	40.0
	98	1717.3	−509.0	−45.0	C15	216	−1454.1	509.0	40.0
	99	1762.3	−509.0	−45.0	C14	217	−1494.1	509.0	40.0
SDO	100	1807.3	−509.0	−45.0	C13	218	−1534.1	509.0	40.0
	101	1852.3	−509.0	−45.0	C12	219	−1574.1	509.0	40.0

Table 55. Bump locations of PCA2117DUGx *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 61

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
SCL	102	1897.3	−509.0	−45.0	C11	220	−1614.1	509.0	40.0
	103	1942.3	−509.0	−45.0	C10	221	−1654.1	509.0	40.0
	104	1987.3	−509.0	−45.0	C9	222	−1694.1	509.0	40.0
SDAOUT	105	2032.3	−509.0	−45.0	C8	223	−1734.1	509.0	40.0
	106	2077.3	−509.0	−45.0	C7	224	−1774.1	509.0	40.0
	107	2122.3	−509.0	−45.0	C6	225	−1814.1	509.0	40.0
	108	2167.3	−509.0	−45.0	C5	226	−1854.1	509.0	40.0
	109	2212.3	−509.0	−45.0	C4	227	−1894.1	509.0	40.0
R17	110	2320.9	−509.0	−108.6	C3	228	−1934.1	509.0	40.0
	111	2365.9	−509.0	−45.0	C2	229	−1974.1	509.0	40.0
R7	112	2410.9	−509.0	−45.0	C1	230	−2014.1	509.0	40.0
	113	2455.9	−509.0	−45.0	C0	231	−2054.1	509.0	40.0
R6	114	2500.9	−509.0	−45.0	R16	232	−2160.2	509.0	106.1
	115	2545.9	−509.0	−45.0		233	−2205.2	509.0	45.0
R5	116	2590.9	−509.0	−45.0	R8	234	−2250.2	509.0	45.0
	117	2635.9	−509.0	−45.0		235	−2295.2	509.0	45.0
	118	2680.9	−509.0	−45.0	R9	236	−2340.2	509.0	45.0
-	-	-	-	-		237	−2385.2	509.0	45.0
-	-	-	-	-	R10	238	−2430.2	509.0	45.0
-	-	-	-	-		239	−2475.2	509.0	45.0
-	-	-	-	-	R11	240	−2520.2	509.0	45.0
-	-	-	-	-		241	−2565.2	509.0	45.0
-	-	-	-	-	R12	242	−2610.2	509.0	45.0
-	-	-	-	-		243	−2655.2	509.0	45.0
-	-	-	-	-		244	−2700.2	509.0	45.0

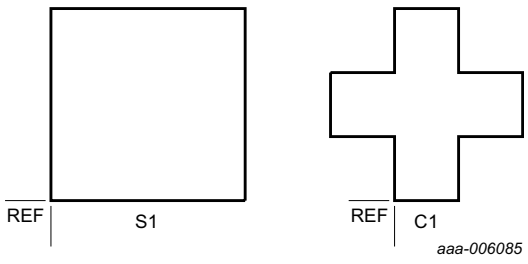


Fig 62. Alignment marks

Table 56. Alignment marking

All x/y coordinates represent the position of the REF point (see Figure 62) with respect to the center (x/y = 0) of the chip; see Figure 61.

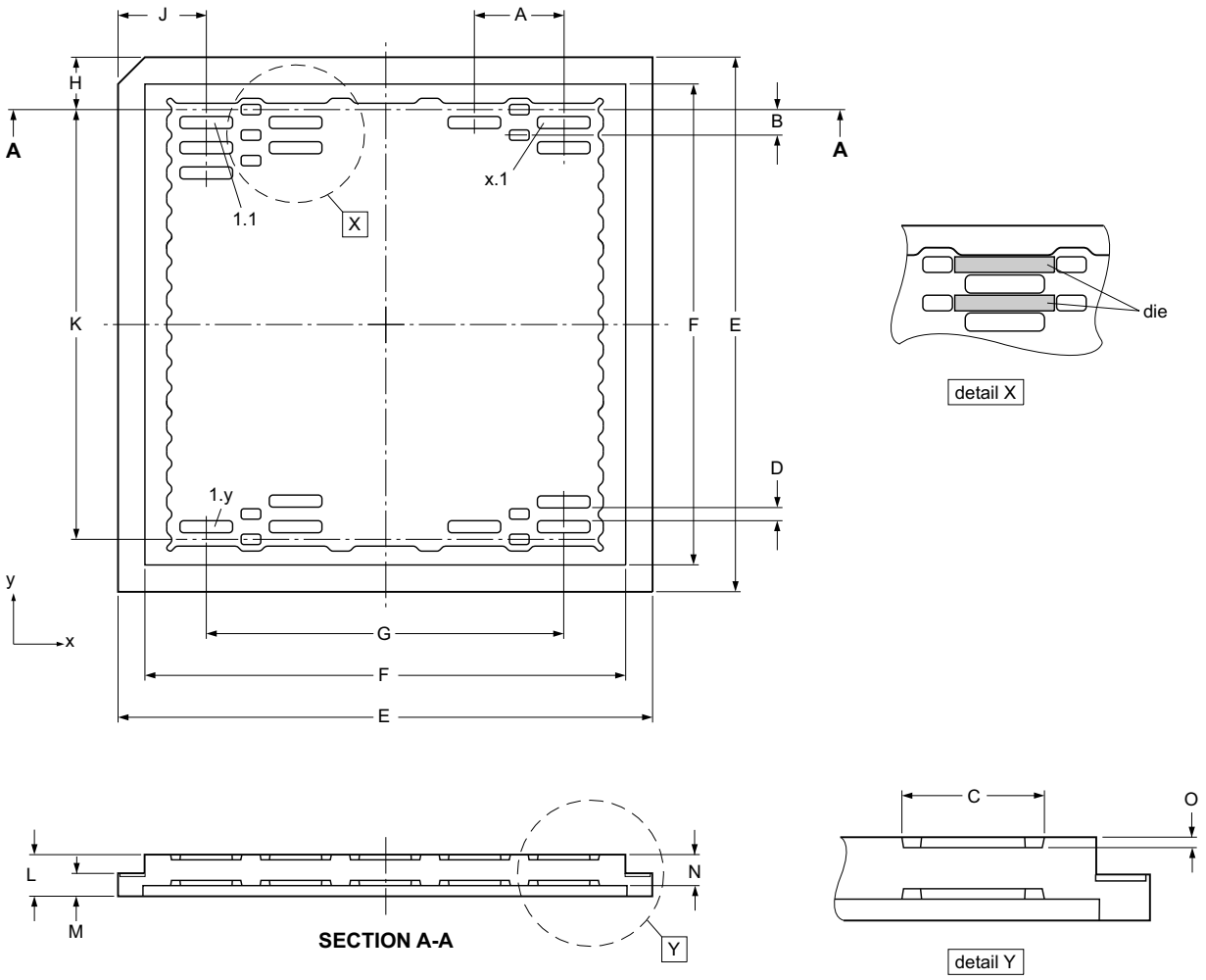
Symbol	Size (μm)	X (μm)	Y (μm)
S1	90 × 90	−2585.0	36.0
C1	90 × 90	2522.0	36

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

18. Packing information

18.1 Packing information on the tray



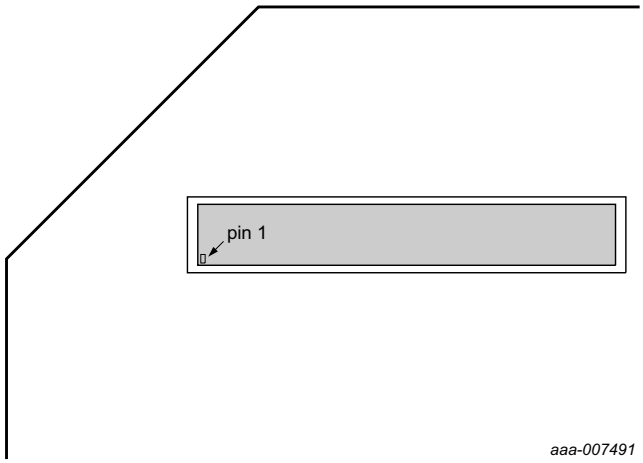
Schematic drawing, not drawn to scale. Top side view. For dimensions, see Table 57. Tray has pockets on both, top side and bottom side. The IC is stored with the active side up. To get the active side down, turn the tray.

Fig 63. Tray details of PCA2117DUGx

Table 57. Specification of 3 inch tray details

Tray details are shown in Figure 63. Nominal values without production tolerances.

Tray details														
Dimensions														
A	B	C	D	E	F	G	H	J	K	L	M	N	O	Unit
7.0	2.5	5.74	1.34	76.0	68.0	56.0	6.75	10.0	62.5	4.2	2.6	3.2	0.48	mm
Number of pockets														
x direction							y direction							
9							26							



The orientation of the IC in a pocket with active side up is indicated by the position of pin 1 with respect to the chamfer on the upper left corner of the tray.

Fig 64. Die alignment in the tray

19. Appendix

19.1 LCD character driver selection

Table 58. Selection of LCD character drivers

Type name	Number of				Character set	V_{DD1} (V)	V_{DD2} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temp. comp	T_{amb} (°C)	Interface	AEC-Q100
	Lines × Characters			Icons										
PCF2113AU	1 × 24	2 × 12	-	120	A	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2113DU	1 × 24	2 × 12	-	120	D	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2113EU	1 × 24	2 × 12	-	120	E	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2113WU	1 × 24	2 × 12	-	120	W	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2116AU	1 × 24	2 × 24	4 × 12	-	A	2.5 to 6	2.5 to 6	3.5 to 9	65	Y	N	–40 to 85	I²C / Parallel	N
PCF2116CU	1 × 24	2 × 24	4 × 12	-	C	2.5 to 6	2.5 to 6	3.5 to 9	65	Y	N	–40 to 85	I²C / Parallel	N
PCF2119AU	1 × 32	2 × 16	-	160	A	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2119DU	1 × 32	2 × 16	-	160	D	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2119FU	1 × 32	2 × 16	-	160	F	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2119IU	1 × 32	2 × 16	-	160	I	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2119RU	1 × 32	2 × 16	-	160	R	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF2119SU	1 × 32	2 × 16	-	160	S	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	–40 to 85	I²C / Parallel	N
PCF21219DUGR	1 × 32	2 × 16	-	160	R	1.5 to 5.5	2.2 to 4	2.2 to 6.5	220	Y	Y	–40 to 85	I²C / Parallel	N
PCA2117DUGR	1 × 40	2 × 20	-	200	R	2.5 to 5.5	2.5 to 5.5	4 to 16	45 to 360[1]	Y	Y	–40 to 105	I²C / SPI	Y
PCA2117DUGS	1 × 40	2 × 20	-	200	S	2.5 to 5.5	2.5 to 5.5	4 to 16	45 to 360[1]	Y	Y	–40 to 105	I²C / SPI	Y

[1] Software programmable.

20. Abbreviations

Table 59. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
CGRAM	Character Generator RAM
CGROM	Character Generator ROM
CRC	Cyclical Redundancy Check
DDRAM	Double Data Random Access Memory
COG	Chip-On-Glass
DC	Direct Current
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MUX	Multiplexer
NC	Numeric Code
OTP	One Time Programmable
PCB	Printed-Circuit Board
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
ROM	Read-Only Memory
SCL	Serial CLock line
SDA	Serial DAta line
SPI	Serial Peripheral Interface
XOR	EXclusive OR operator

21. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10439 —** Wafer Level Chip Size Package

[3] **AN10706 —** Handling bare die

[4] **AN10853 —** ESD and EMC sensitivity of IC

[5] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[6] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[7] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[8] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[9] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[10] **JESD78 —** IC Latch-Up Test

[11] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[12] **UM10204 —** I^2C-bus specification and user manual

[13] **UM10569 —** Store and transport requirements

22. Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA2117 v.4	20150408	Product data sheet	-	PCA2117 v.3
Modifications:	• Fixed typos			
PCA2117 v.3	20140919	Product data sheet	-	PCA2117 v.2
PCA2117 v.2	20131113	Product data sheet	-	PCA2117 v.1
PCA2117 v.1	20130930	Product data sheet	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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