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Kind regards,

Team Nexperia

DATA SHEET

74F373
Octal transparent latch (3-State)
74F374
Octal D flip-flop (3-State)

Product data
Supersedes data of 1994 Dec 05

2002 Nov 20

Philips
Semiconductors

PHILIPS

Latch/flip-flop 74F373/74F374

74F373 Octal transparent latch (3-State)
74F374 Octal D-type flip-flop (3-State)

FEATURES

- 8-bit transparent latch — 74F373
- 8-bit positive edge triggered register — 74F374
- 3-State outputs glitch free during power-up and power-down
- Common 3-State output register
- Independent register and 3-State buffer operation
- SSOP Type II Package

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is HIGH. The latch remains transparent to the data input while E is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, latched or transparent data appears at the output.

When $\overline{OE}$ is HIGH, the outputs are in high impedance “off” state, which means they will neither drive nor load the bus.

The 74F374 is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of the D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop’s Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active-LOW output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in high impedance “off” state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5 ns	35 mA

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F374	165 MHz	55 mA

ORDERING INFORMATION

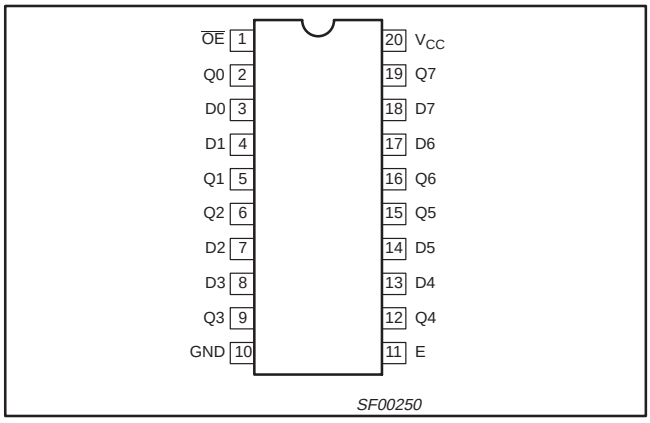
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5 V ±10%, T_{amb} = 0 °C to +70 °C	PKG DWG #
20-pin plastic DIP	N74F373N, N74F374N	SOT146-1
20-pin plastic SOL	N74F373D, N74F374D	SOT163-1
20-pin plastic SSOP type II	N74F373DB, N74F374DB	SOT339-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

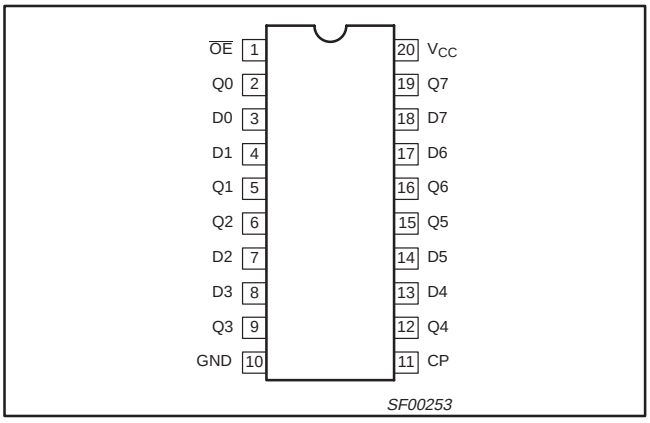
PINS	DESCRIPTION	74F (U.L.) HIGH / LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0 / 1.0	20 µA / 0.6 mA
E (74F373)	Enable input (active-HIGH)	1.0 / 1.0	20 µA / 0.6 mA
$\overline{OE}$	Output enable inputs (active-LOW)	1.0 / 1.0	20 µA / 0.6 mA
CP (74F374)	Clock pulse input (active rising edge)	1.0 / 1.0	20 µA / 0.6 mA
Q0 - Q7	3-State outputs	150 / 40	3.0 mA / 24 mA

NOTE: One (1.0) FAST unit load is defined as: 20 µA in the HIGH state and 0.6 mA in the LOW state.

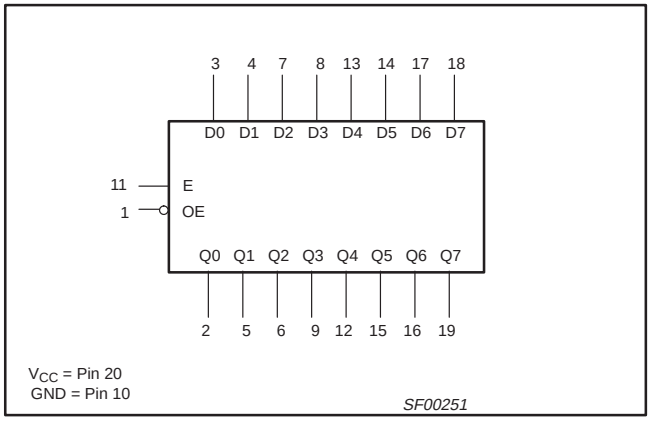
PIN CONFIGURATION – 74F373



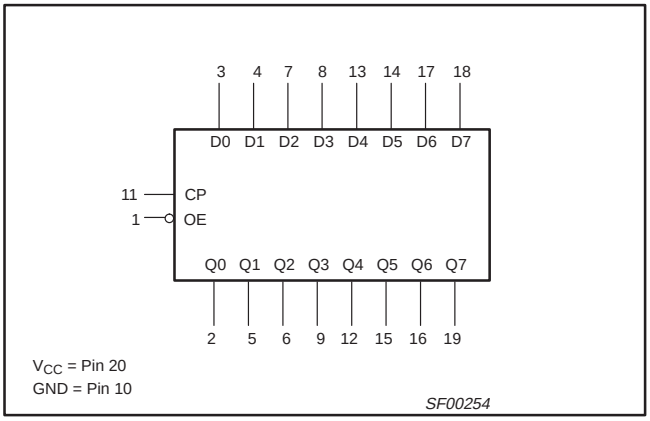
PIN CONFIGURATION – 74F374



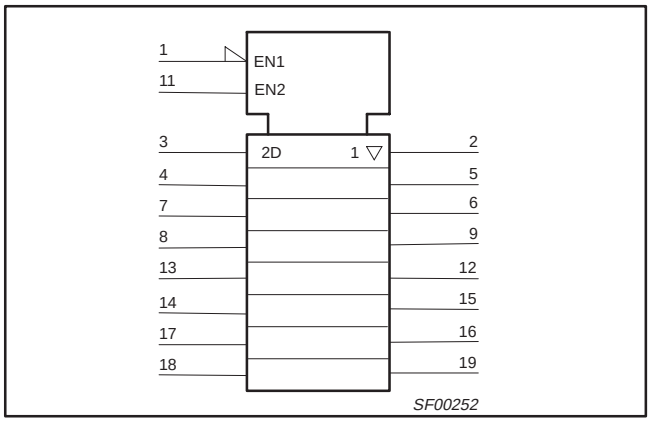
LOGIC SYMBOL – 74F373



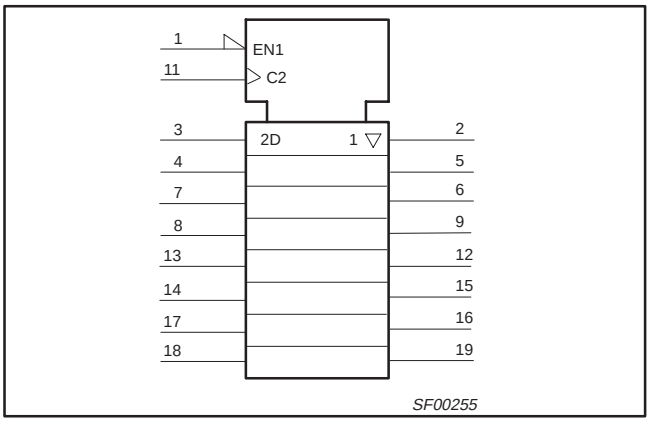
IEC/IEE SYMBOL – 74F374



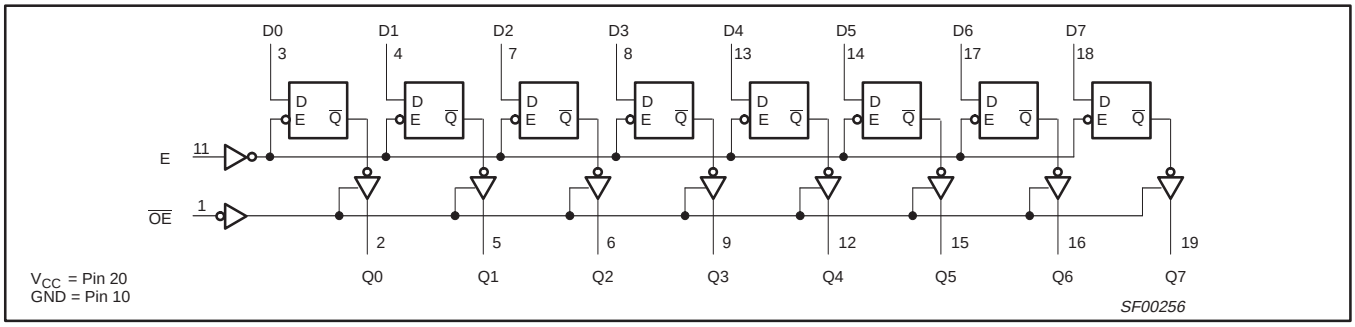
IEC/IEEE SYMBOL – 74F373



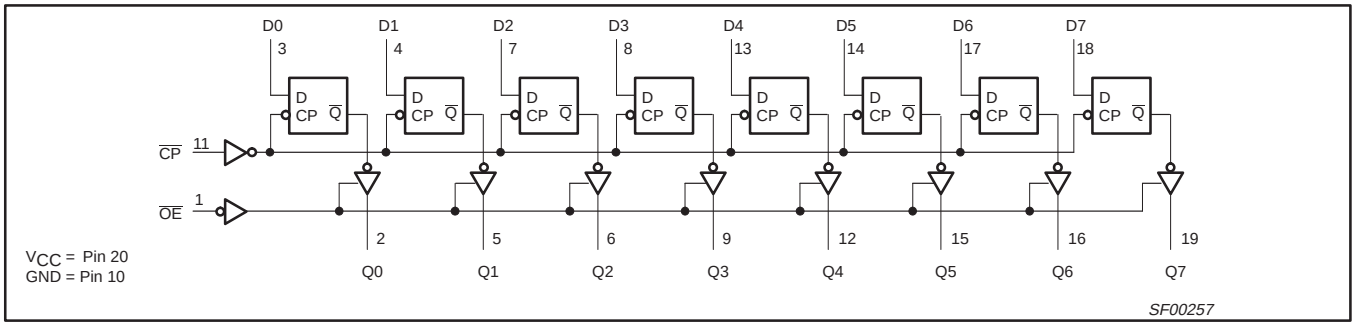
IEC/IEEE SYMBOL – 74F374



LOGIC DIAGRAM FOR 74F373



LOGIC DIAGRAM FOR 74F374



FUNCTION TABLE FOR 74F373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:

H = High-voltage level
h = HIGH state must be present one set-up time before the HIGH-to-LOW enable transition
L = Low-voltage level
l = LOW state must be present one set-up time before the HIGH-to-LOW enable transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = HIGH-to-LOW enable transition

FUNCTION TABLE FOR 74F374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↥	X	NC	NC	Hold
H	↥	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

NOTES:
H = High-voltage level
h = HIGH state must be present one set-up time before the LOW-to-HIGH clock transition
L = Low-voltage level
l = LOW state must be present one set-up time before the LOW-to-HIGH clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH clock transition
↥ = Not LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	–	–	V
V_{IL}	LOW-level input voltage	–	–	0.8	V
I_{Ik}	Input clamp current	–	–	–18	mA
I_{OH}	HIGH-level output current	–	–	–3	mA
I_{OL}	LOW-level output current	–	–	24	mA
T_{amb}	Operating free air temperature range	0	–	+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0 V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V				–0.6	mA
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V				50	µA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.5 V				–50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	74F373	V_{CC} = MAX			35	60	mA
		74F374				57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

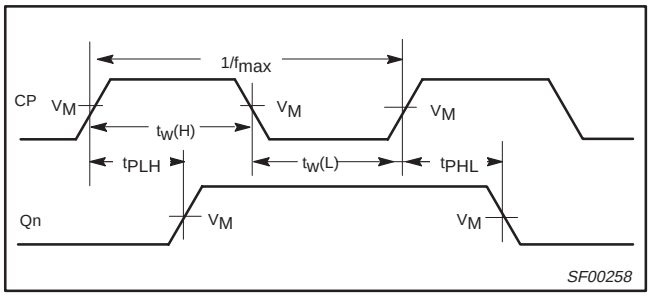
SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_{amb} = +25 °C, V_{CC} = +5.0 V, C_L = 50 pF; R_L = 500 Ω MIN	TYP	MAX	LIMITS T_{amb} = 0 °C to +70 °C, V_{CC} = +5.0 V ± 10%, C_L = 50 pF; R_L = 500 Ω MIN	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f_{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH or LOW level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

AC SET-UP REQUIREMENTS

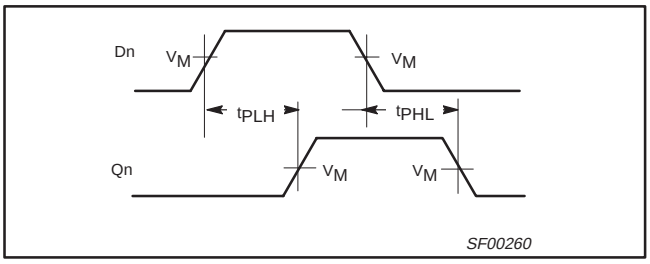
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w (H)	E Pulse width, HIGH		Waveform 1	3.5			4.0		ns
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW level Dn to CP		Waveform 5	0 0			0 0		ns
t_w (H) t_w (L)	CP Pulse width, HIGH or LOW		Waveform 5	3.5 4.0			3.5 4.0		ns

AC WAVEFORMS

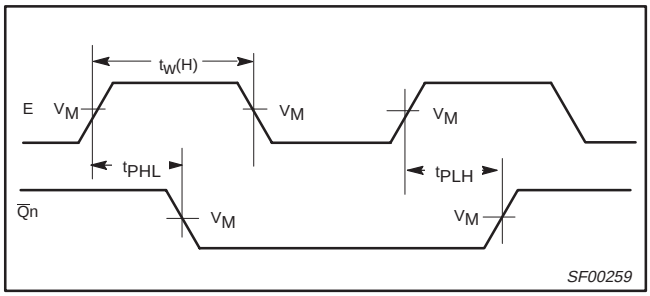
For all waveforms, V_M = 1.5 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



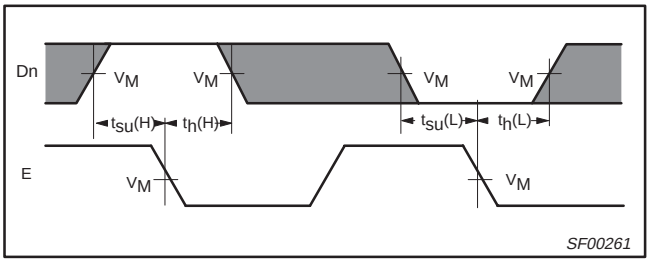
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 3. Propagation delay for data to output



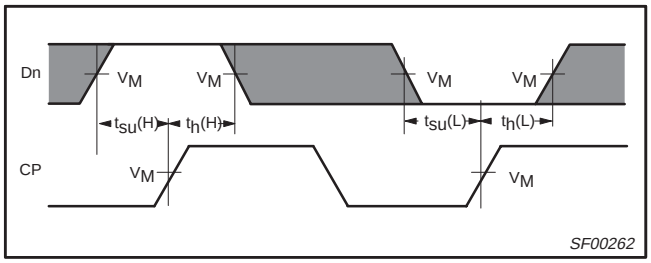
Waveform 2. Propagation delay for enable to output and enable pulse width



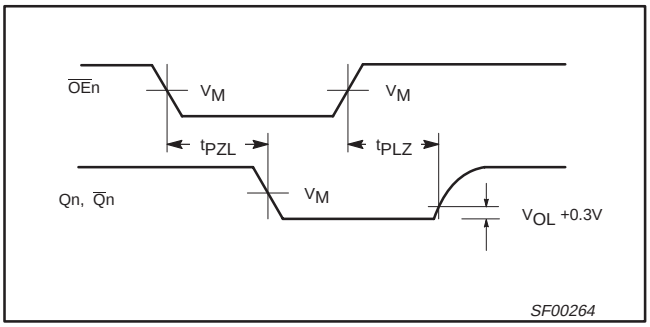
Waveform 4. Data set-up time and hold times

AC WAVEFORMS *(continued)*

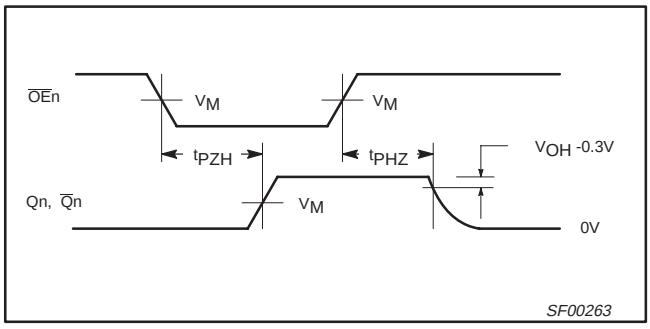
For all waveforms, V_M = 1.5 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 5. Data set-up time and hold times



Waveform 7. 3-State output enable time to LOW level and output disable time from LOW level

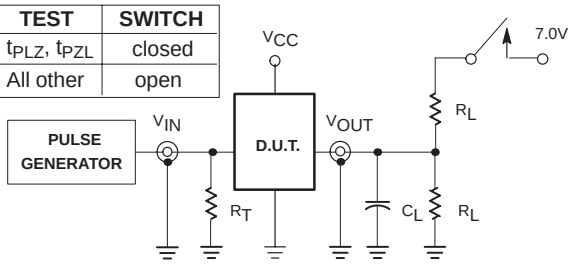


Waveform 6. 3-State output enable time to HIGH level and output disable time from HIGH level

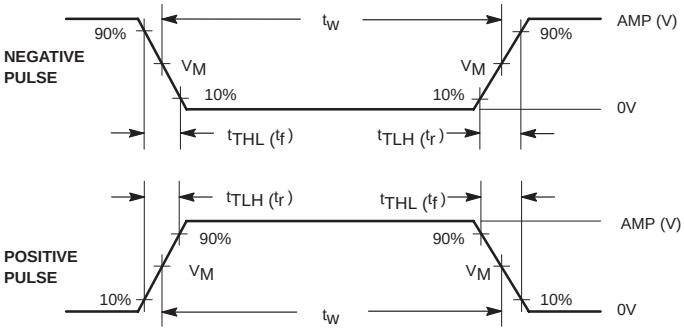
TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test circuit for 3-state outputs



Input pulse definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

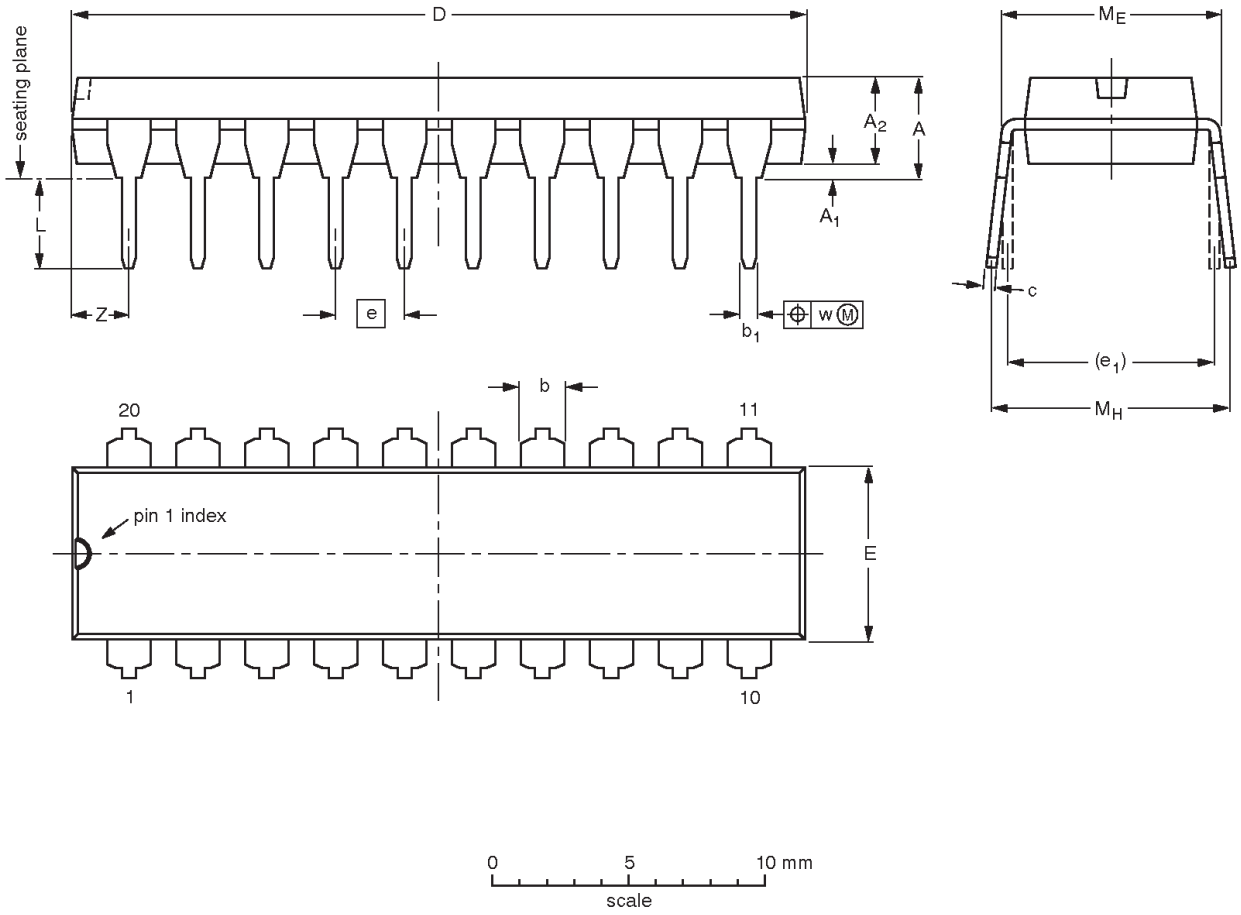
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00265

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

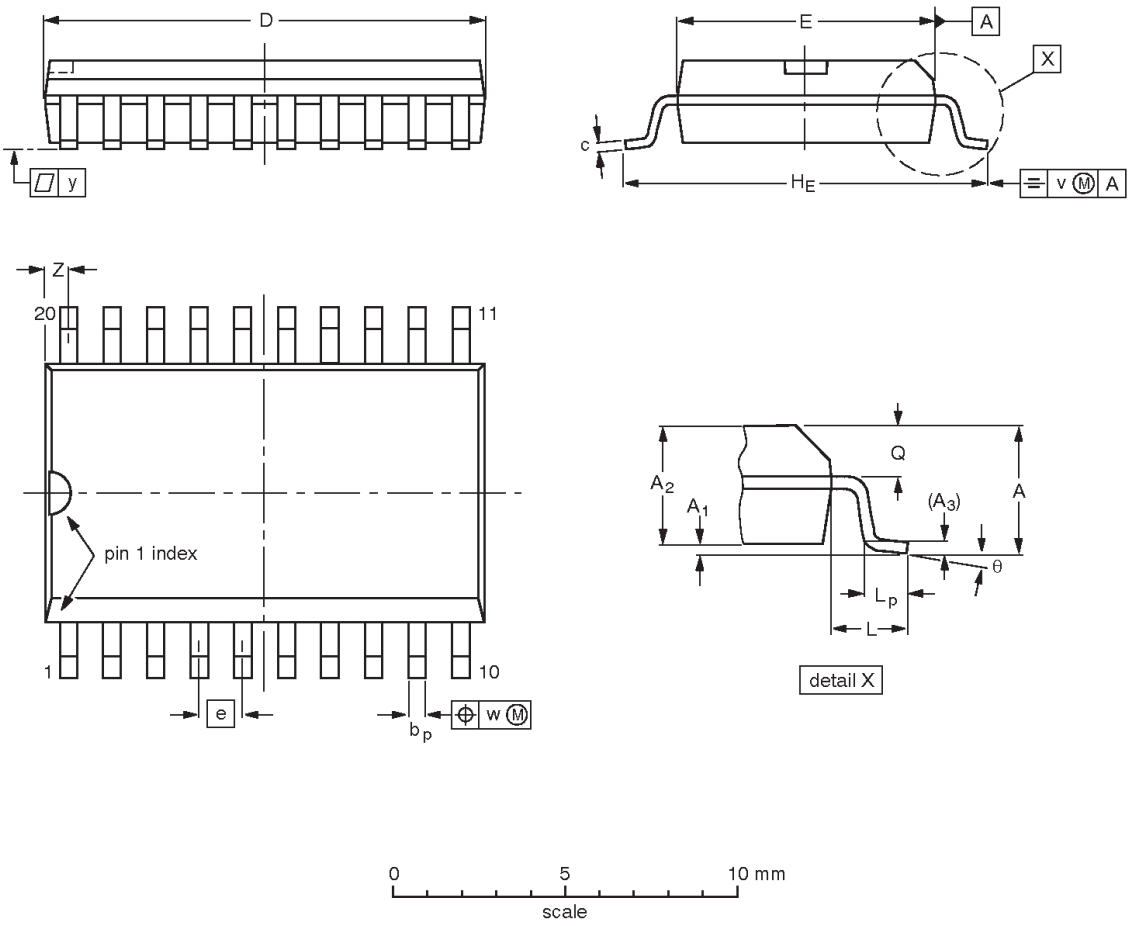
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

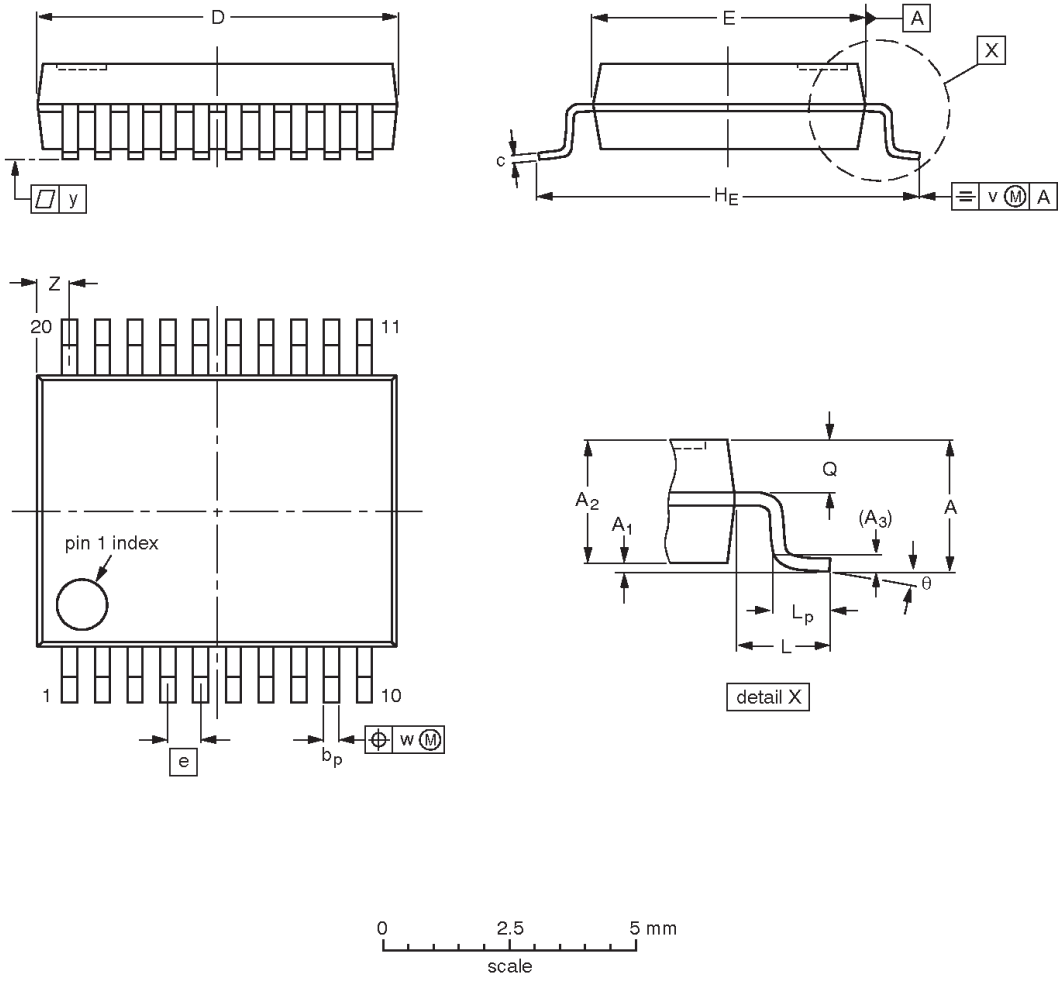
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150				~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20021120	**Product data; third version (9397 750 10758). Supersedes 74F373_374_2 dated 1994 Dec 05 (9397 750 05119).** Engineering Change Notice 853–0369 29206 (date: 20021115). **Modifications:** ● Corrected ordering information table (from 'N74374DB' to '74F374DB'). ● Add SSOP20 (SOT339-1) package outline drawing.
_2	19941205	**Product data; second version (9397 750 05119).** Engineering Change Notice 853–0369 14383 (date: 19941205).

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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