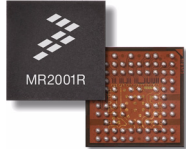


76-77 GHz RF receiver front-end for W-band radar applications

The MR2001 is a scalable three package solution for automotive radar modules. The chipset consists of a four channel VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver. The MR2001R is a high performance, highly integrated, three-channel, receiver (RX) ideally suited for automotive radar applications. In conjunction with the MR2001V, a four-channel voltage controlled oscillator, and an MR2001T, a two-channel transmitter, it provides a scalable three package solution for automotive radar modules.

Features

- 76 GHz to 77 GHz RX input
- Supply voltage 3.3 V
- Supply current typ. 240 mA
- Power dissipation typ. 0.8 W
- Conversion gain 23 dB to 60 dB
- SSB noise figure typical 14 dB
- Saturation detectors
- Tri-state IF outputs

| |
|---|
| MR2001R |
| ADVANCED DRIVER ASSISTANCE SYSTEM |
|  |
| VK SUFFIX (PB-FREE) 98ASA00540D 6.0 X 6.0 X 0.95 RCPBGA |

Applications

- Automotive proximity radar
- LRR, MRR and SRR
- ADAS
- Industrial surveillance and security systems

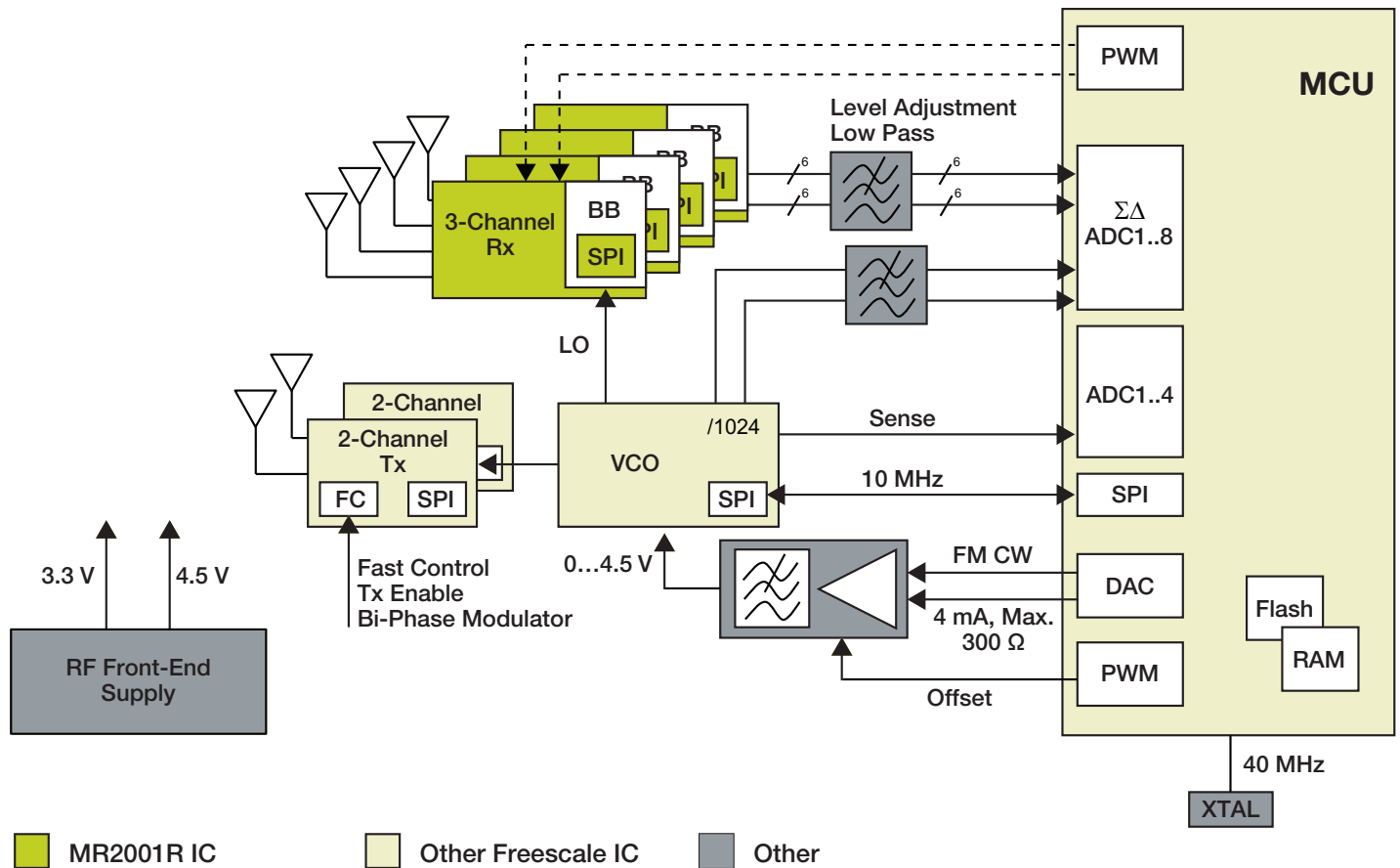


Figure 1. MR2001R simplified application diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

Table 1. Orderable part variations

| Part number | Temperature (temp) | Package | Notes |
|---------------|--------------------|---|-------|
| MC33MR2001RVK | -40 °C to 125 °C | 6.0 x 6.0 mm RCP (10 x 11 array) 0.5 mm pitch | (1) |

Notes

- To order parts in Tape & Reel, add R2 to the suffix of the part number.

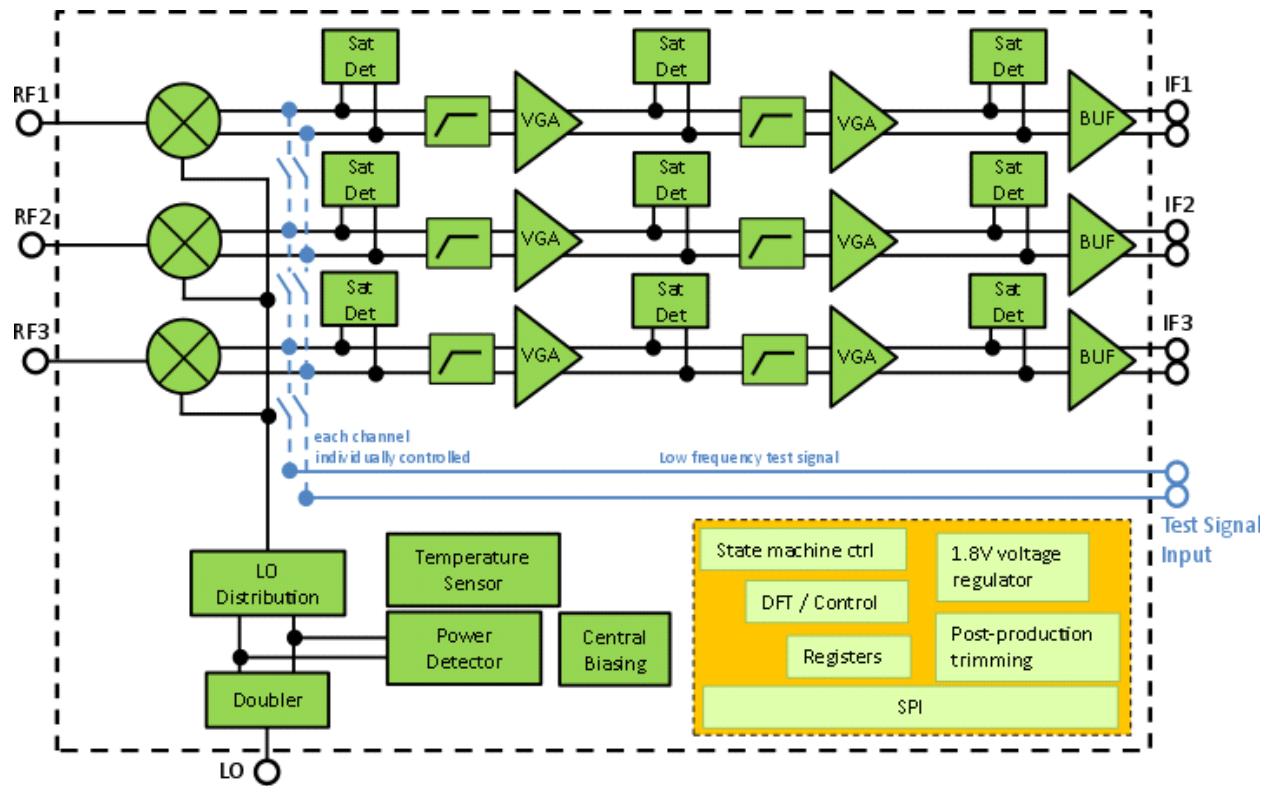


Figure 2. MR2001R three-channel receiver block diagram

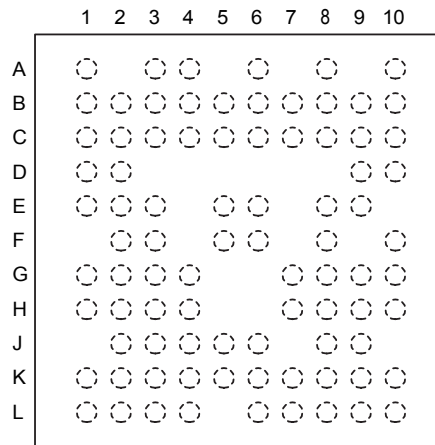


Figure 3. MR2001R pinout (ball) diagram

Table 2. MR2001R pin definitions

| Ball location | Pin function |
|---|----------------------------------|
| A1, A10, D1, D2, E8, F5, F6, F8, G4, G7, G8, G9, G10, H4, H7, K7, L1, L2, L3, L7, L8, L9, L10 | DC Ground |
| A3 | SPI MOSI (master out, slave in) |
| A4 | Digital hard reset signal |
| A6 | Differential IF output channel 1 |
| A8 | Differential IF output channel 3 |
| B1 | SPI enable (chip enable) |
| B2 | SPI serial clock |
| B3 | SPI MISO (master in, slave out) |
| B4 | Digital scan test |
| B5 | Differential IF output channel 2 |
| B6 | Differential IF output channel 2 |
| B7 | Differential IF output channel 1 |
| B8 | Differential IF output channel 3 |

| Ball location | Pin function |
|--|---|
| C1, C2 | 3.3 V Power Supply |
| C6 | 3.3 V Power Supply |
| C8 | 3.3 V Power Supply |
| D9 | Sensor output (temperature and power peak detector) |
| D10 | Bandgap reference resistor (positive temperature slope) |
| E1, E2, E3, F3, G1, G2, G3, H1, H2, H3, H8, H9, H10, J3, J4, J5, J6, J8, K1, K2, K3, K4, K6, K8, K9, K10, L4, L6 | RF Ground |
| E5 | Chip key Bit [1] |
| E6 | Chip key bit [0] |
| E9 | Saturation detector output |
| F2 | 77 GHz RX input channel 2 |
| F10 | Bandgap reference resistor (negative temperature slope) |
| J2 | 77 GHz RX input channel 1 |
| J9 | 77 GHz RX input channel 3 |
| K5 | LO input |

Table 3. Key parameters

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V \pm 5.0%, unless otherwise noted.

| Symbol | Parameter | Typ. | Unit | Notes |
|-----------|---|------|------|-------|
| V_{CC} | Supply Voltage, Nominal supply \pm 5% variation | 3.3 | V | |
| I_{CC} | Supply Current (all channels on) | 242 | mA | |
| I_{CC0} | Supply Current S0 (chip de-activated) | 19 | mA | |
| P_{ON} | Power Consumption (on) | 0.8 | W | |

BB parameters

| | | | | |
|----------|---|-----|-----------|--|
| f_{HP} | High-pass (HP) Filter Edge Frequency (-6.0 dB) | 300 | kHz | |
| s_{HP} | Slope Below f_{HP} | 40 | dB/decade | |
| LP_order | Low Pass Filter (LP) Order - center freq. at approx. 8.0 MHz - information only | 1.0 | - | |

Conversion gain

| | | | | |
|-------------|--|------|----|--|
| CG_{MAX} | Max. Conversion Gain at f = 4.0 MHz - 22 dB 1st VGA, 16 dB 2nd VGA | 57 | dB | |
| CG_{MIN} | Min. Conversion Gain at f = 4.0 MHz - 10 dB 1st VGA, -2.0 dB 2nd VGA | 26.5 | dB | |
| CG_{STEP} | Conversion Gain Step-size (VGA settings) | 5.5 | dB | |

Control

| | | | | |
|-----------------|--|------|------|--|
| R_{SAT} | Overload Detected Output Load | 365 | W | |
| P_MIXER_SAT | Input Referred Saturation Detector Threshold at CG = min at f = 10 kHz | -3.0 | dBm | |
| V_{VGA1_SAT} | 1st VGA Stage Output Saturation Level (stage directly after mixer core) | 400 | mVpk | |
| V_{VGA2_SAT} | 2nd VGA Stage Output Saturation Level | 350 | mVpk | |

Table 4. Revision history

| Revision | Date | Description of changes |
|----------|--------|---|
| 1.0 | 6/2015 | <ul style="list-style-type: none"> Initial release |
| 2.0 | 9/2016 | <ul style="list-style-type: none"> Added revision history table Modified the target application lists Updated Figure 2 |

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