

Octal D-type flip-flop, inverting (3-State)

54ABT534

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +48mA/-24mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 54ABT534 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT534 device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the

Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation.

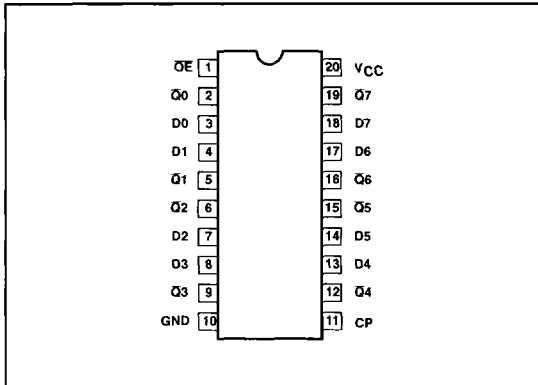
When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

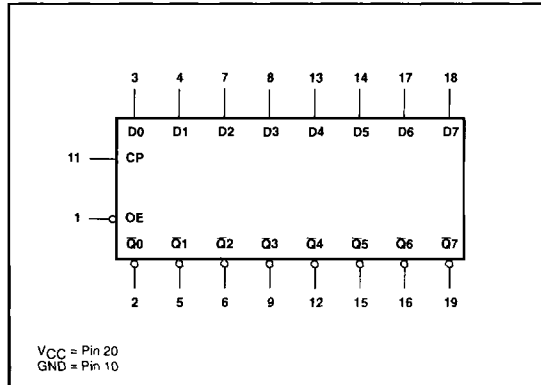
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54ABT534/BRA	GDIP1-T20
20-Pin Ceramic LLCC	54ABT534/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

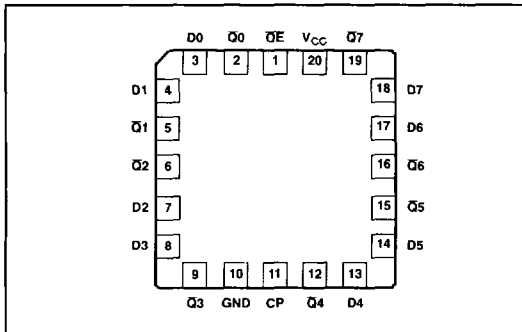
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



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PIN DESCRIPTION

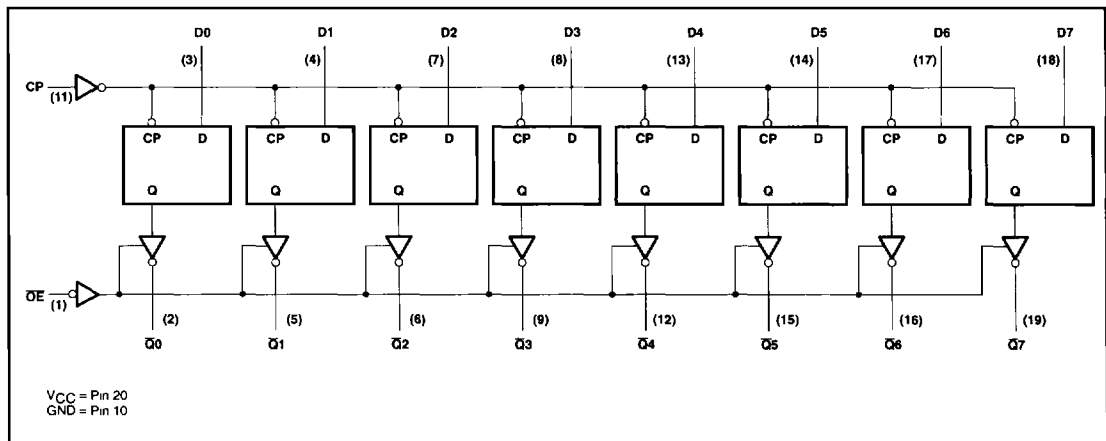
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	Output enable input (active Low)
3, 4, 7, 8, 13, 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q0} - \overline{Q7}$	Inverting 3-State outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS $\overline{Q0} - \overline{Q7}$	OPERATING MODE
\overline{OE}	CP	D _n			
L L	↑ ↑	l h	L H	H L	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X D _n	NC D _n	Z Z	Disable outputs

H = High voltage level
 h = High voltage level one setup time prior to the Low-to-High clock transition
 L = Low voltage level
 l = Low voltage level one setup time prior to the Low-to-High clock transition
 NC = No change
 X = Don't care
 Z = High impedance "off" state
 ↑ = Low-to-High clock transition
 ↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage range		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage range ²		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _O	DC output voltage range ²	Output in Off or High state	-0.5 to +5.5	V
I _O	DC output current	Output in Low state	96	mA
T _{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Input voltage		0.8	V
I _{OH}	High-level output current		-24	mA
I _{OL}	Low-level output current		48	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-55	+125	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = MAX, V_I = V_{IL} or V_{IH} unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			T _{amb} = -55 to +125°C		
			MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V, I _{IK} = -18mA		-1.2	V
V _{OH}	High-level output to voltage	V _{CC} = 4.5V; I _{OH} = -3mA	2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA	3.0		V
		V _{CC} = 4.5V; I _{OH} = -24mA	2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 48mA		0.55	V
I _I	Input leakage current	V _I = GND or 5.5V		±1.0	μA
I _{OZH} ⁸	3-State output High current	V _O = 2.7V, V _I = V _{IL} or 3.0V		10	μA
I _{OZL} ⁸	3-State output Low current	V _O = 0.5V, V _I = V _{IL} or 3.0V		-10	μA
I _O	Short-circuit output current ⁴	V _O = 2.5V, V _I = GND or V _{CC}	-50	-180	mA
I _{CCH}	Quiescent supply current	Outputs High, V _I = GND or V _{CC}		250	μA
I _{CCL}		Outputs Low, V _I = GND or V _{CC}		30	mA
I _{CCZ}		Outputs 3-State, V _I = GND or V _{CC}		250	μA
ΔI _{CC}	Additional supply current per input pin ⁵	One input at 3.4V, other inputs at V _{CC} or GND		1.5	mA
I _{OFF}	Power OFF leakage current	V _{CC} = 0.0V, V _I or V _O ≤ 4.5V TA = 25°C only	-100	100	μA
I _{CEx}	Output High leakage current	V _{CC} = 5.5V, V _O = 5.5V		50	μA

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AC ELECTRICAL CHARACTERISTICSGND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 5\text{V}$		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum Clock frequency	Waveform 1	125	175		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to \bar{Q}_n	Waveform 1	2.6 3.4	4.7 5.4	5.9 6.7	2.1 3.0	6.7 7.6	ns ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.0 2.6	2.9 4.5	4.2 5.8	0.9 2.2	5.3 6.8	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.4 2.3	5.3 4.5	6.6 5.8	2.4 1.3	7.5 6.7	ns ns

AC SETUP REQUIREMENTSGND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			MIN	TYP	MAX	MIN	MAX	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time ⁶ Dn to CP	Waveform 9	1.6 2.2			1.6 2.2		ns ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time ⁶ Dn to CP	Waveform 9	0.5 0.5			0.5 0.5		ns ns
$t_{\text{W}}(\text{H})$	CP pulse width ⁷ High or Low	Waveform 8	3.5 3.5			3.5 3.5		ns ns

NOTES:

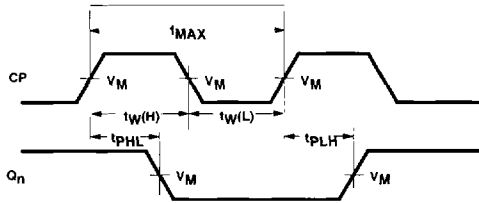
- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C .
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- t_{set} and t_{hold} limits that are less than 3.0ns are guaranteed, but are only tested to a 3.0ns limit due to tester limitations.
- t_{w} limits that are less than 6.0ns are guaranteed, but are only tested to a 6.0ns limit due to tester limitations.
- To accommodate ATE tester limitations, I_{OZ} tests are tested with $V_{\text{IH}} = 3.0\text{V}$, but 2.0V V_{IH} is guaranteed.

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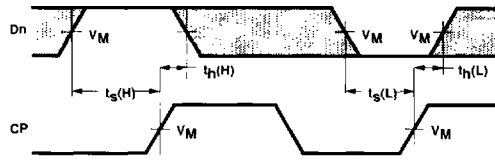
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AC WAVEFORMS

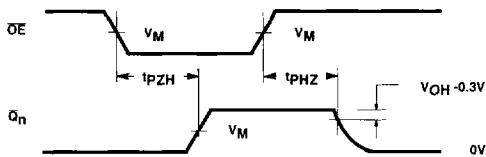
$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$



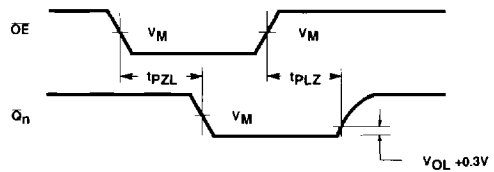
Waveform 8. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



Waveform 9. Data Setup and Hold Times



Waveform 10. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 11. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance

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TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

The test circuit shows a D.U.T. (Device Under Test) with input V_{IN} and output V_{OUT} . The input is connected to a PULSE GENERATOR through a termination resistor R_T . The output is connected to a load resistor R_L through a switch. A load capacitor C_L is also connected to the output. The circuit is powered by V_X and V_{CC} . A 7.0V source is connected to the output through the switch.

Input Pulse Definitions

The input pulse waveforms show a negative pulse (top) and a positive pulse (bottom). The negative pulse starts at 2.7V, falls to a minimum voltage V_M (0.3V), and then rises back to 2.7V. The positive pulse starts at 0.3V, rises to a maximum voltage V_M (2.7V), and then falls back to 0.3V. The pulse width is t_W . The propagation delay times are $t_{THL}(tf)$ and $t_{TLH}(tr)$. The voltage $V_M = 1.5V$.

INPUT PULSE REQUIREMENTS					
Family	Amplitude	Rep. Rate	t_W	t_R	t_F
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:
 R_L = Load Resistor; see AC Characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.