

# UM10757

## OM13257 temperature sensor daughter card

Rev. 1 — 31 October 2013

User manual

### Document information

| Info            | Content                                                                                                                                                                                                                                      |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Keywords</b> | Fm+ Development Kit, OM13320, Temperature Sensor, LM75, SE95, PCT2075                                                                                                                                                                        |
| <b>Abstract</b> | Installation guide and User Manual for the OM13257 Temperature Sensor Daughter Card that connects to OM13320 Fm+ Development Kit. This board permits easy and simple evaluation of most of the NXP temperature sensor portfolio of products. |



## Revision history

| Rev | Date     | Description     |
|-----|----------|-----------------|
| 1   | 20131031 | Initial release |

## Contact information

For more information, please Visit: <http://www.nxp.com>

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## 1. Introduction

The OM13257 Temperature Sensor Daughter Card connects directly to the OM13320 Fm+ Development kit and permits easy evaluation of most of NXP's Temperature Sensor portfolio of products.

[Table 1](#) lists the supported devices.

The OM13257 Temperature Sensor Daughter Card is shipped with no temperature sensor device soldered to the board. The user must purchase the device he is interested in evaluating in a TSSOP8 package (the ordering part number suffix should be 'DP' and the package designation should be SOT505-1). These leaded packages should be relatively easy to solder to the board with a low wattage, fine tipped soldering iron.

**Remark:** The pin 1 orientation is down and to the right when the text on the board readable. Usually, you would expect pin 1 to be up and to the left.

There are two additional package footprints for an XSON8U package (SOT996-2). This same footprint accepts an HWSON8 package (SOT1169-2) with the exposed center pad unconnected. This configuration is acceptable for the temperature sensor devices. There is also a WLCSP6 package footprint for the PCT2202 device. In all cases, the pin 1 orientation is down and to the left when the board text is readable.

**Table 1. Devices supported by OM13257 Temperature Sensor Daughter Card**

| Part Number | Package Number | Package Description |
|-------------|----------------|---------------------|
| LM75ADP     | SOT505-1       | TSSOP8              |
| LM75BDP     | SOT505-1       | TSSOP8              |
| SE95DP      | SOT505-1       | TSSOP8              |
| PCT2075DP   | SOT505-1       | TSSOP8              |
| LM75BGD     | SOT996-2       | XSON8               |
| LM75BTP     | SOT1069-2      | HWSON8              |
| PCT2075TP   | SOT1069-2      | HWSON8              |
| PCT2202UK   | WLCSP6         | —                   |

## 2. Features of the OM13257 Temperature Sensor Daughter Card

- Direct connection to OM13320 Fm+ Development kit
- Footprint for a TSSOP8 package, user solderable
- Flexible power supply configuration: 3.3 V or 5 V
- Jumper configuration of device I<sup>2</sup>C address
- LED indicators for power and  $\overline{\text{INT}}$
- Scope ground connection loop

### 3. Board jumper setup

#### 3.1 Power Supply

The power supply selection for the OM13257 is very flexible and allows for detailed analysis and evaluation of all the NXP temperature sensor devices. JP1 labeled PWR selects between 5 V supplied from the tester connector CN4 (jumper between pin 2 and 3) and the Fm+ board connector CN5 (jumper between pin 1 and 2). If 3.3 V is desired, no jumper is required.

JP2 (labeled VDD) selects between 5 V and 3.3 V for the main power supply on pin 8 of the device under test. Add a jumper between pins 2 & 3 for 3.3 V supplied by the Fm+ board or 1 & 2 for 5 V selected by JP1.

See the schematic section at the end of this document for more details.

#### 3.2 I<sup>2</sup>C Address

The I<sup>2</sup>C address of the slave temperature sensor device is selected via JP10, JP11 and JP12 connected to pin 5, 6, and 7 of the device under test respectively. Pin 1 of the jumpers is connected to 0 V, while pin 3 is connected to VDD selected above. Consult the datasheet for the I<sup>2</sup>C addresses corresponding to the logic levels on each pin.

See the schematic section at the end of this document for more details.

#### 3.3 SCL and SDA source

There are two I<sup>2</sup>C busses implemented on the Fm+ board and JP3 and JP4 select either Bus 1 or Bus 2 as a source to the device under test. Jumper between pins 1 and 2 to select Bus 2 as a source and jumper between pins 2 and 3 to select Bus 1.

**Remark:** SCL and SDA from CN4 Tester Connector are always connected to the device under test. If two masters are used, there may be contention.

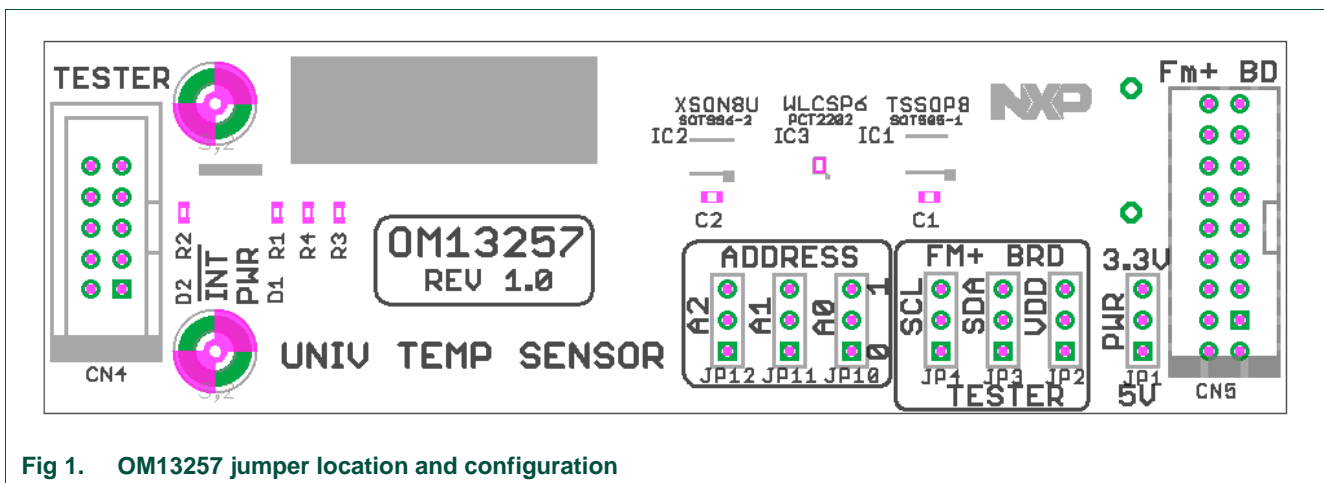


Fig 1. OM13257 jumper location and configuration

## 4. Connector pinouts

### 4.1 CN5 Fm+ Development Board connector

The OM13257 can connect directly to the OM13320 Fm+ Development kit via CN2. This connector provides power, I<sup>2</sup>C signals and other ancillary signals.

**Remark:** The connector on the Fm+ board is a male, shrouded 14-pin type, while the connector on the GPIO board is female, 18-pin. The reason lies with the shroud around the 14-pin connector. To ensure correct mating of the female with the male, two pin positions on both of the female sides are unused.

**Table 2. CN5 Fm+ Board connector pinout**

| CN2 Pin Number | Function | Board Connection                  |
|----------------|----------|-----------------------------------|
| 1              | —        | No connect                        |
| 2              | —        | No connect                        |
| 3              | SCL      | SCL Bus 1 to JP4 pin 3            |
| 4              | SDA2     | SDA Bus 2 JP3 pin 1               |
| 5              | INT      | Interrupt to INT LED and U1 pin 3 |
| 6              | RESET    |                                   |
| 7              | +5 V     | JP1 pin 1                         |
| 8              | +3.3 V   | JP2 pin 3                         |
| 9              | GND      |                                   |
| 10             | GND      |                                   |
| 11             | +3.3 V   | JP2 pin 3                         |
| 12             | +5 V     | JP1 pin 1                         |
| 13             | RESET    |                                   |
| 14             | INT      | Interrupt to INT LED and U1 pin 3 |
| 15             | SDA      | SDA Bus 1 JP3 pin 3               |
| 16             | SCL2     | SCL Bus 2 JP4 pin 1               |
| 17             | —        | No connect                        |
| 18             | —        | No connect                        |

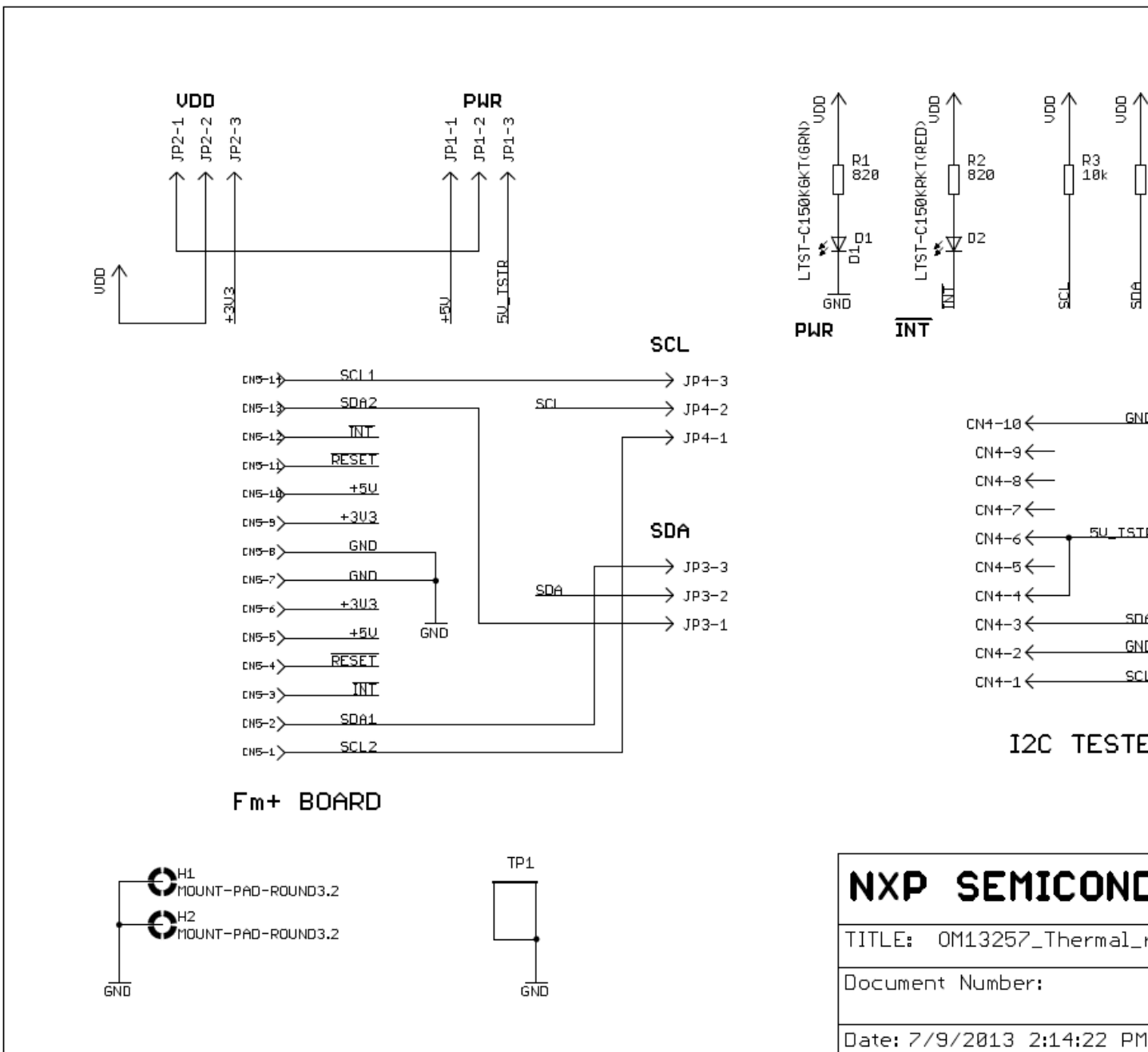
### 4.2 CN4 Tester connector

Generation, inspection and logging of I<sup>2</sup>C-bus data is easily achieved with third-party development tools from Total Phase (<http://nxp.com/redirect/totalphase.com>). There are two tools called Aardvark and Beagle that direct connect to this board through CN4.

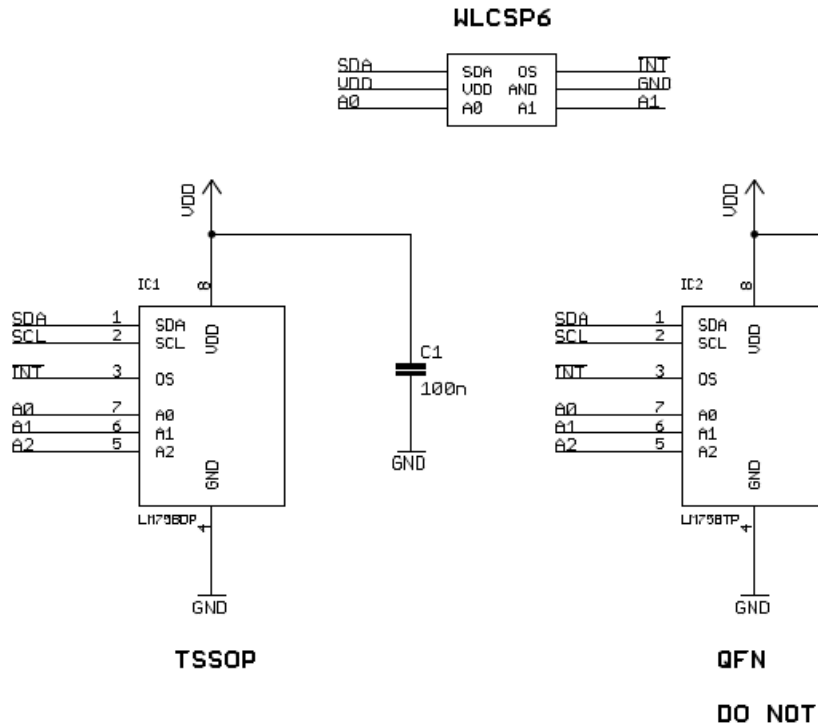
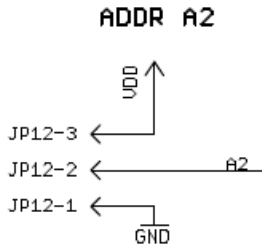
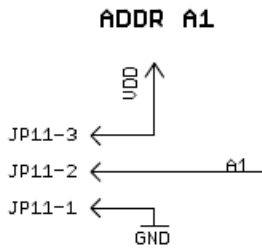
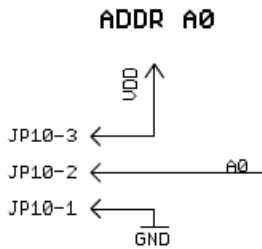
**Remark:** Since SDA and SCL are both connected to the device under test, the Aardvark and the Fm+ Development board cannot be used simultaneously. The Beagle, a bus sniffer, does not have any issues.

**Table 3. CN5 Tester connector pinout**

| CN4 Pin Number | Function | Board Connection |
|----------------|----------|------------------|
| 1              | SCL      | U1 pin 2         |
| 2              | Ground   |                  |
| 3              | SDA      | U1 pin 1         |
| 4              | +5 V     | JP1 pin 3        |
| 5              | +5 V     | JP1 pin 3        |
| 6              | +5 V     | JP1 pin 3        |
| 7              | —        |                  |
| 8              | —        |                  |
| 9              | —        |                  |
| 10             | Ground   |                  |



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| DEVICE TYPE | BASE ADDRESS |
|-------------|--------------|
| LM75B       | 0x90H        |
| PTC1075     | 0x90H/0xD0H  |
| PTC2075     | 0x90H/0xD0H  |
| SE95        | 0x90H        |

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**I<sup>2</sup>C-bus** — Logo is a trademark of NXP B.V.

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