NVT4556

SIM card interface level translator with I²C-bus control and LDO

Rev. 1.1 — 25 August 2015 **Product data sheet**

1. General description

The NVT4556 device is built for interfacing a SIM card with a single low-voltage host-side interface. The NVT4556 contains an LDO that can deliver two different voltages, 1.8 V or 3 V, from a typical mobile phone battery voltage, and three level translators to convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller.

The NVT4556 V_{CC} pin provides power to the host side I/Os and doubles as an enable pin, for this reason it can be connected to a GPIO that matches the host side voltage. The total current draw from the V_{CC} pin is only 100 μA maximum. The NVT4556 also uses the I²C-bus interface to enable normal operation and to select either 1.8 V or 3 V for the SIM card power supply. The NVT4556 can also disable the LDO functionality while maintaining the level translator paths so that the user can use a system-controlled regulator to power the SIM card power supply. The NVT4556 can enable users to provide second and third SIM card functionality with a low-voltage one host SIM port, at the same time reducing the number of GPIOs used in the system. The NVT4556 is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

The NVT4556 is available in a 12-pin WLCSP package and has three factory programmed slave address options.

2. Features and benefits

- Support SIM card supply voltages 1.8 V and 3 V
- Input voltage range to LDO: 2.5 V to 5.25 V
- Host microcontroller operating voltage range: 1.55 V to 3.6 V
- V_{CC} input pin provides both host supply voltage and logic level hardware enable/disable pin: source through Host GPIO (I_{CC} <100 μA)
- RST_HOST/EN pin can be programmed as a reset pin or as a device enable/disable pin
- Level translation of I/O, RSTn and CLKn between SIM card and host-side interface with capacitive isolation
- I²C-bus interface for device enable and LDO voltage selection
- Low current shutdown mode < 3 μA
- Supports clock speed beyond 5 MHz clock
- Supports CLK stop mode
- Integrated EMI filters
- Incorporates ISO-7816-3 shutdown feature for the SIM card signals
- ETSI, IMT2000 and ISO-7816 compliant
- ±8 kV IEC61000-4-2 ESD protected on all SIM card contact pins

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Available in 12-pin WLCSP package (1.205 mm × 1.605 mm × 0.412 mm, 0.4 mm pitch)

3. Applications

- NVT4556 can be used with a range of SIM card attached devices including:
  - Mobile and personal phones
  - Wireless modems
  - SIM card terminals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NVT4556AUK	556A	WLCSP12	wafer level chip-size package; 12 balls; body 1.205 × 1.605 × 0.412 mm (Backside coating included)	NVT4556AUK
NVT4556BUK	556B	WLCSP12	wafer level chip-size package; 12 balls; body 1.205 × 1.605 × 0.412 mm (Backside coating included)	NVT4556BUK

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature	Slave address
NVT4556AUK	NVT4556AUKZ	WLCSP12	Reel 7” Q1/T1 *Special mark chips dry pack	3000	T_{amb} = −40 °C to +85 °C	1100 000xb
NVT4556BUK	NVT4556BUKZ	WLCSP12	Reel 7” Q1/T1 *Special mark chips dry pack	3000	T_{amb} = −40 °C to +85 °C	1100 001xb

5. Functional diagram

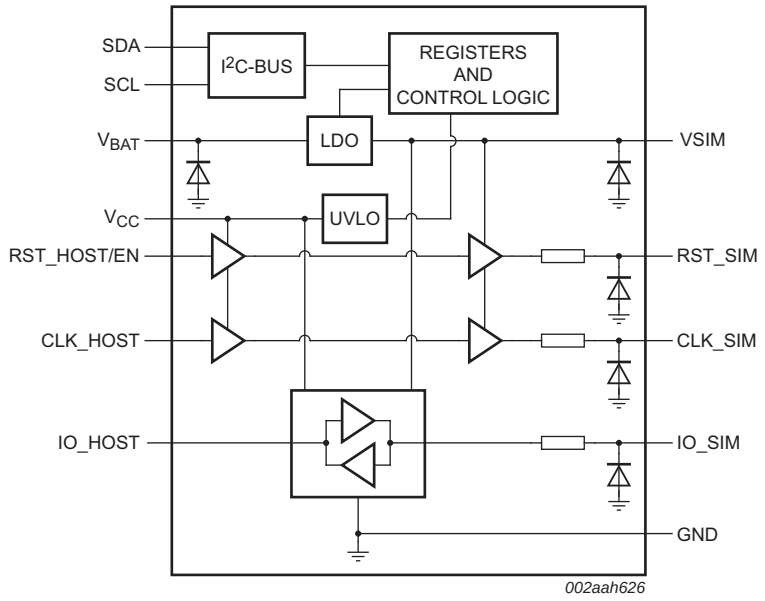


Fig 1. Functional diagram

6. Pinning information

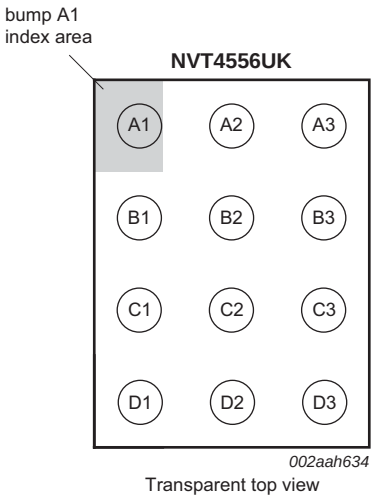


Fig 2. Bump configuration for WLCSP12

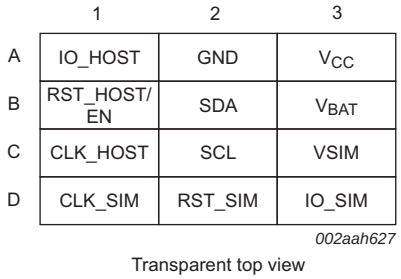


Fig 3. Bump mapping for WLCPS12

6.1 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
IO_HOST	A1	I/O	Host controller bidirectional data input/output. This output must be on an open-drain configuration.
GND	A2	ground	Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications.
V_{CC}	A3	power	Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST/EN, IO_HOST). When V_{CC} is below the UVLO threshold, the VSIM supply is disabled. This pin should be bypassed with a 100 nF ceramic capacitor close to the pin.
RST_HOST/EN	B1	I	Reset input from host controller or acts as a programmable logic-level enable/disable when bit 6 = 1.
SDA	B2	I/O	Digital input/output. I²C-bus serial bidirectional data line; open-drain.
V_{BAT}	B3	power	Battery voltage supply for internal LDO. This input voltage ranges from 2.5 V to 5.25 V. This pin should be bypassed with a 1.0 μF ceramic capacitor close to the pin.
CLK_HOST	C1	I	Clock input from host controller.
SCL	C2	I	Digital input. I²C-bus serial bidirectional clock line.
VSIM	C3	power	SIM card supply voltage from internal LDO. The voltage at this pin can be selected for either 1.8 V (CTRL = 0) or 3 V (CTRL = 1). This pin should be bypassed with a 4.7 μF ceramic capacitor close to the pin.
CLK_SIM	D1	O	Clock output pin for the SIM card.
RST_SIM	D2	O	Reset output pin for the SIM card.
IO_SIM	D3	I/O	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver.

7. Functional description

Refer to Figure 1 “Functional diagram”.

7.1 Shutdown sequence of NVT4556

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals. This shutdown sequence ensures that these channels are properly disabled and does not have any accidental corruption of data. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data.

When the V_{CC} falls below its UVLO threshold, a shutdown sequence is immediately initiated. The RST_SIM is first driven LOW after a short delay the CLK_SIM and IO_SIM are driven LOW followed by VSIM. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds.

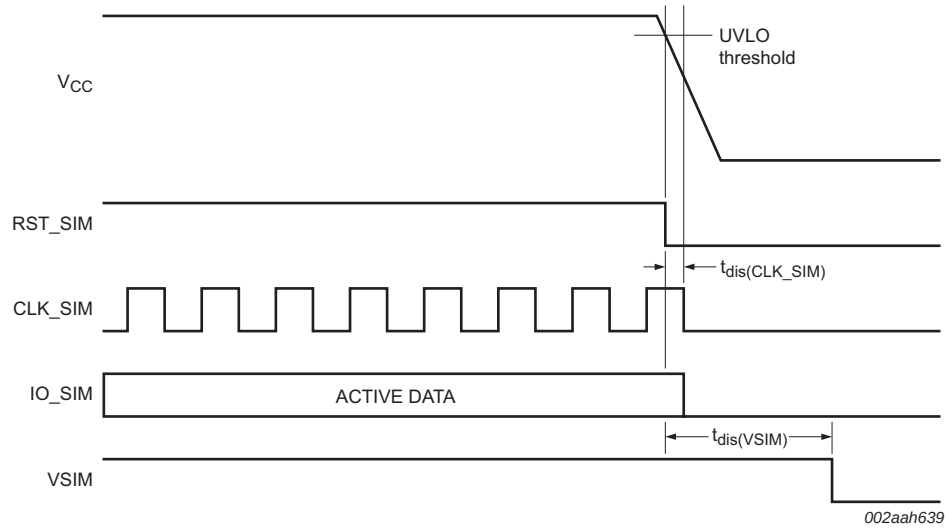


Fig 4. V_{CC} UVLO shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and VSIM of NVT4556 SIM card translator

The shutdown sequence can also be initiated by one of two events: by de-asserting the RST_HOST/EN pin if bit 6 (RST_HOST pin mode select bit) is set to 1, or by writing a 0 to bit 0 (Device enable bit) if bit 6 is set to 0. The shutdown sequence consists of first powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM, IO_SIM and VSIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that enable is written LOW before V_{BAT} and V_{CC} supplies go LOW to ensure that the shutdown sequence is properly initiated. The NVT4556 is enabled and disabled at the end of the I²C-bus write sequence, so a delay in the start of the I/O signals should account for time of this data sequence.

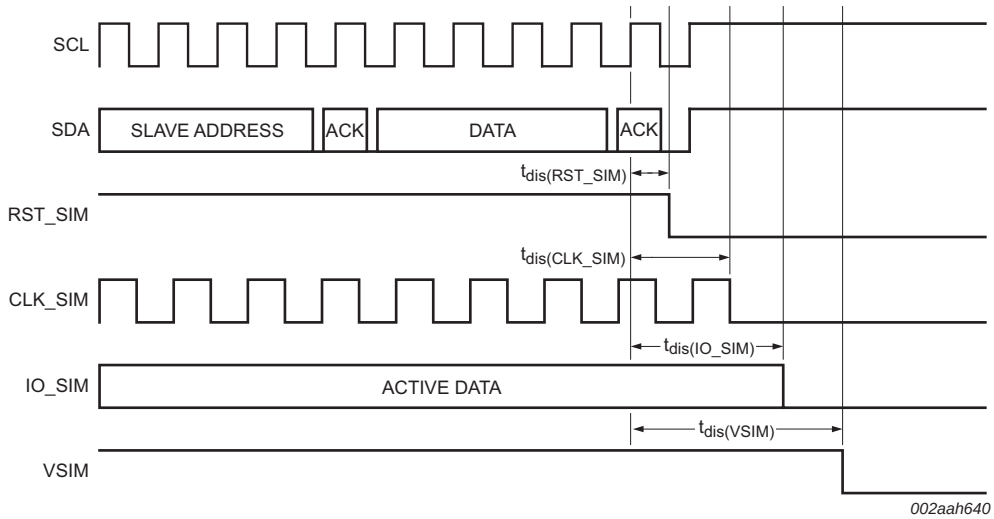


Fig 5. I²C-bus shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and VSIM of NVT4556 SIM card translator

7.2 RST_HOST/EN pin

The NVT4556 RST_HOST/EN pin can be programmed to accept the reset signal from the host to the SIM card or programmed to be an enable pin for the part. When the NVT4556 is programmed with bit 6 = 0, the RST_HOST/EN pin acts as a pass-through logic-level translator. A 0 on the host side appears as a 0 on the SIM side, and a 1 at the host side appears as a 1 on the SIM side. When the NVT4556 is programmed with bit 6 = 1, the RST_HOST/EN pin becomes a hardware enable/disable pin, so that the part can be enabled and disabled with a logic level input. In this case, the V_{CC} can be powered from the host supply and does not need to be pulled down to disable the part. Also, the reset signal for the SIM card must be written to bit 5. When a 1 is written to bit 5, a logic 1 is asserted onto RST_SIM. When a 0 is written to bit 5, a logic 0 is asserted on onto RST_SIM.

When bit 6 is set to 1 and RST_HOST/EN acts as an enable pin, bit 0 is ignored and only logic signals acting on RST_HOST/EN and the V_{CC} enable and disable the part. Bit 0 can be read to see the state of the RST_HOST/EN pin and bit 3 can be programmed to set the EN polarity to be active HIGH or active LOW.

7.3 Clock stop, latch I/O state

The NVT4556 can also support clock stop modes as well as an I/O stop so that two NVT4556 devices can operate from a single host SIM port. The NVT4556 can latch the state of the IO_HOST, CLK_HOST and RST_HOST/EN when bit 4 is toggled to 1. This asserts the logic value onto the IO_SIM, CLK_SIM and RST_SIM pins. This effectively initiates the clock stop mode and free the user to activate a secondary NVT4556 attached to the same host port. The NVT4556 devices must have different I²C-bus addresses so that they can be accessed independently of each other.

If bit 6 is programmed to 1 and the RST_HOST/EN pin is acting as an enable pin, then bit 5 must be used to latch the RST_SIM state through the I²C-bus.

7.4 Software reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as the following (see Figure 6):

1. A START command is sent by the I²C-bus master.
2. The reserved General Call I²C-bus address '0000 000' with the R/$\overline{W}$ bit set to 0 (write) is sent by the I²C-bus master.
3. The NVT4556 device(s) acknowledge(s) after seeing the General Call address '0000 0000' (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h. The NVT4556 acknowledges this value only. If the byte is not equal to 06h, the NVT4556 does not acknowledge it. If more than 1 byte of data is sent, the NVT4556 does not acknowledge any more.
5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: NVT4556 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

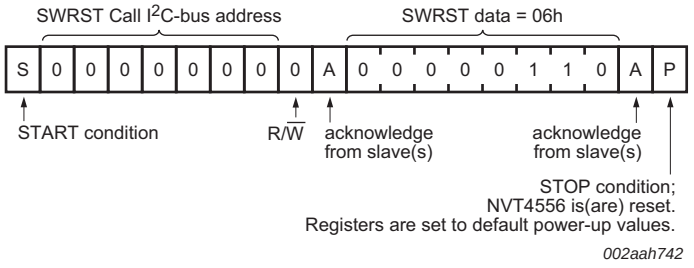


Fig 6. Software reset sequence

The I²C-bus master must interpret a non-acknowledge from the NVT4556 (at any time) as a 'Software Reset Abort'.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	SIM card side and VSIM pins; IEC 61000-4-2 [1]	-	±8	kV
		all other pins; IEC 61000-4-2 [1]	-	±2	kV
		all other pins; HBM [2]	-	±2	kV
		all other pins; CDM [3]	-	±500	V
V_{CC}	supply voltage		GND – 0.5	3.6	V
V_{BAT}	battery supply voltage		GND – 0.5	5.5	V
$V_{I(CLK\_HOST)}$	input voltage on pin CLK_HOST	input signal voltage, HOST side	GND – 0.5	V_{CC} + 0.5	V
$V_{I(RST\_HOST/EN)}$	input voltage on pin RST_HOST/EN	input signal voltage, HOST side	GND – 0.5	V_{CC} + 0.5	V
$V_{I(IO\_HOST)}$	input voltage on pin IO_HOST	input signal voltage, HOST side	GND – 0.5	V_{CC} + 0.5	V
$V_{I(CLK\_SIM)}$	input voltage on pin CLK_SIM	input signal voltage, SIM side	GND – 0.5	V_{VSIM} + 0.5	V
$V_{I(RST\_SIM)}$	input voltage on pin RST_SIM	input signal voltage, SIM side	GND – 0.5	V_{VSIM} + 0.5	V
$V_{I(IO\_SIM)}$	input voltage on pin IO_SIM	input signal voltage, SIM side	GND – 0.5	V_{VSIM} + 0.5	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C

[1] IEC 61000-4-2, level 4, contact discharge.

[2] Human Body Model (HBM) according to JESD22-A114.

[3] Charged-Device Model (CDM) according to JESD22-C101.

9. Characteristics

Table 5. Supplies

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.55 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{CC}	supply voltage		1.55	-	3.6	V
I_{CC}	supply current	operating mode; register 00h = 01h/03h; SDA = IO_HOST = V_{CC}; RST_HOST/EN = GND; f_{clk} = 1 MHz; $f_{clk(SCL)}$ = 400 kHz	-	40	100	µA
		operating mode; register 00h = 01h/03h; SDA = SCL = IO_HOST = V_{CC}; RST_HOST/EN = GND; f_{clk} = 1 MHz	-	10	20	µA
		operating mode; register 00h = 01h/03h; SCL = SDA = IO_HOST = V_{CC}; CLK_HOST = RST_HOST/EN = GND	-	10	20	µA
		standby mode; register 00h = 00h; SDA = SCL = IO_HOST = V_{CC}; CLK_HOST = RST_HOST/EN = GND; V_{CC} = 1.8 V	-	5	10	µA
		shut-down mode; register 00h = 00h; V_{CC} = 0 V	-	-	1	µA
V_{BAT}	battery supply voltage		2.5	-	5.25	V
I_{BAT}	battery supply current	operating mode; register 00h = 01h/03h; IO_HOST = V_{CC}; CLK_HOST = RST_HOST/EN = GND	-	30	40	µA
		shutdown mode; register 00h = 00h	-	2	3	µA
$V_{th(UVLO)}$	undervoltage lockout threshold voltage	V_{CC} rising; V_{BAT} = 3.6 V	1.2	-	1.5	V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage		-	100	-	mV

[1] Typical values measured at 25 °C. V_{CC} = 1.8 V; V_{BAT} = 3.6 V; V_{VSIM} (VSIM pin) = 1.8 V.

Table 6. Static characteristics

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.55 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I²C-bus						
$f_{clk(SCL)}$	SCL clock frequency		-	-	400	kHz
V_{IH}	HIGH-level input voltage	pins SCL, SDA	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	pins SCL, SDA	-	-	0.3 × V_{CC}	V
$I_{OL(sink)(SDA)}$	LOW-level output sink current on pin SDA	V_{OL} = 0.4 V	-	3	-	mA

Table 6. Static characteristics *...continued*

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.55 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
LDO						
V_{VSIM}	voltage on pin VSIM	VSIM pin; 00h = 03h; 3.2 V ≤ V_{BAT} ≤ 5.25 V; 0 mA ≤ I_{SIM} ≤ 50 mA	2.85	3.0	3.15	V
		VSIM pin; 00h = 01h; 2.5 V ≤ V_{BAT} ≤ 5.25 V; 0 mA ≤ I_{SIM} ≤ 50 mA	1.7	1.8	1.9	V
V_{do}	dropout voltage	I_O = 50 mA; V_{BAT} = 2.90 V	-	100	150	mV
I_{sc}	short-circuit current	VSIM shorted to GND	90	135	170	mA
$t_{startup}$	start-up time	V_{VSIM} = 1.8 V or 3 V; I_O = 50 mA; C_o = 1 µF	-	-	400	µs
$T_{j(sd)}$	shutdown junction temperature		-	160	-	°C
$T_{sd(hys)}$	hysteresis of shutdown temperature		-	20	-	°C
R_{pd}	pull-down resistance	VSIM discharge; 00h = 00h; V_{BAT} = 3.6 V; V_{CC} = 1.55 V	-	100	-	Ω
PSRR	power supply rejection ratio	V_{BAT} = 3.6 V; I_{SIM} = 20 mA; V_{VSIM} = 1.8 V or 3 V				
		f = 1 kHz	-	60	-	dB
		f = 10 kHz	-	50	-	dB
Level shifter						
V_{IH}	HIGH-level input voltage	IO_HOST, RST_HOST/EN, CLK_HOST				
		1.55 V ≤ V_{CC} < 3.6 V [2]	0.7 × V_{CC}	-	V_{CC} + 0.2	V
		IO_SIM [2]	0.7 × V_{VSIM}	-	V_{VSIM} + 0.2	V
V_{IL}	LOW-level input voltage	IO_HOST, RST_HOST/EN, CLK_HOST [2]	−0.15	-	0.15 × V_{CC}	V
		IO_SIM [2]	−0.3	-	0.15 × V_{VSIM}	V
R_{PU}	pull-up resistance	IO_SIM connected to VSIM [3]	4	6	8	kΩ
		IO_HOST connected to V_{CC} [3]	3.5	5	6.5	kΩ
V_{OH}	HIGH-level output voltage	RST_SIM, CLK_SIM; I_{OH} = −1 mA [2]	-	0.7 × V_{VSIM}	V_{VSIM}	V
		IO_SIM; I_{OH} = −10 µA [2]	-	0.7 × V_{VSIM}	V_{VSIM}	V
		IO_HOST; I_{OH} = −10 µA [2]	-	0.7 × V_{CC}	V_{CC}	V
V_{OL}	LOW-level output voltage	RST_SIM, CLK_SIM; I_{OL} = 1 mA [2]	-	100	300	mV
		IO_SIM; I_{OL} = 1 mA [2]	-	100	300	mV
		IO_HOST; I_{OL} = 1 mA [2]	-	100	300	mV
R_{pd}	pull-down resistance	CLK_HOST, RST_HOST/EN; EN = 0	70	100	130	kΩ

Table 6. Static characteristics *...continued*

2.5 V ≤ V_{BAT} ≤ 5.5 V; 1.55 V ≤ V_{CC} ≤ 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
EMI filter						
R_S	series resistance	IO_SIM [2][4]	-	200	-	Ω
		RST_SIM [4]	-	200	-	Ω
		CLK_SIM [2][4]	-	200	-	Ω
C_{io}	input/output capacitance	IO_SIM [2][4]	-	45	-	pF
		RST_SIM [4]	-	45	-	pF
		CLK_SIM [2][4]	-	45	-	pF

[1] Typical values measured at 25 °C.

[2] V_{IL}, V_{IH} depend on the individual supply voltage per interface.

[3] See Figure 10 for details.

[4] Guaranteed by design.

Table 7. Dynamic characteristics

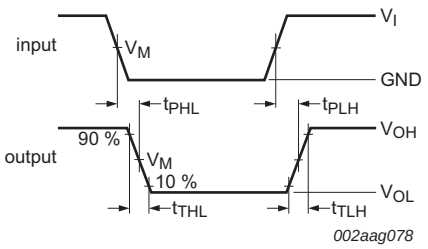
2.5 V ≤ V_{BAT} ≤ 5.5 V; f_{clk} = f_{io} = 1 MHz; T_{amb} = −40 °C to +85 °C; unless otherwise specified. Refer to Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} = 1.8 V; VSIM = 3 V; SIM card C_L ≤ 30 pF; host C_L ≤ 10 pF						
$t_{d(latch)}$	latch delay time	time after ACK from I²C-bus write to latch host I/Os to SIM I/Os; bit 4 = 1 [1]	-	-	5	µs
t_t	transition time	[1]	-	-	10	ns
$t_{sk(o)}$	output skew time	between channels; IO_SIM and CLK_SIM [2]	-	2	-	ns
t_{PD}	propagation delay	I/O channel; SIM card side to host side [1]	-	15	25	ns
		all channels; host side to SIM card side [1]	-	15	25	ns
$f_{o(clk)}$	clock output frequency	CLK_SIM	5	-	-	MHz
$t_{dis(RST\_SIM)}$	RST_SIM disable time	disable time from initiating RST_HOST/EN bit 6 = 1 or from I²C-bus disable ACK	-	20	50	µs
$t_{dis(CLK\_SIM)}$	CLK_SIM disable time		-	25	60	µs
$t_{dis(IO\_SIM)}$	IO_SIM disable time		-	35	65	µs
$t_{dis(VSIM)}$	VSIM disable time	$C_{o(L)}$ = 4.7 µF	-	200	-	µs

[1] All dynamic measurements are done with a 50 pF load. Rise times are determined by internal pull-up resistors.

[2] Skew between any two outputs of the same package switching in the same direction with the same C_L.

9.1 Waveforms



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Data input to data output propagation delay times

10. Application information

Figure 8 is the application circuit for the NVT4556 and shows the typical interface with a SIM card. The V_{CC} pin on the NVT4556 powers the host I/O pins and is designed to be driven from a GPIO. This GPIO then acts as both the host-side power supply and an enable/disable pin. The NVT4556 provides a Low-DropOut (LDO) regulator that is designed for high Power Supply Rejection Ratio (PSRR) at a very low drop-out voltage ($V_{BAT} - V_{VSIM}$). The LDO regulator provides two levels of fixed voltage regulation at 1.8 V or 3 V, which are selected with an I²C-bus write. Since there is only one register, a subaddress is not necessary.

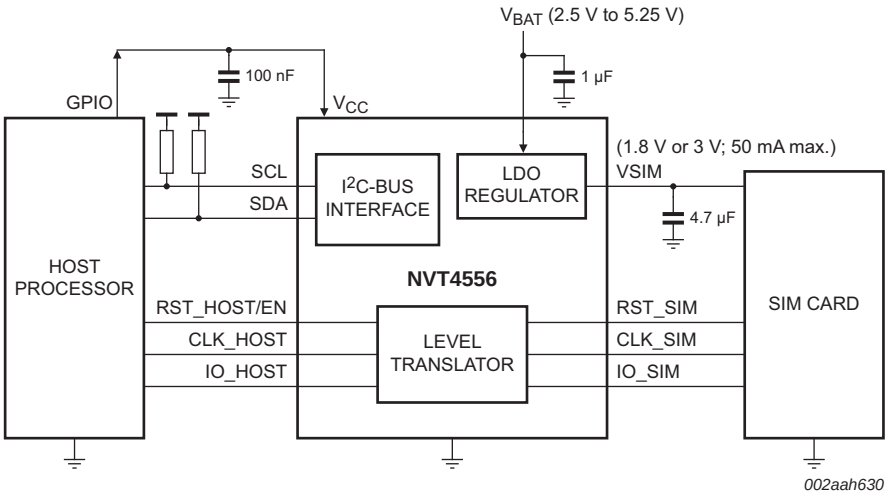


Fig 8. NVT4556 application circuit interfacing with typical SIM card

10.1 Input/output capacitor considerations

It is recommended that a 1 μF capacitor and a 100 nF capacitor having low Equivalent Series Resistance (ESR) are used respectively at the battery (V_{BAT}) and V_{CC} input terminals of the NVT4556. X5R and X7R type multi-layer ceramic capacitors (MLCC) are preferred because they have minimal variation in value and ESR over temperature. The maximum ESR should be < 500 mΩ (50 mΩ typical).

Also, a 2.2 μF to 4.7 μF capacitor is recommended at the Low Dropout regulator (LDO) output terminal to ensure stability. X5R and X7R type are recommended for their minimal variation over temperature and low ESR over frequency which avoids stability issues at high frequencies. The maximum ESR should be < 1.0 Ω. Furthermore, the decrease in capacitance with an increase in the bias voltage should be considered to optimize LDO stability. In addition, the trade-off in LDO stability versus the value and constraint in case size of the capacitor determined by the application must be considered. As output load capacitance decreases, the LDO stability becomes marginal. A given 4.7 μF ceramic capacitor may become 0.33 μF capacitance depending on the effects of bias voltage and temperature. It is recommended to refer to the manufacturer's characterization of a capacitor based on case size, bias voltage and type. Figure 9 is an example of how a 4.7 μF capacitor is affected by the above parameters.

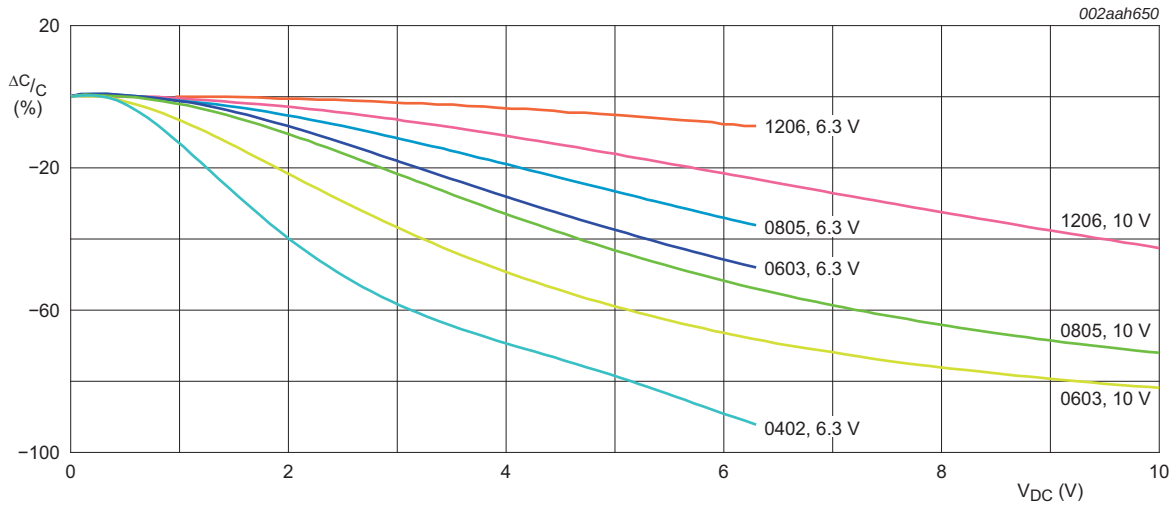


Fig 9. Variation of capacitance for a 4.7 μF capacitor versus DC voltage, value, and case size

10.2 Layout consideration

The capacitors should be placed directly at the terminals and ground plane. Since the internal band gap regulator is the dominant noise source in a typical application, connections and routing of the ground is very important to improve and optimize noise performance, PSRR and transient response. It is recommended to design the PCB with separate ground planes for the V_I (V_{BAT}) and V_O (VSIM) of the LDO regulator with each ground plane connected only at the GND pin of the NVT4556.

10.3 Dropout voltage

The NVT4556 uses a PMOS pass transistor to achieve a very low dropout voltage. When $V_{BAT} - V_{VSIM}$ is less than the dropout voltage, the PMOS transistor operates in the linear region and the input-to-output resistance is R_{DSon} of the PMOS device. The dropout voltage, V_{do}, scales with the output current since the PMOS device behaves like a resistor in the input-to-output path.

10.4 Level translator stage

The architecture of the NVT4556 I/O channel is shown in Figure 10. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is possible only when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one-shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os return to HIGH level once released from being driven LOW.

The channels RST and CLK contain single direction drivers without the holding mechanism of the I/O channel, as these are driven only from the host to the card side.

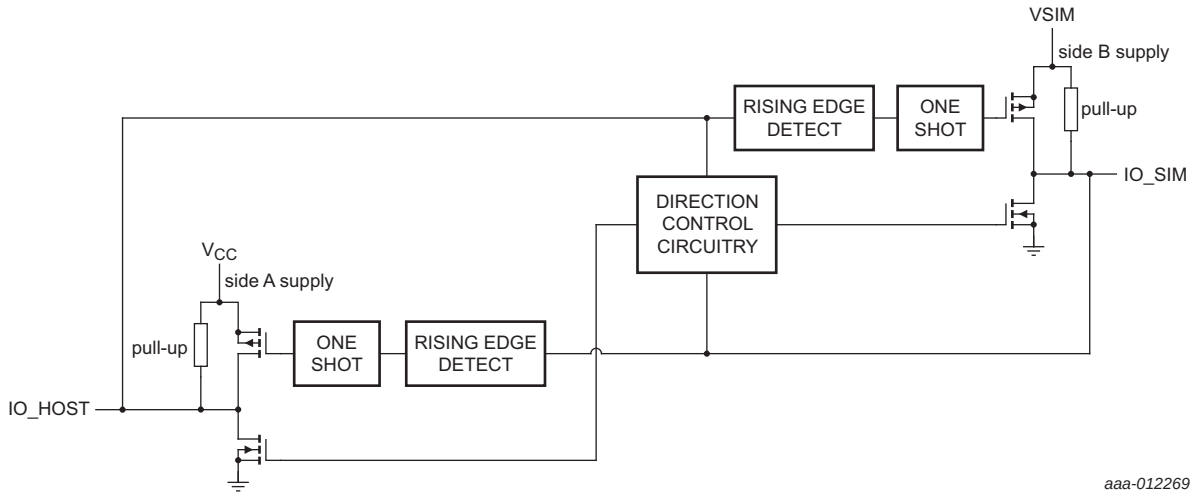


Fig 10. Automatic direction control level translator for HIGH-level direction change interfaces

10.5 LDO block diagram

The block diagram of the LDO is depicted in Figure 11. It contains a pull-down mechanism to avoid any uncontrolled voltage level at the VSIM pin in the disabled state. Furthermore, thermal protection as well as an overcurrent protection are integrated to disable the output in case of a permanent short that may result in excessive self-heating.

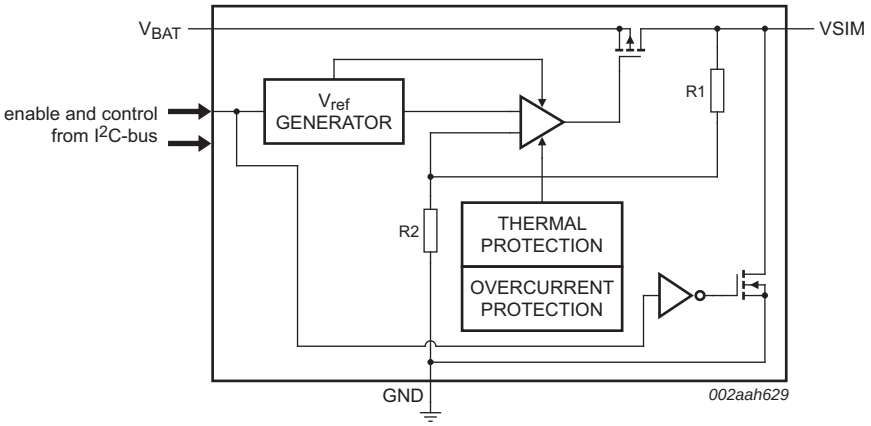


Fig 11. LDO block diagram

The default LDO output voltage is 1.8 V but can be selected to be either 1.8 V or 3.0 V through the proper I²C-bus writes.

The I²C-bus has the ability to disable the LDO such that the VSIM can be powered through an external system regulator. If the LDO is disabled, the RSTn, CLKn and IOn data paths are still active. It is necessary to supply external power to the V_{CC}, VSIM, and V_{BAT} power supply pins, since there is active circuitry that still exists on the three supplies.

10.6 Power-on reset

When power is applied to V_{CC}, an internal Power-On Reset (POR) holds the NVT4556 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the NVT4556 registers and I²C-bus state machine initialize to their default states. Thereafter V_{CC} must be lowered below 1.2 V to reset the device.

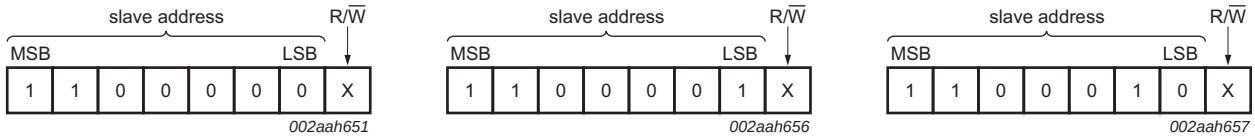
10.7 Serial bus interface

The NVT4556 communicates with a host controller by means of the 2-wire serial bus (I²C-bus) that consists of a serial clock (SCL) and serial data (SDA) signals. The device supports I²C-bus Standard-mode and Fast-mode. The I²C-bus Standard-mode speed is defined to have bus speeds from 0 Hz to 100 kHz. I²C-bus Fast-mode speed is from 0 Hz to 400 kHz. The host or bus master generates the SCL signal and the NVT4556 uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is 1 byte at a time with the Most Significant Bit (MSB) transferred first. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

10.8 Slave address

The NVT4556 uses a 7-bit slave address to identify it on the I²C-bus. The last bit of the address byte defines the operation to be performed. When set to logic 1, a read is selected, while a logic 0 selects a write operation. The level translator's 7-bit fixed slave address is '60h' for the NVT4556AUK, '61h' for the NVT4556BUK and '62h' for the NVT4556CUK. However, for a write operation (R/$\overline{W}$ bit = 0) to the NVT4556, the address byte content (8 bits) is 'C0h' for the NVT4556AUK, 'C2h' for the NVT4556BUK, and 'C4h' for the NVT4556CUK.

Remark: Device variant NVT4556CUK is under development.



a. NVT4556A

b. NVT4556B

c. NVT4556C (under development)

Fig 12. Slave address; normal read/write

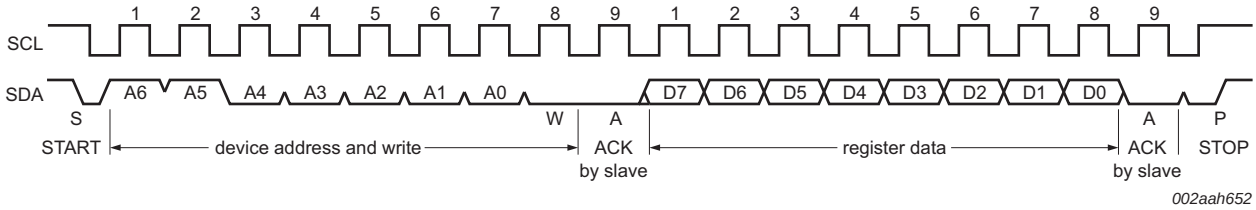
10.9 I²C-bus interface

There is only one data register in this device, so the Pointer register is always set to '00h'. For this reason, a subaddress is not required for reading or writing. Only data is required to be sent on the bus after a slave address acknowledge.

A 'write' to this device always includes the slave address byte and data byte.

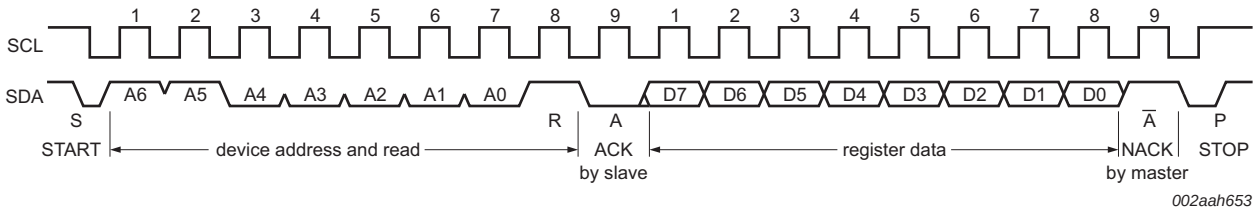
A 'read' to this device always includes the slave address byte and data byte.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).



A = ACK = Acknowledge bit. W = Write bit = 0.

Fig 13. I²C-bus write to NVT4556A



A = ACK = Acknowledge bit. R = Read bit = 1.

Fig 14. I²C-bus read from NVT4556A

10.10 Write operations

10.10.1 Byte Write

In Byte Write mode, the master creates a START condition and then broadcasts the slave address and data to be written. The slave acknowledges the bytes by pulling down the SDA line during the ninth clock cycle following each byte. The master creates a STOP condition after the last ACK from the slave, which then starts the internal write operation (see Figure 15). During internal write, the slave ignores any read/write request from the master.

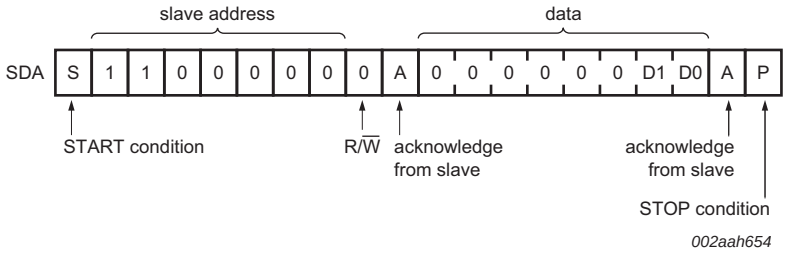


Fig 15. Byte Write for NVT4556A

10.11 Read operations

10.11.1 Byte Read

If the NVT4556 decodes a slave address with a '1' in the R/$\overline{W}$ bit position (Figure 16), it issues an Acknowledge in the ninth clock cycle and then transmits the data byte. The master can then stop further transmission by issuing a No Acknowledge on the ninth bit then followed by a STOP condition.

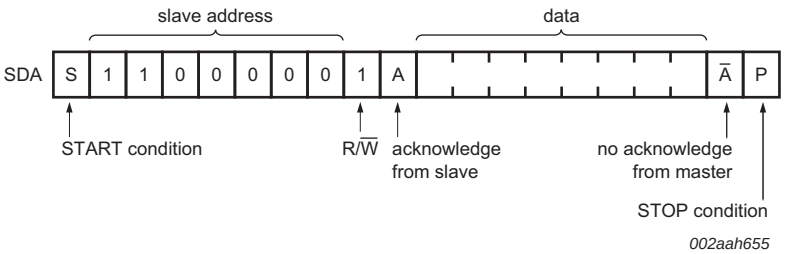


Fig 16. Byte Read for NVT4556A

10.12 User accessible registers

10.12.1 Register overview

This section describes all the registers used in the NVT4556. The device contains only one register which is read/write-able. No subaddress is necessary when reading or writing to the device.

Table 8. Register summary

Address	Register name	Description
00h	DEV_CFG	Device information and revision and enable functions

10.12.2 Register map

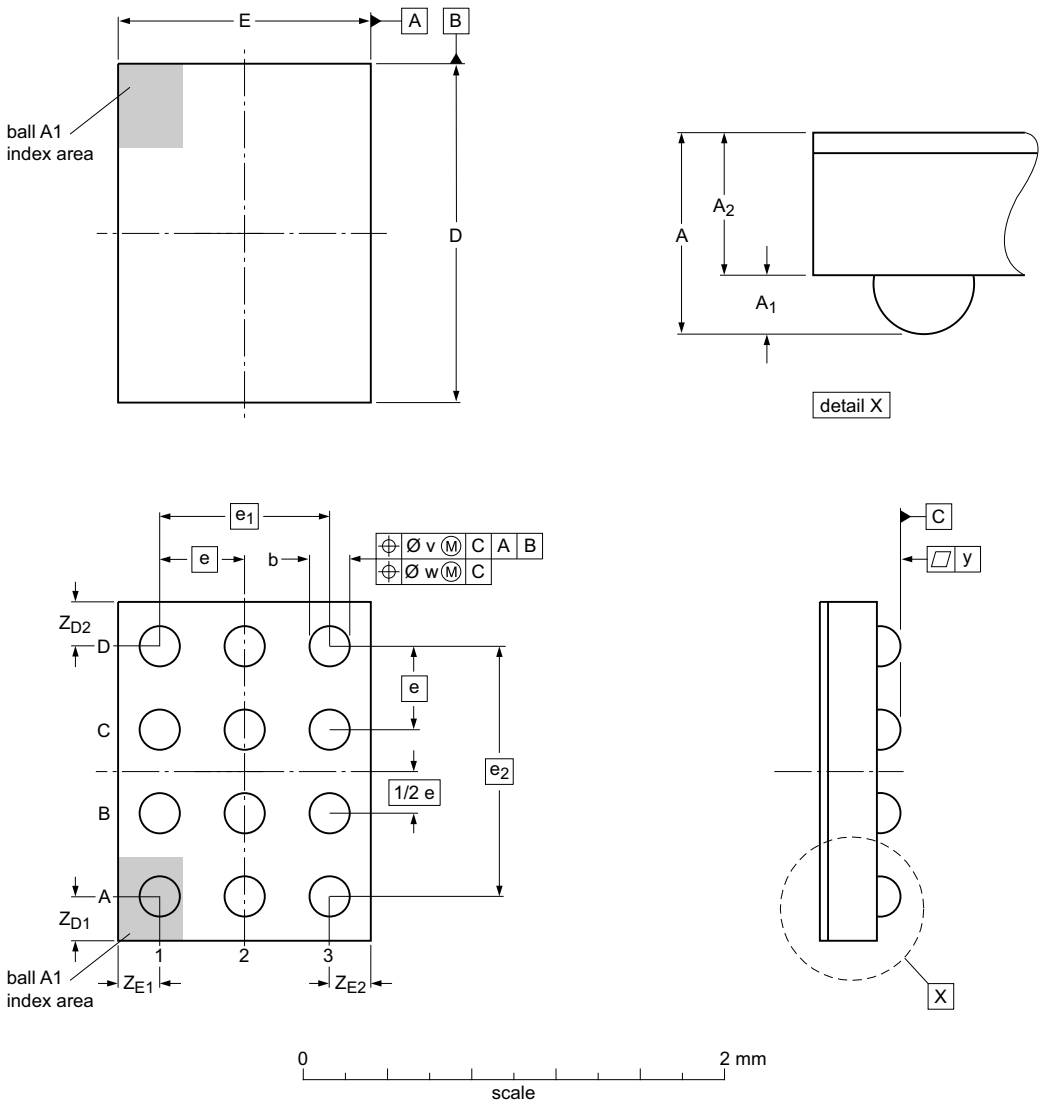
Table 9. User accessible register maps

*Legend: * = default. Register modes and default values are only valid with operating the NVT4556 in I²C-bus mode.*

Address	Register name	Symbol	Bit	Description
00h	DEV_CFG			Device information. Contains enable functions.
		D7	7	LDO disable; enables/disables the LDO. The I/O paths are still operational. V_{VSIM} (VSIM pin) must be provided from the system. V_{BAT} must be connected to the battery voltage. **0*** — LDO enabled (default) **1** — LDO disabled
		D6	6	RST_HOST/EN pin mode select **0*** — RST_HOST enabled (default) The RST_HOST/EN pin passes the logic on the input directly to the RST_SIM pin. **1** — EN The RST_HOST/EN pin becomes an enable/disable pin for the device. The polarity of the RST_HOST/EN pin is set by bit 3. The RST_SIM signal is sent through bit 5.
		D5	5	RST_SIM active: this bit is active only when bit 6 = 1. **0*** — RST_SIM disable (default) This sends and latches a logic LOW to the RST_SIM pin. **1** — RST_SIM enabled This sends and latches a logic HIGH to the RST_SIM pin.
		D4	4	Latch IO states Setting this bit latches the state of the input pins IO_HOST, CLK_HOST and RST_HOST/EN (when bit 6 = 0) to the output pins IO_SIM, CLK_SIM, and RST_SIM. This can be used for clock stop when two NVT4556 devices are used on the same host. **0*** — Latch OFF (default) **1** — I/Os latched
		D3	3	Enable polarity. This bit sets the RST_HOST/EN pin polarity when bit 6 is set to 1. **0*** — Active HIGH enable: Device enables when RST_HOST/EN pin = 1. **1** — Active LOW enable: Device enables when RST_HOST/EN pin = 0.
		-	2	reserved
		D1	1	Voltage selection: selects the output voltage of the LDO **0*** — 1.8 V (default) **1** — 3 V
		D0	0	Device enable **0*** — Disable (default) **1** — Enable bit 6 = 0: R/W bit 6 = 1: R only and displays RST_HOST/EN status

11. Package outline

WLCSP12: wafer level chip-scale package, 12 balls; 1.205 x 1.605 x 0.412 mm (Backside coating included) **NVT4556UK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}
	max	0.412	0.125	0.287	0.205	1.620	1.220										
mm	nom	0.382	0.110	0.272	0.190	1.605	1.205	0.4	0.8	1.2	0.15	0.05	0.05	0.2025	0.2025	0.2025	0.2025
	min	0.352	0.095	0.257	0.175	1.590	1.190										

wlcsp12_nvt4556uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NVT4556UK						~~14-04-11~~ 14-04-22

Fig 17. Package outline NVT4556UK (WLCSP12)

12. Soldering of WLCSP packages

12.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

12.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

12.3 Reflow soldering

Key characteristics in reflow soldering are:

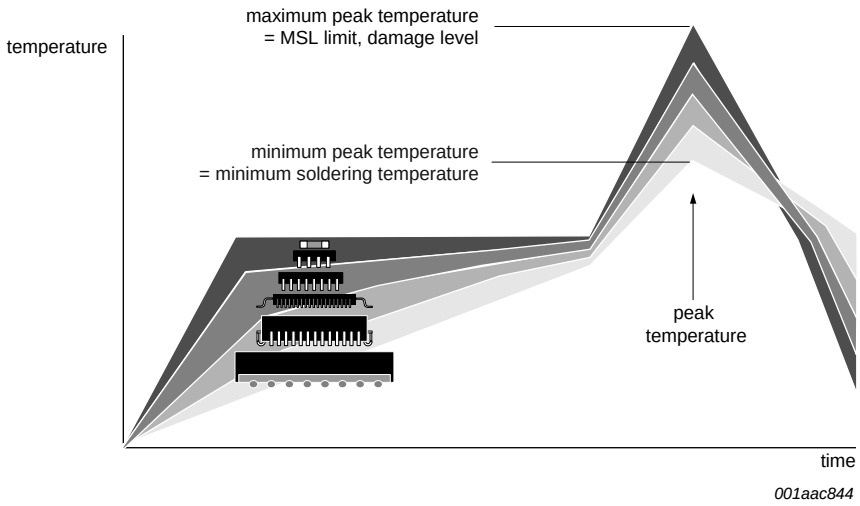
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10.

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

12.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

12.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

12.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

12.3.4 Cleaning

Cleaning can be done after reflow soldering.

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LDO	Low DropOut regulator
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
SIM	Subscriber Identification Module
UVLO	UnderVoltage Lock-Out

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NVT4556 v.1.1	20150825	Product data sheet	-	NVT4556 v.1
Modifications:	• Table 3 "Pin description": V_{CC} description; changed "1.0 nF" to "100 nF"			
NVT4556 v.1	20140602	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 25 August 2015
Document identifier: NVT4556