# 12-V Voice Coil Motor Driver

## DESCRIPTION

The Si9961A is a linear actuator (voice coil motor) driver suitable for use in disk drive head positioning systems. The Si9961A contains all of the power and control circuitry necessary to drive the VCM that is typically found in $3^1/_2$ inch hard disk drives and optical disk drives. The driver is capable of delivering 1.8 A at a nominal supply of 12 V.

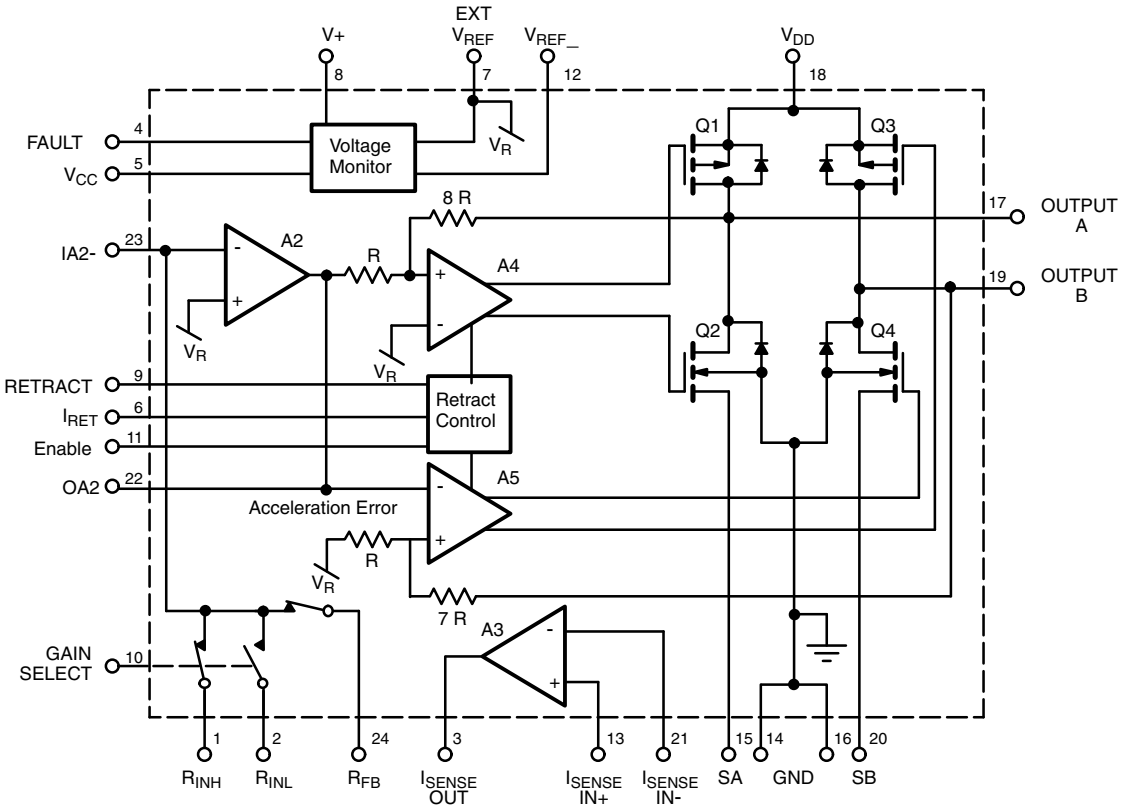
The Si9961A provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier and a power amplifier featuring four complementary MOSFETs in a H-bridge configuration. The output crossover protection ensures no cross-conducting current and true Class B operation during linear tracking. Externally programmable gain switch at the input summing junction increases the resolution and dynamic range for a given DAC. The head retract circuitry can be activated by either an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract.

The Si9961A is constructed on a self-isolated BiC/DMOS power IC process. The IC is available in both standard and lead (Pb)-free, 24-pin SO packages for operation over the commercial, C suffix (0 to 70 °C) temperature range.

## FEATURES

- 1.8 A H-Bridge Output
- Class B Linear Operation
- Externally Programmable Gain and Bandwidth
- Undervoltage Head Retract
- Programmable Retract Current
- Low Standby Current
- Rail-to-Rail Output Swing
- Single 12 V Supply
- System Voltage Monitor with Fault Output

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Limit | Unit |
|---|---|---|---|
| **Voltages Referenced to Common Pin** | | | |
| V+ Supply Range | | - 0.3 V to 16 V | V |
| Pin ($\overline{FAULT}$) | | -0.3 V to $V_{CC}$ + 0.3 V | |
| Pin (Output A & B, Source A & B) | | - 0.3 V to $V_{DD}$ + 0.3 V | |
| Pin (All Others) | | - 0.3 V to V+ + 0.3 V | |
| Maximum Clamp Current<br>Output A, Output B (Pulsed 10 ms at 10 % duty cycle) | | ± 1.8 | A |
| Pin (All Others) | | ± 20 | mA |
| Storage Temperature | | - 65 to 150 | °C |
| Operating Temperature | | 0 to 70 | |
| Junction Temperature ($T_J$) | | 150 | |
| Power Dissipation (Package)[a] | 24-Pin SOIC[b] | 3.125 | W |
| Thermal Impedance ($\Theta_{JA}$)[a] | 24-Pin SOIC | 40 | °C/W |

Notes:
a. Device Mounted with all leads soldered or welded to PC board.
b. Derate 25 mW/°C above 25 °C.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## SPECIFICATIONS

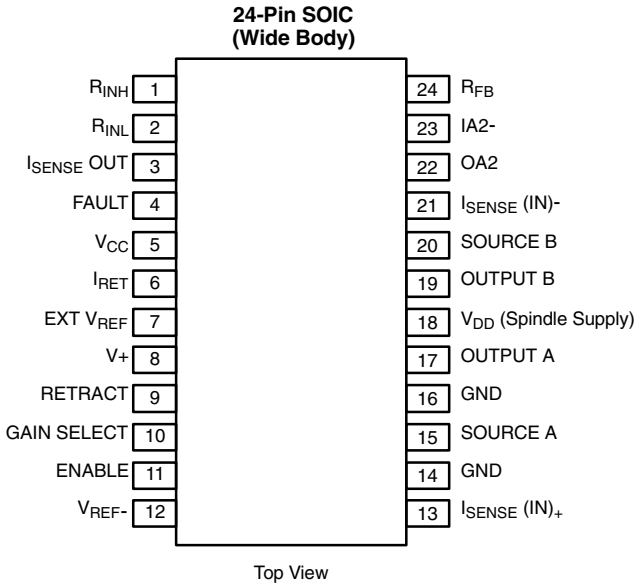
| Parameter | Symbol | Test Conditions Unless Otherwise Specified<br>V+ = 12 V ± 10 %, $V_{DD}$ = 11.6 V ± 10 %<br>$V_{CC}$ = 5 V ± 10 %, $V_{REF-}$ = GND = 0 V<br>$V_{REF}$ = 5 V ± 5 % | Limits C Suffix 0 to 70 °C Min[b] | Typ[a] | Max[b] | Unit |
|---|---|---|---|---|---|---|
| **Bridge Outputs ($A_4$, $A_5$)** | | | | | | |
| High Level Output Voltage | $V_{OH}$ | $I_{OH}$ = 1.0 A, $V_{DD}$ = 10.2 V, $OA_2 = V_{REF}$ ± 1 V | 8.0 | 9.1 | | V |
| Low Level Output Voltage | $V_{OL}$ | $I_{OL}$ = - 1.0 A, $OA_2 = V_{REF}$ ± 1 V | | 0.6 | 1.1 | |
| Clamp Diode Voltage | $V_{CL}$ | $I_F$ = 1.0 A, $\overline{ENABLE}$ = High | | | 2.5 | |
| Amplifier Gain | | Output $V_{RANGE} = V_{REF}$ ± 2 V | 12 | 16 | 18 | V/V |
| Dynamic Crossover Current | | Measured at $V_{DD}$ | | 10 | | mA |
| Slew Rate | SR | | 1 | | | V/µS |
| Small Signal Bandwidth (- 3 dB) | | | | 0.2 | | MHz |
| Input Deadband | | | - 60 | | 60 | mV |
| **$A_2$, Loop Compensation Amplifier** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | - 8 | | 8 | mV |
| Input Bias Current | $I_B$ | Gain Select = High, $IA_2$- = 5 V | - 50 | | 50 | nA |
| Unity Gain Bandwidth | | $R_{LOAD}$ = 10 kΩ, $C_{LOAD}$ = 100 pF to $V_{REF}$ | | 1 | | MHz |
| Slew Rate | SR | | 1 | | | V/µs |
| Power Supply Rejection Ratio | PSRR | at 10 kHz | | 50 | | dB |
| Open Loop Voltage Gain | $A_{VOL}$ | | | 80 | | |
| Output Voltage Swing | $V_O$ | $R_{LOAD}$ = 10 kΩ to $V_{REF}$ | $V_{REF}$ - 2 | | $V_{REF}$ + 2 | V |
| **$A_3$, Current Sense Amplifier** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | - 5 | | 5 | mW |
| Input Impedance | $R_{IN}$ | $I_{SENSE}$IN+ to $I_{SENSE}$IN- | | 5 | | kΩ |
| Small Signal Bandwidth (- 3 dB) | | $R_{LOAD}$ = 10 kΩ, $C_{LOAD}$ = 100 pF to $V_{REF}$ | | 1 | | MHz |
| Common Mode Rejection Ratio | CMRR | at 5 kHz | | 50 | | dB |
| Slew Rate | SR | | 2 | | | V/µs |
| Gain | | | 3.9 | 4 | 4.1 | V/V |
| Input Common-Mode Voltage Range | $V_{CM}$ | To GND | - 0.3 | | 2 | V |
| Output Voltage Swing | $V_O$ | $R_{LOAD}$ = 10 kΩ, $C_{LOAD}$ = 100 pF to $V_{REF}$ | $V_{REF}$ - 2 | | $V_{REF}$ + 2 | |

## SPECIFICATIONS

| Parameter | Symbol | Test Conditions Unless Otherwise Specified V+ = 12 V ± 10 %, $V_{DD}$ = 11.6 V ± 10 % $V_{CC}$ = 5 V ± 10 %, $V_{REF-}$ = GND = 0 V $V_{REF}$ = 5 V ± 5 % | Limits C Suffix 0 to 70 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min[b] | Typ[a] | Max[b] | |
| **Supply** | | | | | | |
| Supply Current (Normal) | $I_{CC}$ | Static, No Load $\overline{RETRACT}$ = High $\overline{ENABLE}$ = Low | | | 0.01 | mA |
| | $I_{V+}$ | | | 2 | 5 | |
| | $I_{DD}$ | | | 5 | 13 | |
| Supply Current (Standby) | $I_{CC}$ | Static, No Load $\overline{RETRACT}$ = High $\overline{ENABLE}$ = High | | | 0.01 | |
| | $I_{V+}$ | | | 0.2 | 0.4 | |
| | $I_{DD}$ | | | 0.8 | 1.6 | |
| $V_{DD}$ Range | $V_{DD}$ | Normal Mode | 10.2 | 11.6 | 13.2 | V |
| | | Retract Mode | 2.0 | | 14 | |
| $V_{CC}$ Range | $V_{CC}$ | | 4.5 | 5 | 5.5 | |
| V+ Range | V+ | | 10.8 | 12 | 13.2 | |
| **Gain Select Switch** | | | | | | |
| $R_{FB}$ Switch Resistance | | | | 108 | 240 | Ω |
| $R_{INH}$ Switch Resistance | | IA2 - = 5 V | | 135 | 300 | |
| $R_{INL}$ Switch Resistance | | | | 810 | 1800 | |
| **$V_{REF}$ (EXT)** | | | | | | |
| Input Current | $I_{REF}$ | OA2 = $V_{REF}$ | 0.15 | 0.40 | 0.65 | mA |
| External Voltage Range | $V_{REF}$ | | 4.75 | 5 | 5.25 | V |
| **Power Supply Monitor** | | | | | | |
| $V_{CC}$ Undervoltage Threshold | | $V_{REF}$ = 5.0 V | 3.82 | 4.12 | 4.42 | V |
| Hysteresis | | | | 40 | | mV |
| V+ Undervoltage Threshold | | $V_{REF}$ = 5.0 V | 9.1 | 9.8 | 10.6 | V |
| Hysteresis | | | | 100 | | mV |
| **Gain Select, $\overline{RETRACT}$, $\overline{ENABLE}$ Input** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 3.5 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 1.5 | |
| Input High Current | $I_{IH}$ | $V_{IN}$ = 5 V | - 1 | | 1 | µA |
| Input Low Current | $I_{IL}$ | $V_{IN}$ = 0 V | - 1 | | 1 | |
| **$\overline{FAULT}$ Output** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = - 100 µA | $V_{CC}$ - 0.8 | $V_{CC}$ - 0.33 | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | 0.25 | 0.50 | |
| Output High Sourcing Current | $I_{OHS}$ | $V_{OUT}$ = 0 V | | 400 | 1100 | µA |
| **RETRACT Current Control ($\overline{RETRACT}$ = Low, Output Current from A to B)** | | | | | | |
| $I_{RET}$ Bias Voltage | $V(I_{RET})$ | $V_{DD}$ = 10 V, $R_{RET}$ = 3.74 kΩ | | 0.66 | | V |
| Retract Output Pull-Up Voltage | $V_{OUT\ A}$ | $V_{DD}$ = 2.5 V to 14 V, $I_{OUTA}$ = 30 mA | $V_{DD}$ - 1 | | | |
| Retract Output Pull-Down Current | $I_{OUTB}$ | $V_{DD}$ = 10 V, $V_{OUTB}$ = 5 V $R_{RET}$ = 3.74 kΩ $R_{SB}$ = 0.5 Ω, $T_A$ = 25 °C | 22 | 30 | 38 | mA |
| Maximum Emergency Retract Current | $I_{OUTB}$ (Max) | $V_{DD}$ = 2 V, $V_{OUTB}$ = 0.7 V $R_{RET}$ = < 10 Ω $R_{SB}$ = 0.5 Ω | 40 | | | |
| Retract Current $V_{DD}$ Supply Rejection Ratio | | $V_{DD}$ = 2 V to 14 V, $R_{RET}$ = 3.74 kΩ | | 3.0 | | %/V |
| Retract Current Temperature Coefficient | | $V_{DD}$ = 10 V, $R_{RET}$ = 3.74 kΩ | | - 0.3 | | %/°C |

Notes:
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

## PIN CONFIGURATION AND ORDERING INFORMATION




| ORDERING INFORMATION | | | |
|---|---|---|---|
| **Part Number** | **Lead (Pb)-free Part Number** | **Temperature Range** | **Package** |
| Si9961ACY | | 0 to 70 °C | SOIC-24 (Wide Body) |
| Si9961ACY-T1 | Si9961ACY-T1-E3 | | |

## APPLICATIONS

### Introduction

The Si9961A Voice Coil Motor (VCM) driver integrates the active feedback and drive components of a head-positioning servo loop for high-performance hard-disk applications. The Si9961A operates from a 12 V (± 10 %) power supply and delivers 1 A of steady-state output current. This device is made possible by a power IC process which combines bipolar, CMOS and complimentary DMOS technologies. CMOS logic and linear components minimize power consumption, bipolar front-ends on critical amplifiers provide necessary accuracy, and complimentary (P- and N-Channel) DMOS devices allow the transconductance output amplifier to operate from ground to $V_{DD}$. Two user-programmable, current feedback/input voltage ratios may be digitally selected to optimize gain for both seek and track following modes, to maximize system accuracy for a given DAC resolution. An undervoltage lockout circuit monitors the V+ supply and generates a fault signal to trigger an orderly head-retract sequence at a voltage level sufficient to allow the spindle motor's back EMF-generated voltage to supply the necessary head parking energy. Head retract can also be commanded via a separate $\overline{\text{RETRACT}}$ input. VCM current during retract can be user programmed with a single external resistor. External components are limited to R/C filter components for loop compensation and the resistors that are required to program gain, retract current, and the load current sense.

### User-Programmable Gains

During linear operation, the transconductance amplifiers' gains (input voltage at $V_{IN}$ vs. VCM current, in Figure 1) are set by external resistors $R_3$ -> $R_5$, $R_{SA}$, and $R_{SB}$ and selected by gain input. After selecting a value for $R_{SA}$ and $R_{SB}$ that will yield the desired VCM current level, the High and Low feedback gain ratios may be determined by the following:

$$\text{High Gain} = \left(\frac{R_5}{R_3}\right)\frac{1}{4\,R_S} \qquad \text{(GAIN SELECT Input = High)}$$

$$\text{Low Gain} = \left(\frac{R_5}{R_4}\right)\frac{1}{4\,R_S} \qquad \text{(GAIN SELECT Input = Low)}$$

Where $R_S = R_{SA} = R_{SB}$

Input offset current may then be calculated as:

$$I_{OS} = \frac{1}{4\,R_S}\left(\left(\frac{(R_S + R_{IN})}{R_{IN}}V_{OSA2}\right) + 5\,V_{IAS3}\right)$$

Where $R_{IN} = R_3$ or $R_4$

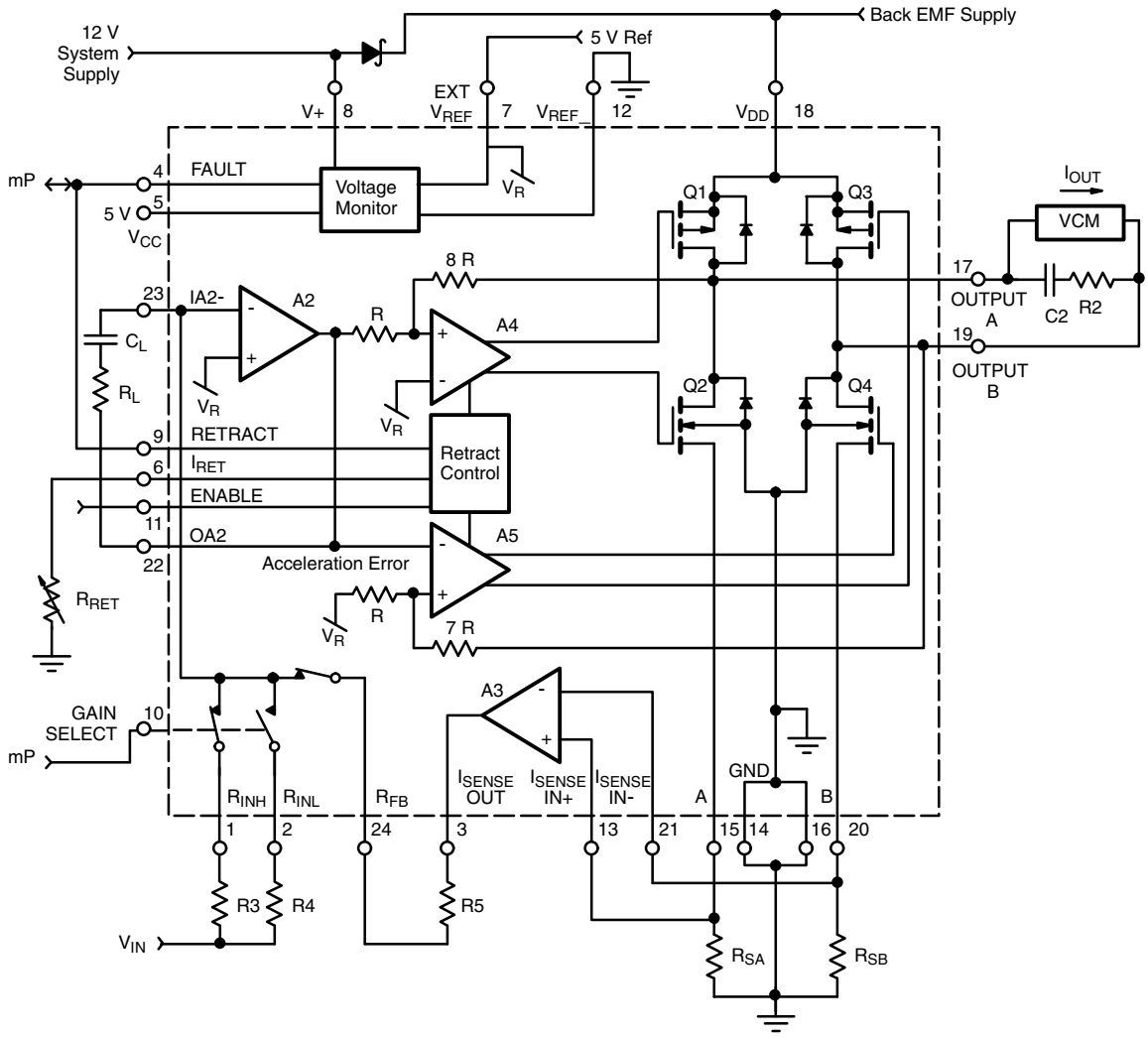



**Figure 1. Si9961A Typical Application**

### Head Retract

A low on the $\overline{\text{RETRACT}}$ input pin turns output devices Q1 and Q4 on, and output devices Q2 and Q3 off. Maximum VCM current can be set during head retract by adding an external resistor between the IRET pin and ground. Maximum retract current may be calculated as:

$$I_{OUT} = 175 \times I_{ret} = 175 \times \frac{0.66\ V}{R_{ret}}$$

Head retract can be initiated automatically by an undervoltage condition (either the 12 V or 5 V supplies on the Si9961A) by connecting the $\overline{\text{FAULT}}$ output to the $\overline{\text{RETRACT}}$ input.

A high $\overline{\text{ENABLE}}$ input puts both driver outputs in a high-impedance state. The $\overline{\text{ENABLE}}$ function can be used to eliminate quiescent output current when power is applied but the head has been parked, such as a sleep mode. A sleep-mode power down sequence should be preceded by a retract signal since a power failure during this state may not provide adequate spindle-motor back EMF to permit head retraction.

### Transconductance Amplifier Compensation

The Si9961A features an integrated transconductance amplifier to drive the voice coil motor (VCM). To ensure proper operation, this amplifier must be compensated specifically for the VCM being driven. As a first approximation, the torque constant and inertia of the VCM may be ignored, although they will have some influence on the final results, especially if large values are involved. (See Figure 1.)

**Frequency Compensation:**

The VCM transconductance (in siemens) of this simplified case may be expressed in the s (Laplace) plane as:)

$$g_v = \frac{\frac{1}{L_v}}{s + \frac{R_v}{L_v}}$$

Where $R_v$ = VCM resistance in ohms
$L_V$ = VCM inductance in henrys
s is the Laplace operator

In this case, the transconductance pole is at - Rv/Lv. It is desirable to cancel this pole in the interest of stability. To do this, a compensation amplifier is cascaded with the VCM and its driver. The transfer function of this amplifier is:

$$H_c = A \times \frac{\left(s + \frac{1}{R_L \times C_L}\right)}{s}$$

Where $R_L$ = Compensation amplifier feedback resistor in ohms
$C_L$ = Compensation amplifier feedback capacitor in farads
A = Compensation amplifier and driver voltage gain at high frequency

If $R_L$ x $C_L$ is set equal to $L_v/R_v$, then the combined open loop transconductance in siemens becomes:

$$g_{to} = \frac{A}{s \times L_v}$$

In this case, the transconductance has a single pole at the origin. If this open loop transfer is closed with a transimpedance amplifier having a gain of B ohms, the resultant closed loop transconductance stage has the transfer function (in siemens) of:

$$g_{tc} = \frac{\frac{A}{L_v}}{s + \frac{A \times B}{L_v}}$$

Where B = Current feedback transimpedance amplifier gain in ohms.

The entire transconductance now contains only a single pole at - A*B/Lv. A and B are chosen to be considerably higher than the servo bandwidth, to avoid undue phase margin reduction.

As a typical example, in the referenced schematic, assume that Rsa and Rsb = 0.5 Ω, $R_5 = R_3$ = 10 kΩ, VCM inductance (Lv) = 1.5 mH, VCM resistance (Rv) = 15 Ω. Hence:

$R_v$ = 15 Ω
$L_v$ = 1.5 mH
B = 2 Ω
A = 16 x $R_L$/10000
$C_L = Lv/(R_v \times R_L) = 100 \times 10^{-6}/R_L$ farads

**Gain Optimization:**

There are three things to consider when optimizing the gain (A) above. The first is servo bandwidth. The main criterion here is to avoid having the transconductance amplifier cause an undue loss of phase margin in the overall servo (mechanical + electrical + firmware) loop. The second is to avoid confirguing a bandwidth that is more than required in view of noise and stability considerations. The third is to keep the voltage output waveform overshoot to a level that will not cause cross-conduction of the output FETs.

The first two problems can be considered together. Let us assume a disk drive with a spindle RPM of 4400 and with 50 servo sectors per track. The sample rate is therefore:

$$f_s = 50 \times \frac{440}{60}$$ This is a sample frequency of 3667 H:

As a rule of thumb, the open loop unity gain crossover frequency of the entire servo (mechanical + electrical + firmware) loop should be less than 1/10 of the sample frequency. In this example, the servo open loop unity gain crossover frequency would be less than 367 Hz. If we allow only a 10° degradation in phase margin due to the transconductance amplifier, then a phase lag of 10° at 367 Hz is acceptable. This results in a 3 dB point in the transconductance at :

$$f_{3db} = \frac{367}{\tan(10)}$$

or a 3 dB point in the transconductance at 2081 Hz.

The pole in the closed loop transconductance (- A * B / Lv) should then be 2081 * 2 * π = 13075. This means that A = 9.8. From the above equation for A, $R_L$ = 6.2 kΩ. This sets the minimum gain limit governed by the servo bandwidth requirements. The gain should not be much greater than this, since increased noise will degrade the servo response.

The third problem, keeping the transconductance amplifier voltage output wave form overshoot to a level that will not cause the wrong output FETs to conduct, can be evaluated by deriving the voltage transfer function of the closed loop transconductance amplifier from input voltage to output voltage (Vin to output A and B on the reference schematic).

This is :

$$H_{to} = A \times \frac{s + p}{s + x}$$

Where p = $1/R_L$ x $C_L$) or $R_v/L_v$ Comp amplifier zero/VCM pole
x = A x $B/L_v$ closed loop pole

If a unit step voltage is applied to the above transfer function and the inverse Laplace transform is taken, the output result is:

$$V_O = A \times \frac{p + (x - p) \times e^{-x \times t}}{x}$$

Where t = time

As we can see, if x = p (i.e. if the VCM pole and compensation amplifier zero = the transconductance closed loop pole), then Vo reduces to A. In other words, a step input results in a step output without overshoot. If x < p then a step input results in an increased rise time output and no overshoot. If x > p, a step input results in a step output with an overshoot.

If this overshoot is large enough, there may be a cross-conduction condition in the output FETs.

Let us look at the above equation at t = 0 and t >> 0, expressed in terms of the open loop high frequency voltage gain, A.

$$V_O = A \qquad \text{At } t = 0$$

$$V_O = \frac{p \times L_v}{B} \qquad \text{At } t > > 0$$

In the example shown above, p = 10,000 and A = 9.8. This means that there is some overshoot. At t = 0, the output voltage is 9.8 V per volt of input. At some later time, it has dropped to 7.5 V per volt of input. An overshoot of 31 % is thus produced.

The maximum overshoot voltage requires careful consideration, since it constitutes a potentially catastrophic problem area. If we had decided to optimize for no overshoot, A would equal 7.5, and hence the closed loop pole (A * B / Lv) would be 10,000, which is a frequency of 1.592 kHz. This would have resulted in a phase margin degradation of 13° at the 367 Hz frequency desired. This may or may not be acceptable. One must weigh the servo bandwidth, phase margin degradation, and maximum voltage at the VCM for each individual case.

**Result:**

In the example for the 2081 Hz roll-off case with 31 % overshoot and proper pole cancellation, the compensation values are:

$R_L$ = 6.2 kΩ
$C_L$ = 0.016 µF

In the example for the 1592-Hz roll-off case with no overshoot and proper pole cancellation, the compensation values are:

$R_L$ = 4.7 kΩ
$C_L$ = 0.022 µF

The linearity of the transconductance amplifier (around a center value of 500 mA/volt) is shown in Figure 2. In this case, the output current sense resistors ($R_{SA}$ and $R_{SB}$) were ± 5 % tolerance, 0.5 Ω . Any mismatch between $R_{SA}$ and $R_{SB}$ contribute directly to mismatch between the positive and negative "full-scale". Including the external resistor mismatch, the overall loop nonlinearity is approximately 1 % maximum over a ± 250 mV input voltage range.

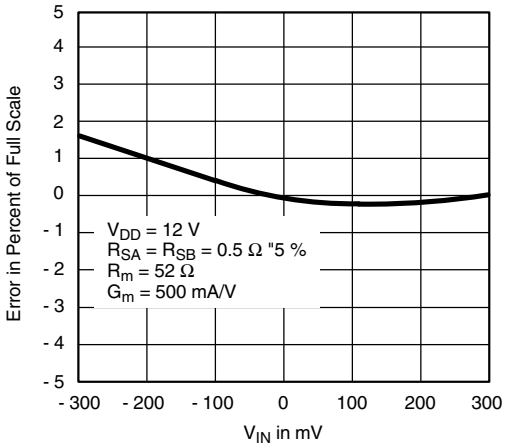



**Figure 2. Si9961A Transconductance End Point Non-Linearity**

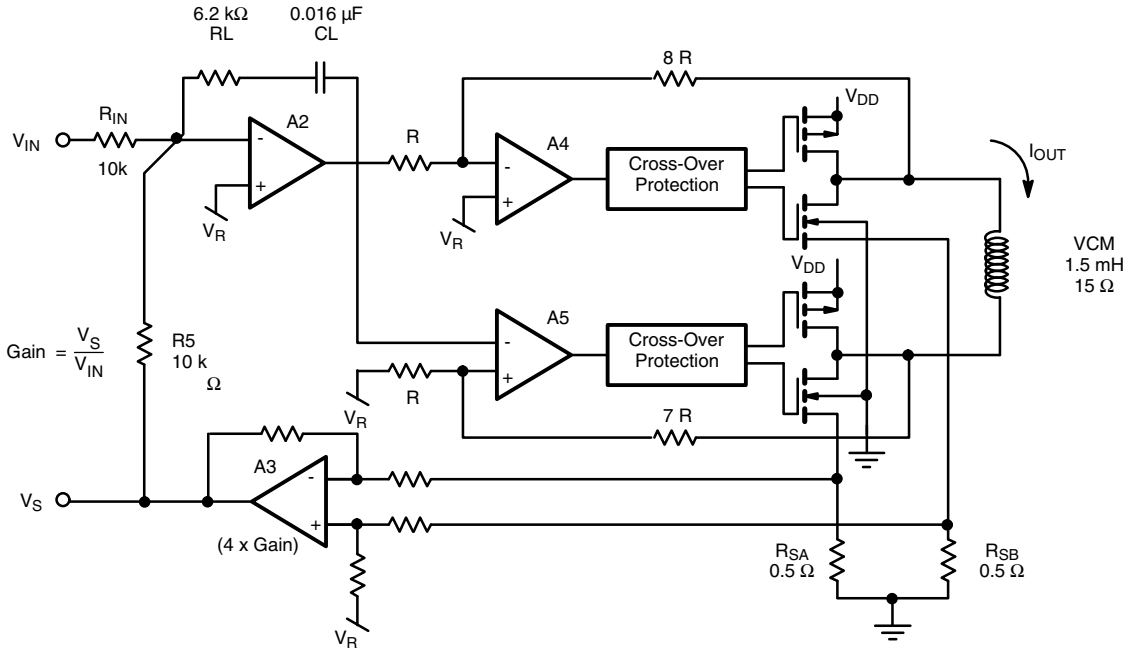



**Figure 3. Transconductance Amplifier**

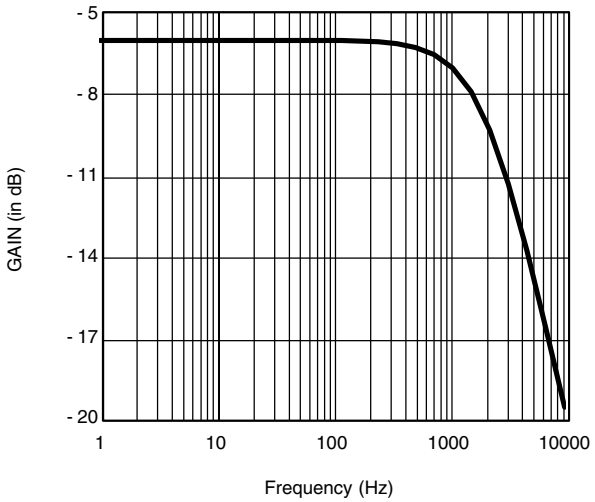



**Figure 4. $R_L$ = 6.2 kΩ, $C_L$ = 0.016 µF**

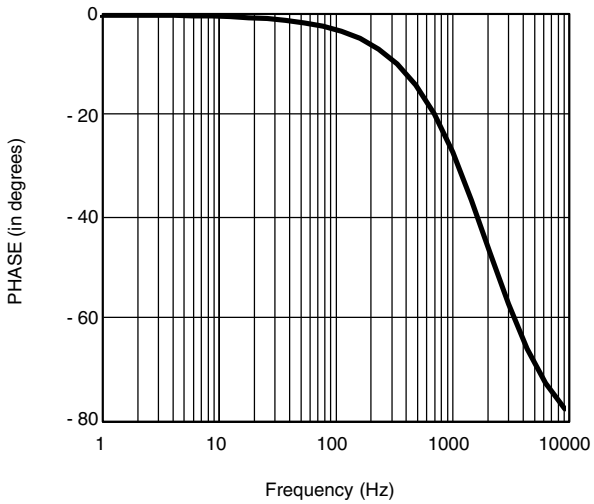



**Figure 5. $R_L$ = 6.2 kΩ, $C_L$ = 0.016 µF**

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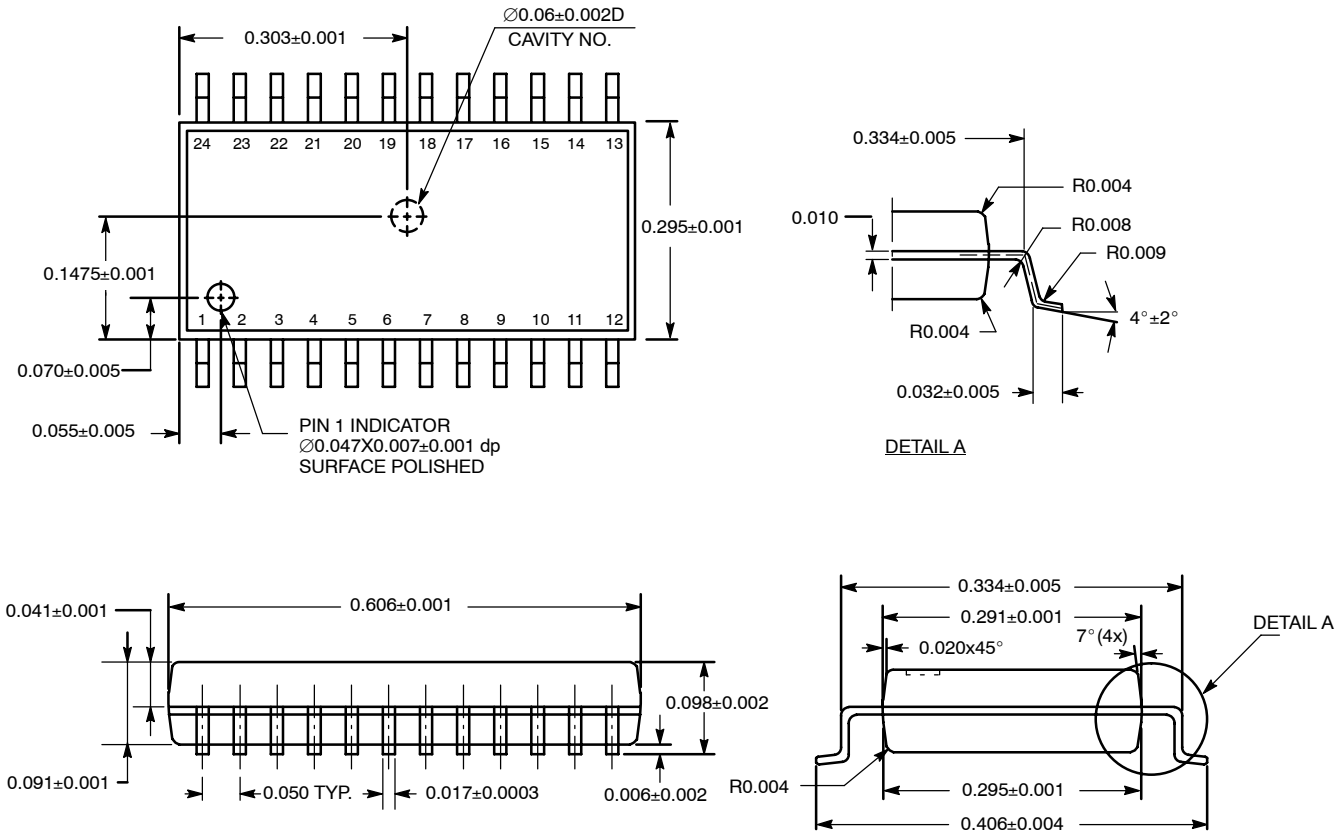
## SOIC (WIDE-BODY): 24-LEAD (POWER IC ONLY)

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DWG: 5930

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