

Vishay Siliconix

Low Voltage, 1 Ω Single SPDT Analog Switch (1:2 Multiplexer) with Power Down Protection

DESCRIPTION

The DG4157 is a high performance single pole double throw analog switch designed for 1.65 V to 5.5 V operation with single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance as 1 Ω at 4.5 V power supply and fast switching speed. The - 3 dB bandwidth is typically 117 MHz.

DG4157 features break before make switch performance, and guarantees logic high control input threshold as low as 1.4 V over the range up to 5.5 V.

It can handle both analog and digital signals and permits signals with amplitudes of up to V_{CC} to be transmitted in either direction.

Power down protection circuit is built in to prevent abnormal current path through signal pins during power down

Each output pin (A, B₀, or B₁) can withstand greater than 8 kV (human body model).

It is available in both SC-70-6 and miniQFN6 packages.

The features make it an ideal part for the switching of audio, video, and data stream.

FEATURES

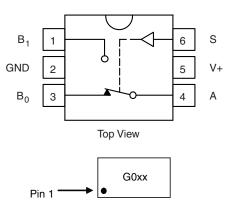
- Direct cross of industry standard xxx4157
- 1.65 V to 5.5 V operation voltage range
- Guaranteed 1.4 V logic high input threshold at $V_{CC} = 5.5 \text{ V}$
- 117 MHz, 3 dB bandwidth
- · Low on-resistance
- Power down protection
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



HALOGEN FREE

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

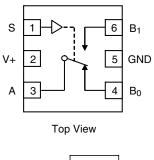


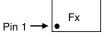


Device Marking: G0xx xx = Date/Lot Traceability Code

TRUTH TABLE						
LOGIC INPUT (S)	FUNCTION					
0	B ₀ Connected to A					
1	B ₁ Connected to A					

miniQFN-6L





Device Marking: Fx x = Date/Lot Traceability Code

ORDERING INFORMATION						
TEMP. RANGE	PART NUMBER					
-40 °C to +85 °C	SC-70-6L	DG4157DL-T1-E3				
	miniQFN-6L	DG4157DN-T1-E4				





ABSOLUTE MAXIMUM RATINGS						
PARAMETER		LIMIT	UNIT			
Reference V+ to GND	-0.3 to +6	V				
S, A, B ^a	-0.3 to (V+ + 0.3)	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \				
Continuous Current (Any terminal)	± 200	A				
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 400	mA			
Storage Temperature	D Suffix	-65 to +150	°C			
Power Dissipation (Packages) ^b	SC-70-6L ^c	250	mW			
Fower Dissipation (Fackages)	miniQFN-6L ^d	160	IIIVV			

Notes

- a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 3.1 mW/°C above 70 °C.
- d. Derate 2 mW/°C above 70 °C.

SPECIFICATIONS								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP.ª	LIMITS -40 °C to +85 °C			UNIT	
		$V+ = 3 V$, $V_{IN} = 0 V$ or $V+ e$		MIN. b	TYP. c	MAX. b		
DC Characteristics								
		$V+ = 2.7 \text{ V}, B_0 \text{ or } B_1 = 1.5 \text{ V}, I_0 = 100 \text{ mA}$	Room	-	1.7	2.5		
On Resistance	R _{ON}	V+ - 2.7 V, B(01 B) = 1.5 V, 10 = 100 HIA	Full	-	-	3		
On nesistance	TION	$V+ = 4.5 \text{ V}, B_0 \text{ or } B_1 = 3.5 \text{ V}, I_0 = 100 \text{ mA}$	Room	ı	0.95	1.2		
		$V + = 4.5 \text{ V}, B_0 \text{ Of } B_1 = 3.5 \text{ V}, I_0 = 100 \text{ Hz}$	Full	-	-	1.4		
		$V+ = 2.7 \text{ V}, B_0 \text{ or } B_1 = 0.75 \text{ V}, 1.5 \text{ V},$ $I_0 = 100 \text{ mA}$		-	0.2	-		
On Resistance Flatness	R _{FLATNESS}	$V+ = 4.5 \text{ V}, B_0 \text{ or } B_1 = 1 \text{ V}, 3.5 \text{ V},$	Room	-	0.14	0.3	Ω	
		$I_0 = 100 \text{ mA}$	Full	-	-	0.4		
	ΔR _{ON}	$V+ = 2.7 \text{ V}, B_0 \text{ or } B_1 = 1.5 \text{ V},$ $I_0 = 100 \text{ mA}$	Room	-	0.04	-		
On Resistance Match		$V+ = 4.5 \text{ V}, B_0 \text{ or } B_1 = 3.5 \text{ V},$	Room	-	0.05	0.12		
		$I_O = 100 \text{ mA}$	Full	-	-	0.15		
Constant Off Landson Comment	I _{OFF}		Room	-2	-	2	nA	
Switch Off Leakage Current		V+ = 5.5 V, A = 1 V, 4.5 V	Full	-20	-	20		
Contab On Lankana Commant		B_0 or $B_1 = 4.5$ V, 1 V or floating	Room	-4	-	4		
Switch On Leakage Current	I _{ON}		Full	-40	-	40		
Digital Control								
Input, High Voltage	V_{INH}	V+ = 2.7 V to 5.5 V	Full	1.4	-	ı	V	
Input, Low Voltage	V_{INL}	V+ = 2.7 V to 3.3 V	Full	-	-	0.4	v	
Input Current	I _{INH} , I _{INL}	$V_{IN} = 0$ or $V+$	Full	-1	-	1	μA	
Power Supply								
Power Supply Range	V+		Full	1.65	-	5.5	V	
Quiescent Supply Current	I+	V+ = 5.5 V, V _{IN} = 0 V, 5.5 V	Room	-	0.05	0.5	μA	
Quioscent Supply Suitent	IT.	ντ – 5.5 ν, ν _{IN} – 6 ν, 5.5 ν	Full	-	-	1	μΛ	



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SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED	TEMP.a	LIMITS -40 °C to +85 °C			UNIT
TANAMETEN	OTHER	V+ = 3 V, V _{IN} = 0 V or V+ e	12.011	MIN. b	TYP.c	MAX. b	
AC Characteristics							
		$V+ = 2.7 \text{ V}, B_0 \text{ or } B_1 = 1.5 \text{ V}, R_L = 50 \Omega,$	Room	-	40	55	
Turn-On Time ^d		C _L = 35 pF	Full	ı	1	60	
rum-on rime	t _{ON}	$V+ = 4.5 \text{ V}, B_0 \text{ or } B_1 = 1.5 \text{ V}, R_L = 50 \Omega,$	Room	-	22	37	
		C _L = 35 pF	Full	-	-	40	
	t _{OFF}	$V+ = 2.7 \text{ V}, B_0 \text{ or } B_1 = 1.5 \text{ V}, R_L = 50 \Omega,$	Room	-	12	27	ns
Turn-Off Time d		$C_L = 35 \text{ pF}$	Full	-	-	30	
rum-on time •		$V+ = 4.5 \text{ V}, B_0 \text{ or } B_1 = 1.5 \text{ V}, R_L = 50 \Omega,$	Room	-	8	23	
		C _L = 35 pF	Full	-	-	25	
	t _{BBM}	$V+=2.7 \text{ V}, \ B_0=B_1=1.5 \text{ V}, \ R_L=50 \ \Omega, \ C_L=35 \text{ pF}$	Room	1	26	-	
Break-Before-Make Time ^d		$V+=4.5 \; V, \; B_0=B_1=1.5 \; V, \; R_L=50 \; \Omega, \\ C_L=35 \; pF$	ROOM	1	15	-	
Charge Injection d	Q	$C_L = 1 \text{ nF, } R_{GEN} = 0 \Omega, V_{GEN} = 0 \text{ V}$	Room	-	50	-	рC
O((1 1 1) d	OIDD	$R_L = 50 \Omega$, $f = 1 MHz$	Doom	-	-58	-	- dB
Off Isolation d	OIRR	$R_L=50 \Omega$, $f=10 MHz$	Room	-	-31	-	
Crosstalk ^d	,,	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	D	-	-63	-	
Crosstalk ^a	X _{TALK}	$R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MHz$	Room	-	-36	-	
Bandwidth ^d	BW	R _L = 50 Ω	Room	-	117	-	MHz
Total Harmonic Distortion d	THD	R_L = 600 Ω , V_{IN} = 0.5 V , f = 20 kHz to 20 kHz	Room	-	0.02	-	%
Capacitance							•
BX Port Off Capacitance d	C _{B(OFF)}			-	20	-	
A Port On Capacitance d	C _{A(ON)}	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	Room	1	57	-	pF
Control Pin Capacitance d				-	5	-]

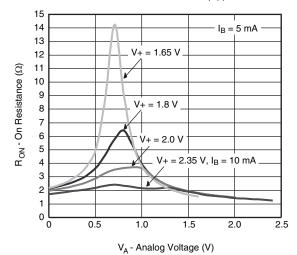
Notes

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.

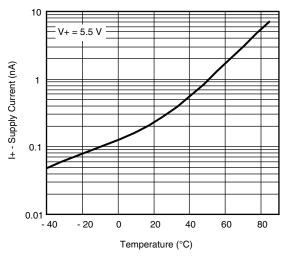
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



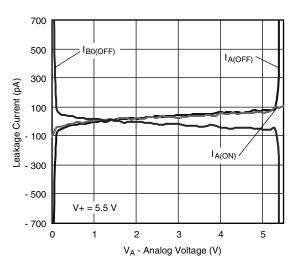
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



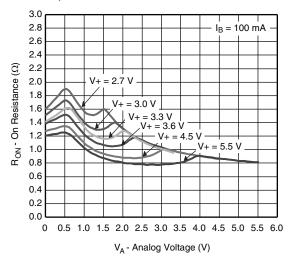
R_{ON} vs. V_A and Supply Voltage



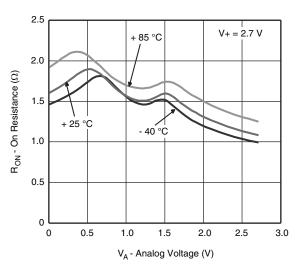
Supply Current vs. Temperature



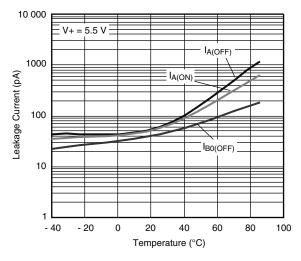
Leakage vs. Analog Voltage



R_{ON} vs. V_A and Supply Voltage



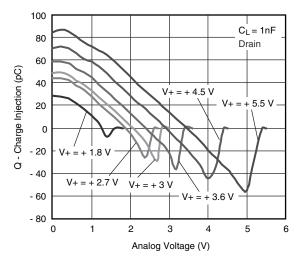
 R_{ON} vs. V_D and Temperature



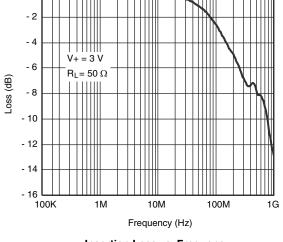
Leakage Current vs. Temperature



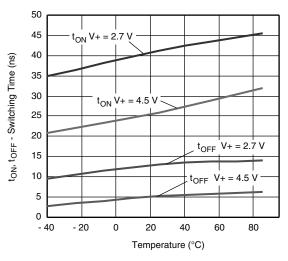
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



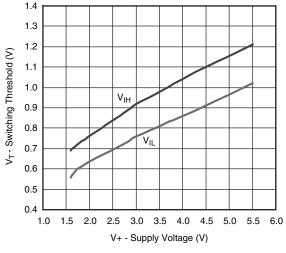
Charge Injection vs. Analog Voltage



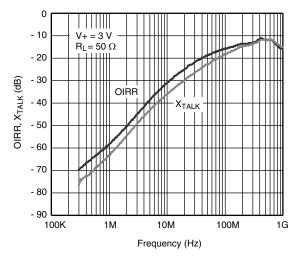
Insertion Loss vs. Frequency



Switching Time vs. Temperature



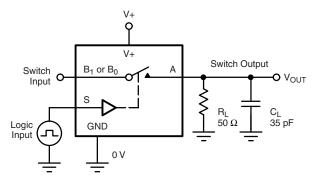
Switching Threshold vs. Supply Voltage

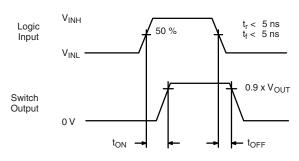


Off-Isolation and Crosstalk vs. Frequency



TEST CIRCUITS





C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_A \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Fig. 1 - Switching Time

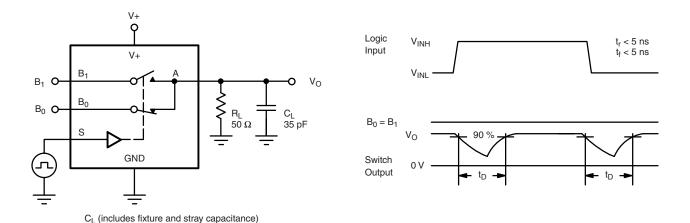


Fig. 2 - Break-Before-Make Interval

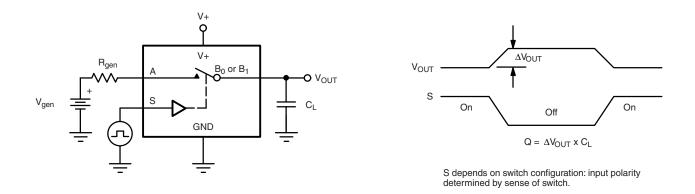


Fig. 3 - Charge Injection

TEST CIRCUITS

Fig. 4 - Off-Isolation

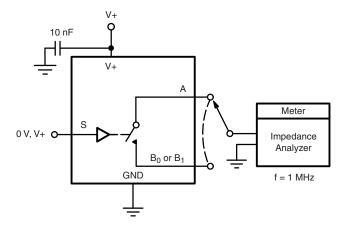
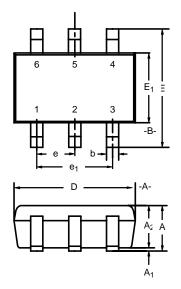


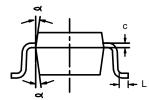
Fig. 5 - Channel Off/On Capacitance

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SC-70: 6-LEADS





	MIL	LIMET	ERS	I	S	
Dim	Min	Nom	Max	Min	Max	
Α	0.90	-	1.10	0.035	-	0.043
A ₁	_	-	0.10	_	_	0.004
A ₂	0.80	-	1.00	0.031	_	0.039
b	0.15	.15 - 0.30 0.0		0.006	_	0.012
С	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
Е	1.80	1.80 2.10 2.40		0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65BSC				0.026BSC	;
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
۵	7°Nom 7°Nom					
ECN: S-03946—Rev. B, 09-Jul-01						

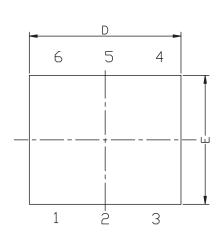
DWG: 5550

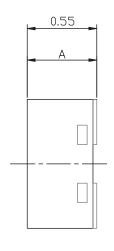
Document Number: 71154 www.vishay.com 06-Jul-01 sww.vishay.com

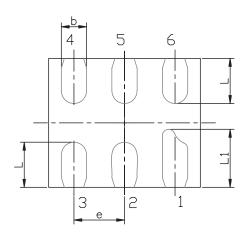


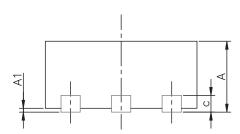
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MINI QFN-6L CASE OUTLINE









DIM	MILLIMETERS			INCHES			
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.	
Α	0.50	0.55	0.60	0.0197	0.0217	0.0236	
A1	0.00	-	0.05	0.000	0.002		
b	0.15	0.20	0.25	0.006	0.010		
С	0.15 REF			0.006 REF			
D	1.15	1.20	1.25	0.045 0.047 0.04		0.049	
E	0.95	1.00	1.05	0.037	0.039	0.041	
е		0.40 BSC					
L	0.30	0.35	0.40	0.012	0.014	0.016	
L1	0.40	0.45	0.50	0.016	0.018	0.020	

ECN T-07039-Rev. A, 12-Feb-07 DWG: 5958

Document Number: 74497

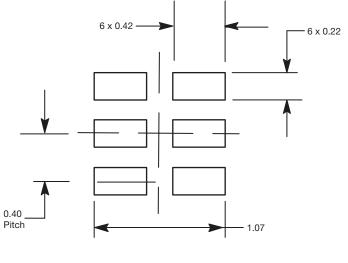
12-Feb-07

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RECOMMENDED MINIMUM PADS FOR MINI QFN 6L



Mounting Footprint Dimensions in mm

Document Number: 66556 www.vishay.com Revision: 05-Mar-10

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