8-Ch/Dual 4-Ch High-Performance CMOS Analog Multiplexers

DESCRIPTION

The DG408 is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409 is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408, DG409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see Technical Article TA201.

FEATURES

- Low on-resistance - $R_{DS(on)}$: 100 Ω
- Low charge injection - Q: 20 pC
- Fast transition time - t_{TRANS}: 160 ns
- Low power - I_{SUPPLY}: 10 µA
- Single supply capability
- 44 V supply max. rating
- TTL compatible logic
- **Compliant to RoHS directive 2002/95/EC**

Pb-free Available

RoHS* COMPLIANT

BENEFITS

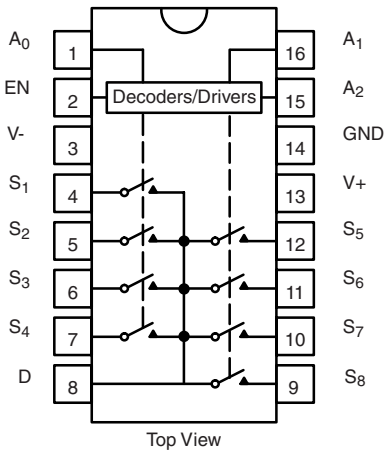
- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges (± 5 V to ± 20 V)

APPLICATIONS

- Data acquisition systems
- Audio signal routing
- ATE systems
- Battery powered systems
- High rel systems
- Single supply systems
- Medical instrumentation

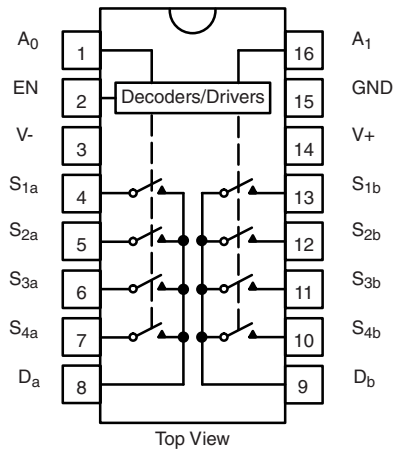
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG408 Dual-In-Line, SOIC and TSSOP



Top View

DG409 Dual-In-Line, SOIC and TSSOP



Top View

* Pb containing terminations are not RoHS compliant, exemptions may apply

TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE DG408

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

ORDERING INFORMATION DG408

Temp. Range	Package	Part Number		
- 40 °C to 85 °C	16-Pin Plastic DIP	DG408DJ DG408DJ-E3		
	16-Pin SOIC	DG408DY DG408DY-E3 DG408DY-T1 DG408DY-T1-E3		
	16-Pin TSSOP	DG408DQ DG408DQ-E3 DG408DQ-T1 DG408DQ-T1-E3		
Temp. Range	**Package**	**Generic #**	**DSCC #**	**Ordering Part Number**
- 55 °C to 125 °C	16-Pin CerDIP	DG408AK DG408AK-E3 DG408AK/883	- - 5962-9204201MEA	DG408AK DG408AK-E3 9204201EA
	LCC-20	DG408AZ/883	5962-9204201M2A 5962-9204201M2C	92042012A 92042012C
	Flat-Pack 16[a]	DG408AL/883	5962-9204201MXA 5962-9204201MXC	9204201XA 9204201XC

ORDERING INFORMATION DG409

Temp. Range	Package	Part Number
- 40 °C to 85 °C	16-Pin Plastic DIP	DG409DJ DG409DJ-E3
	16-Pin SOIC	DG409DY DG409DY-E3 DG409DY-T1 DG409DY-T1-E3
	16-Pin TSSOP	DG409DQ DG409DQ-E3 DG409DQ-T1 DG409DQ-T1-E3

ORDERING INFORMATION DG409				
Temp. Range	**Package**	**Generic #**	**DSCC #**	**Ordering Part Number**
- 55 °C to 125 °C	16-Pin CerDIP	DG409AK DG409AK-E3 DG409AK/883	- - 5962-9204202MEA	DG409AK DG409AK-E3 9204202EA
	LCC-20	DG409AZ/883	5962-9204202M2A 5962-9204202M2C	92042022A 92042022C
	Flat-Pack 16[a]	DG409AL/883	5962-9204202MXA 5962-9204202MXC	9204202XA 9204202XC

Note:
a. Block diagram and pin configuration not shown.

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any Terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max.)		100	
Storage Temperature	(A Suffix)	- 65 to 150	°C
	(DJ, DY Suffix)	- 65 to 125	
Power Dissipation (Package)[b]	16-Pin Plastic DIP[c]	450	mW
	16-Pin Narrow SOIC and TSSOP[d]	600	
	16-Pin CerDIP[e]	900	
	LCC-20[f]	750	

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75 °C.
d. Derate 7.6 mW/°C above 75 °C.
e. Derate 12 mW/°C above 75 °C.
f. Derate 10 mW/°C above 75 °C.

SPECIFICATIONS[a]

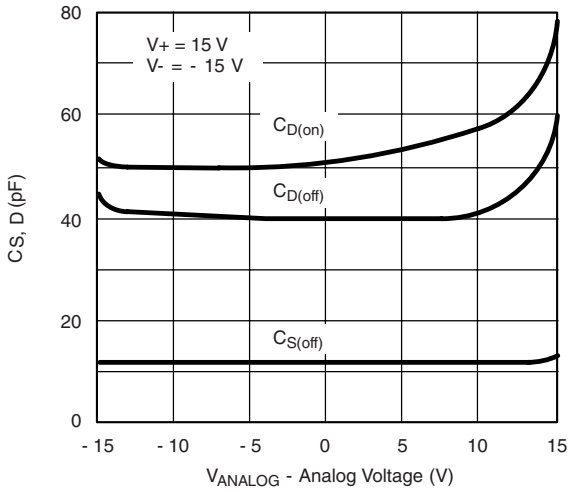
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 10 V, I_S = - 10 mA		Room Full	40		100 125		100 125	Ω
$R_{DS(on)}$ Matching Between Channels[g]	$\Delta R_{DS(on)}$	V_D = ± 10 V		Room			15		15	%
Source Off Leakage Current	$I_{S(off)}$	V_S = ± 10 V V_D = ± 10 V, V_{EN} = 0 V		Room Full		- 0.5 - 50	0.5 50	- 0.5 - 5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ± 10 V V_S = ± 10 V V_{EN} = 0 V	DG408	Room Full		- 1 - 100	1 100	- 1 - 20	1 20	
			DG409	Room Full		- 1 - 50	1 50	- 1 - 10	1 10	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 10 Sequence Each Switch On	DG408	Room Full		- 1 - 100	1 100	- 1 - 20	1 20	
			DG409	Room Full		- 1 - 50	1 50	- 1 - 10	1 10	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{AH}	V_A = 2.4 V, 15 V		Full		- 10	10	- 10	10	µA
Logic Low Input Current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		- 10	10	- 10	10	
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Full	160		250		250	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room		10		10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	115		150 225		150	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	105		150		150	
Charge Injection	Q	C_L = 10 nF, V_S = 0 V		Room	20					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ f = 100 kHz		Room	- 75					dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	3					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V V_D = 0 V f = 1 MHz	DG408	Room	26					
			DG409	Room	14					
Drain On Capacitance	$C_{D(on)}$		DG408	Room	37					
			DG409	Room	25					
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0 V or 5 V		Full	10		75		75	µA
Negative Supply Current	I-			Full	1	- 75		- 75		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room Full	0.2		0.5 2		0.5 2	mA
Negative Supply Current	I-			Full		- 500		- 500		µA

SPECIFICATIONS[a] for Single Supply									
		Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]			**A Suffix** - 55 °C to 125 °C		**D Suffix** - 40 °C to 85 °C		
Parameter	**Symbol**		**Temp.**[b]	**Typ.**[c]	**Min.**[d]	**Max.**[d]	**Min.**[d]	**Max.**[d]	**Unit**
Analog Switch									
Drain-Source On-Resistance[e, f]	$R_{DS(on)}$	V_D = 3 V, 10 V, I_S = - 1 mA	Room	90					Ω
Dynamic Characteristics									
Switching Time of Multiplexer[e]	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V	Room	180					ns
Enable Turn-On Time[e]	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V V_{S1} = 5 V	Room	180					
Enable Turn-Off Time[e]	$t_{OFF(EN)}$		Room	120					
Charge Injection[e]	Q	C_L = 1 nF, V_S = 6 V, R_S = 0	Room	5					pC

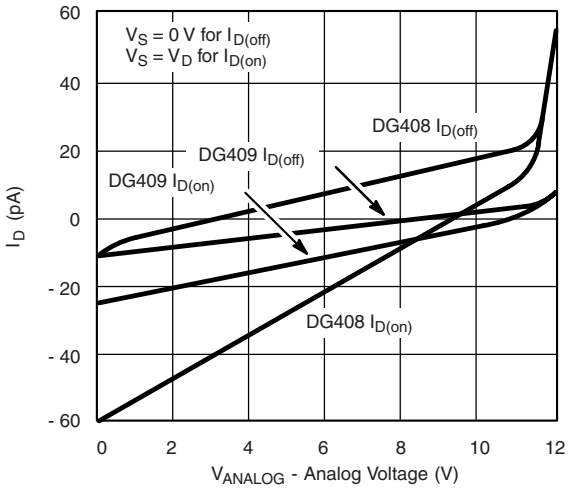
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

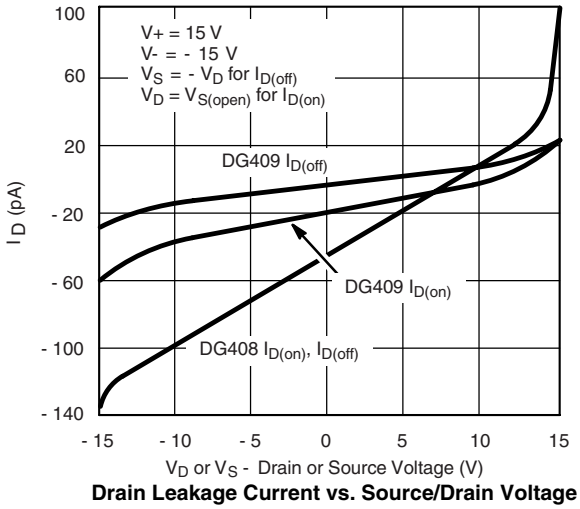
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



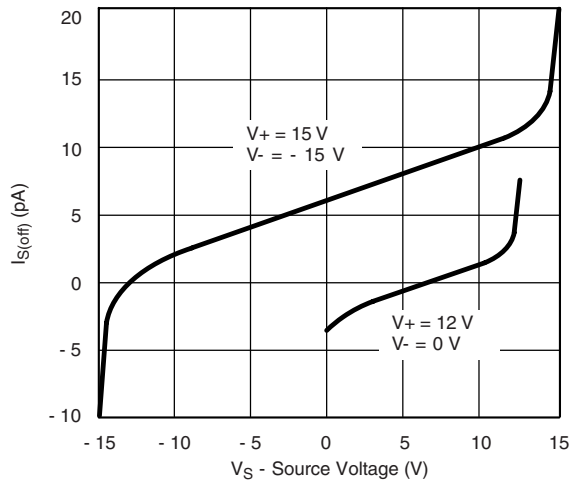
Source/Drain Capacitance vs. Analog Voltage



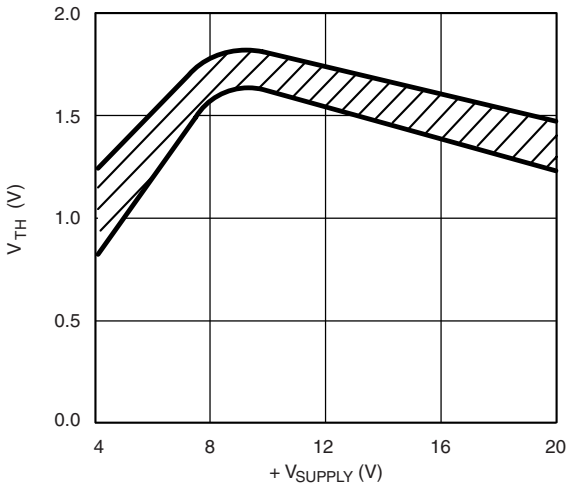
Drain Leakage Current vs. Source/Drain Voltage (Single 12 V Supply)



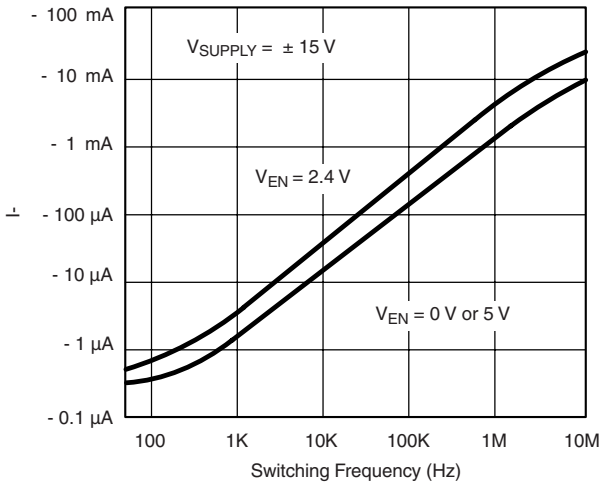
Drain Leakage Current vs. Source/Drain Voltage



Source Leakage Current vs. Source Voltage

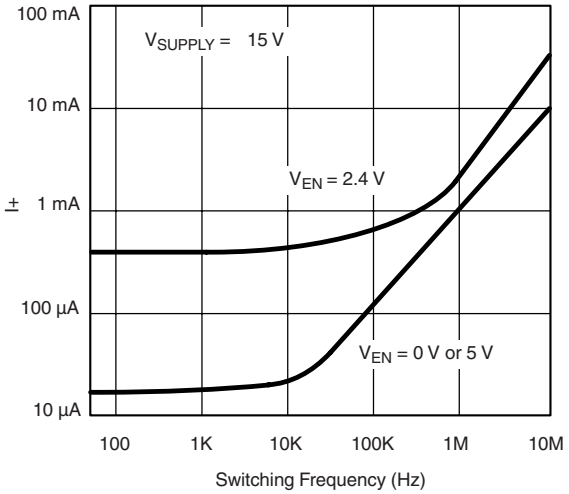


Input Switching Threshold vs. Supply Voltage

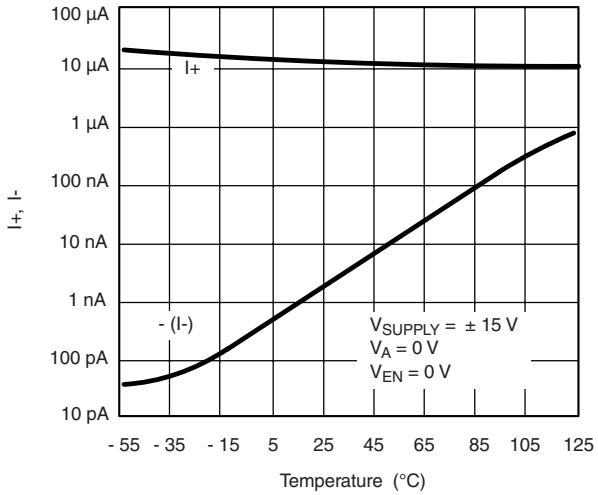


Negative Supply Current vs. Switching Frequency

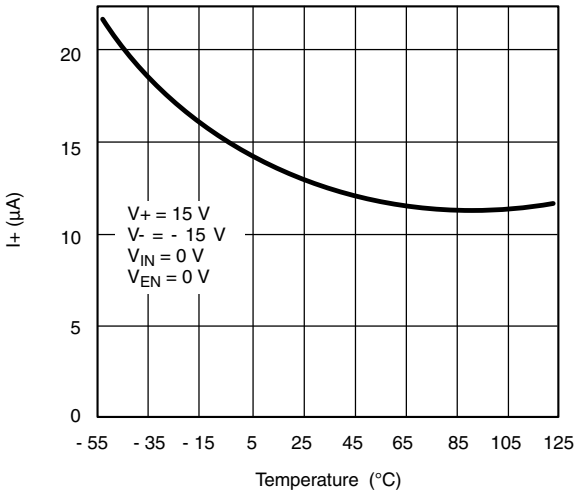
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



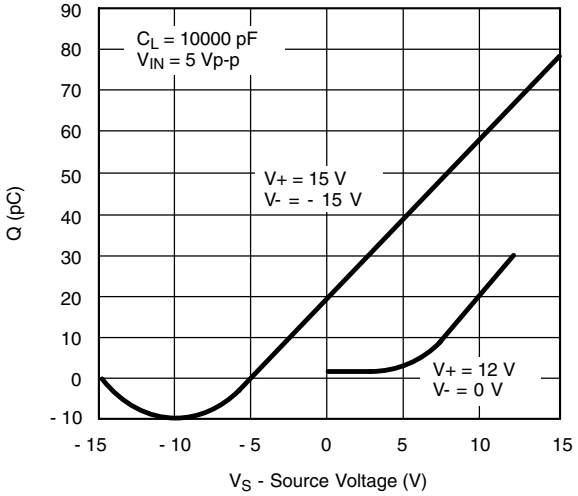
Positive Supply Current vs. Switching Frequency



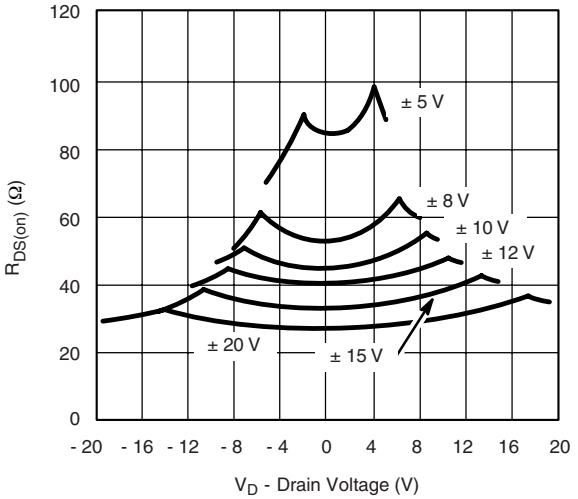
I_{SUPPLY} vs. Temperature



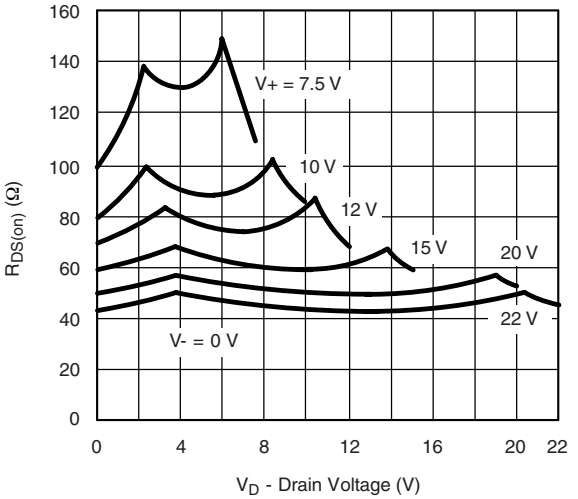
Positive Supply Current vs. Temperature (DG408)



Charge Injection vs. Analog Voltage

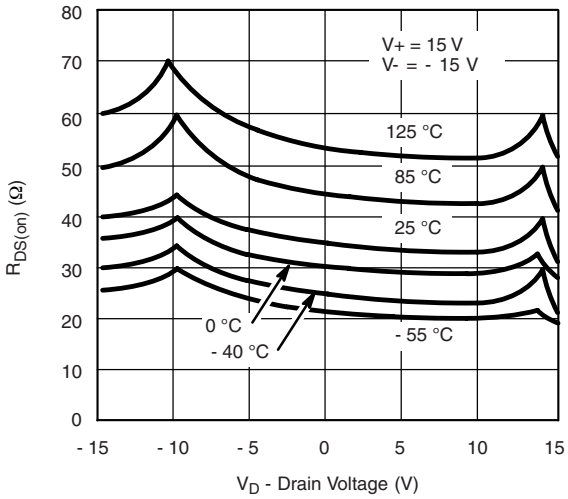


$R_{DS(on)}$ vs. V_D and Supply

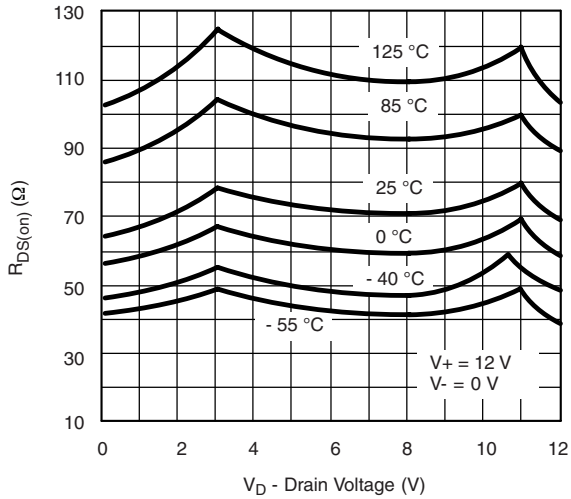


$R_{DS(on)}$ vs. V_D and Supply (Single Supply)

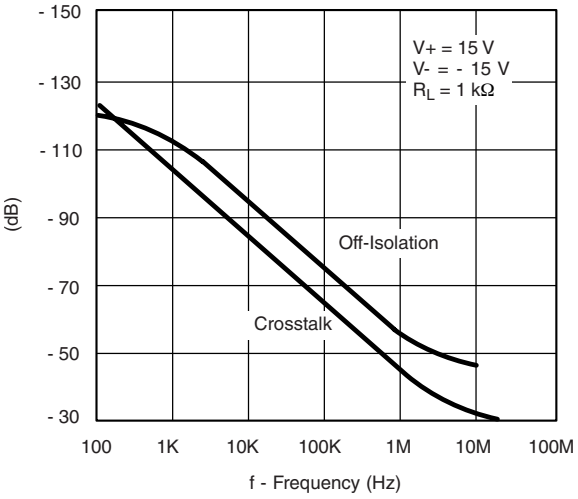
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



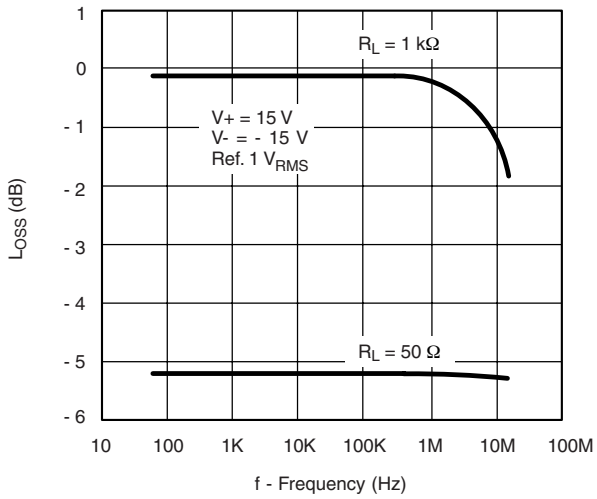
$R_{DS(on)}$ vs. V_D and Temperature



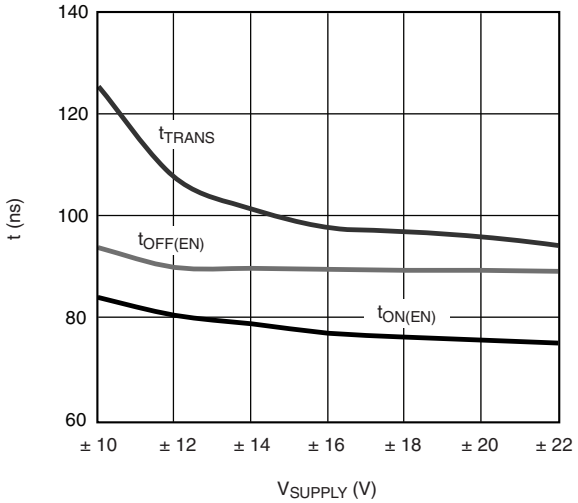
$R_{DS(on)}$ vs. V_D and Temperature (Single Supply)



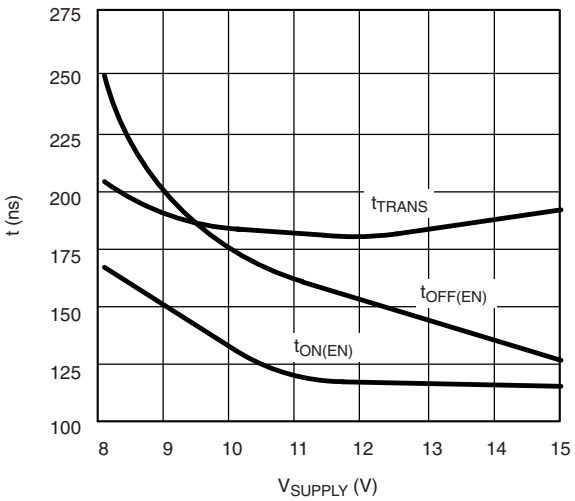
Off Isolation and Crosstalk vs. Frequency



Insertion Loss vs. Frequency



Switching Time vs. Bipolar Supply



Switching Time vs. Single Supply

SCHEMATIC DIAGRAM Typical Channel

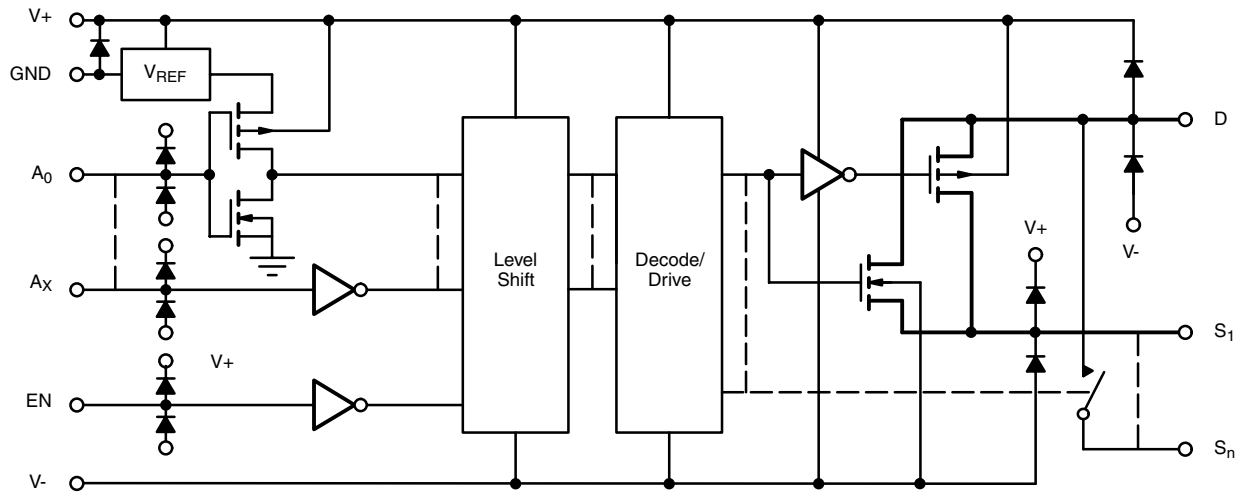


Figure 1.

TEST CIRCUITS

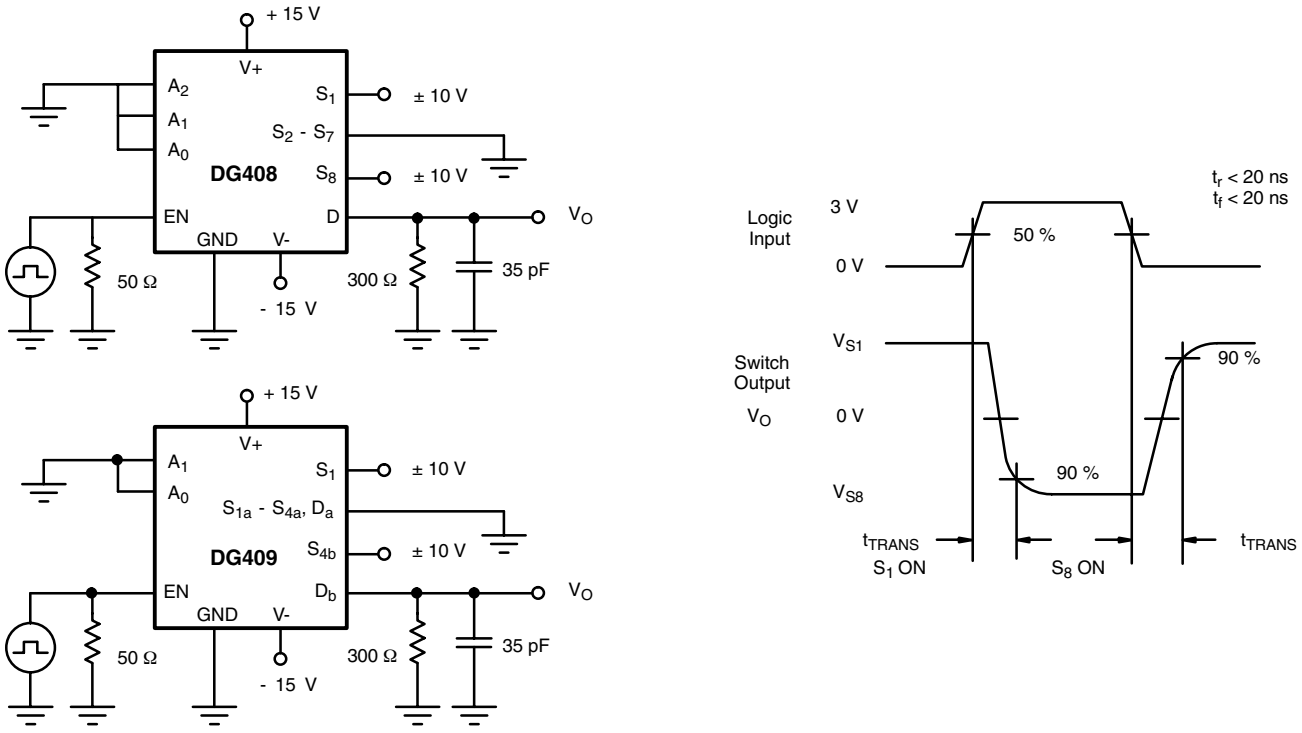


Figure 2. Transition Time

TEST CIRCUITS

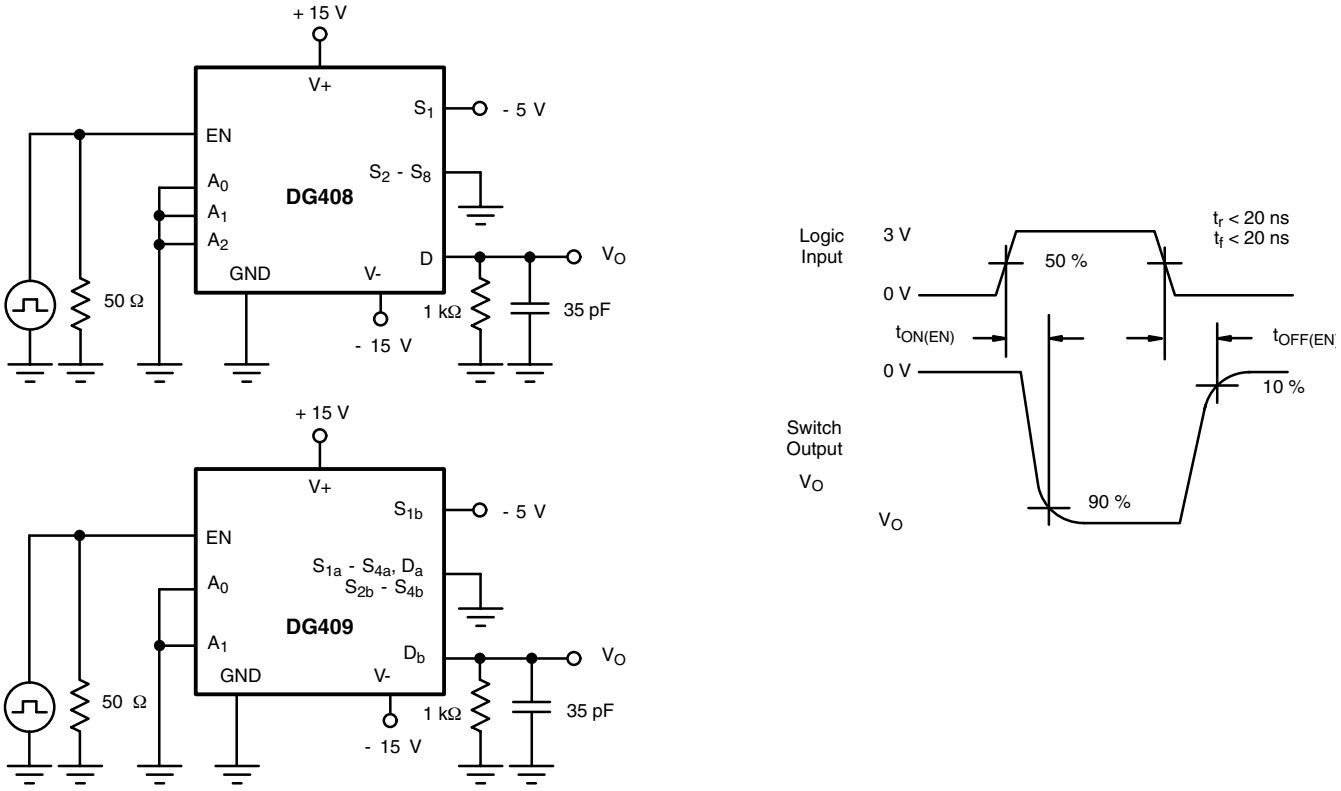


Figure 3. Enable Switching Time

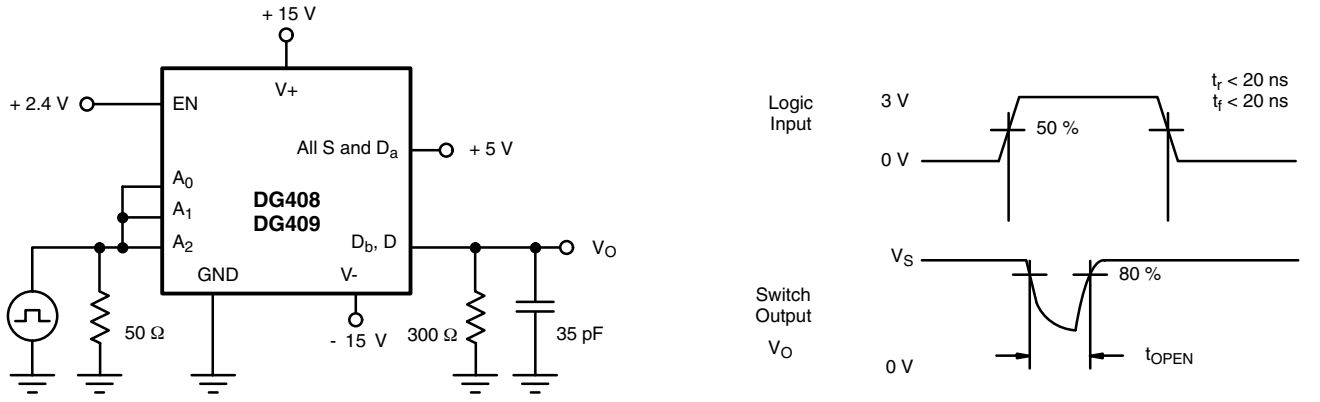


Figure 4. Break-Before-Make Interval

TEST CIRCUITS

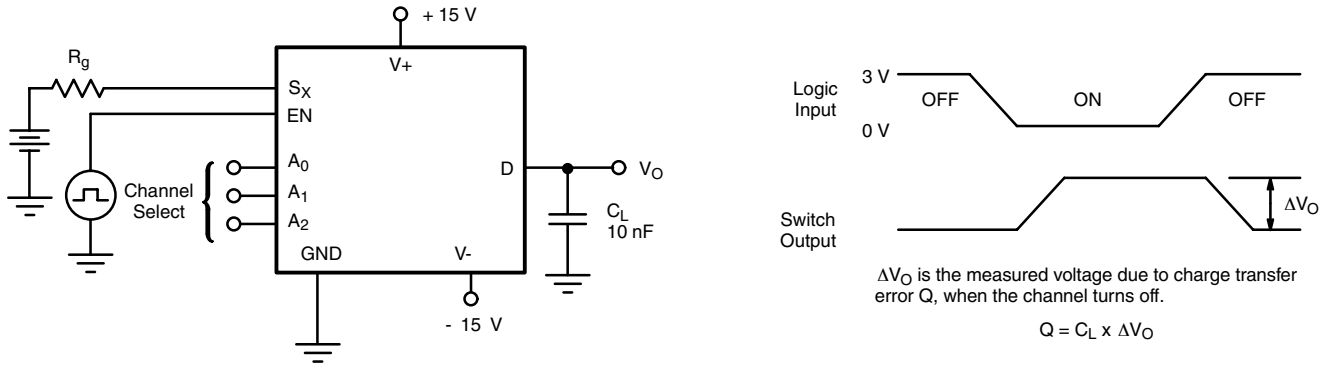


Figure 5. Charge Injection

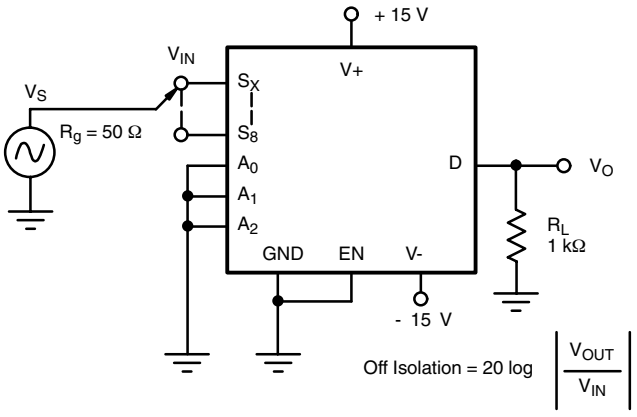


Figure 6. Off Isolation

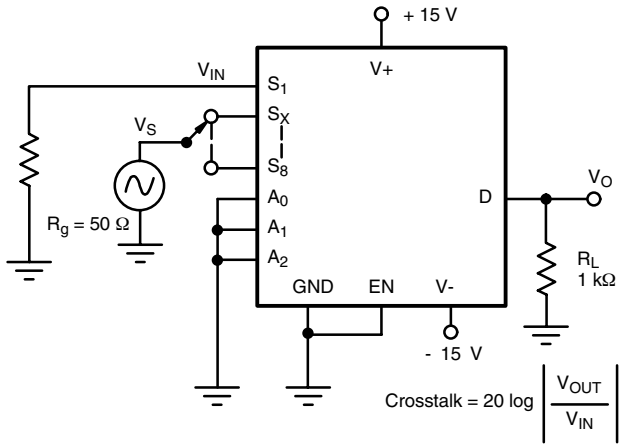


Figure 7. Crosstalk

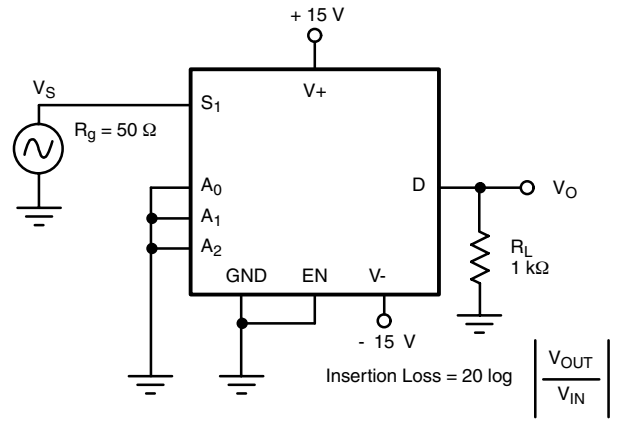


Figure 8. Insertion Loss

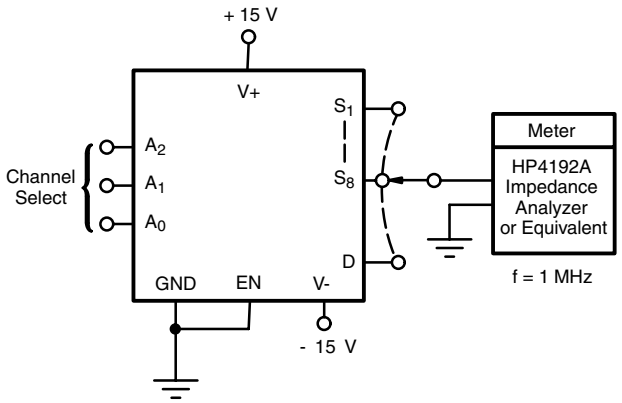


Figure 9. Source Drain Capacitance

APPLICATIONS HINTS

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S - (V-) doesn't exceed + 44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

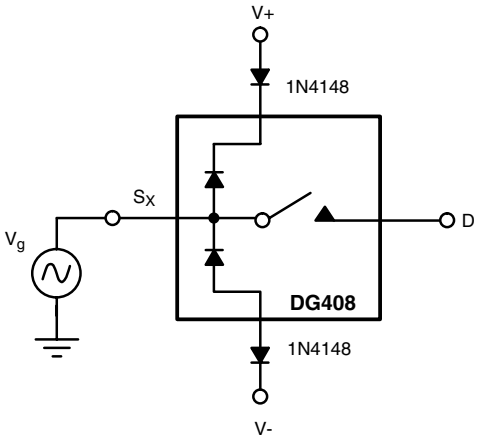
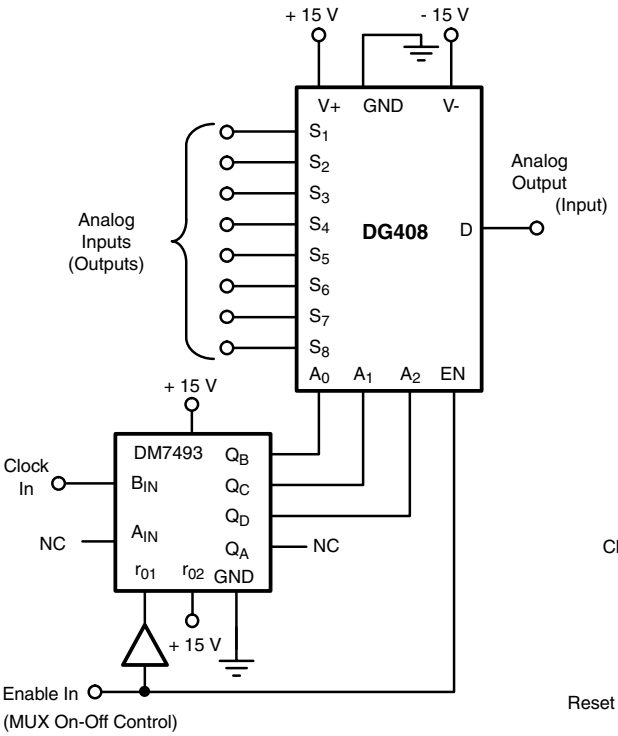


Figure 10. Overvoltage Protection Using Blocking Diodes

8-Channel Sequential Multiplexer/Demultiplexer



Differential 4-Channel Sequential Multiplexer/Demultiplexer

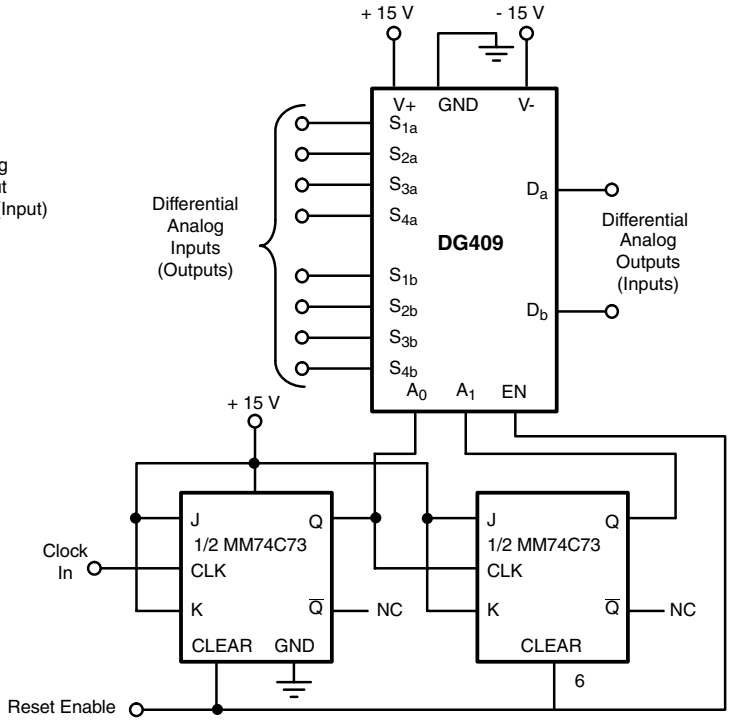


Figure 11.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70062.

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